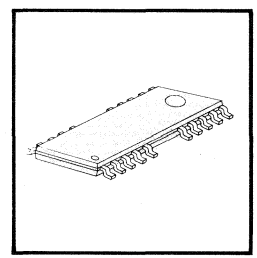
SAMSUNG

Data Book

MOS Memory

Vol. 1 1992/93



• DRAM

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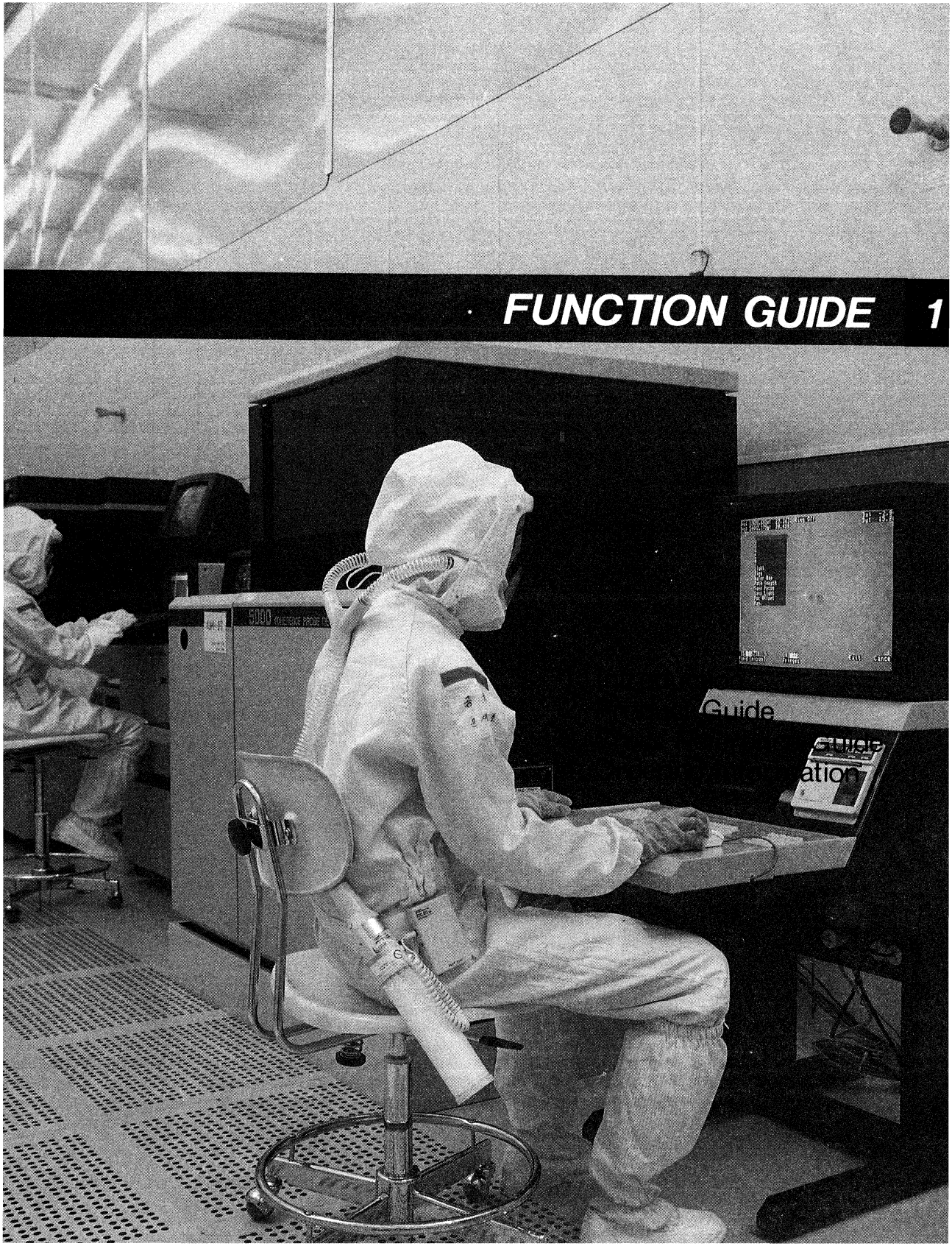
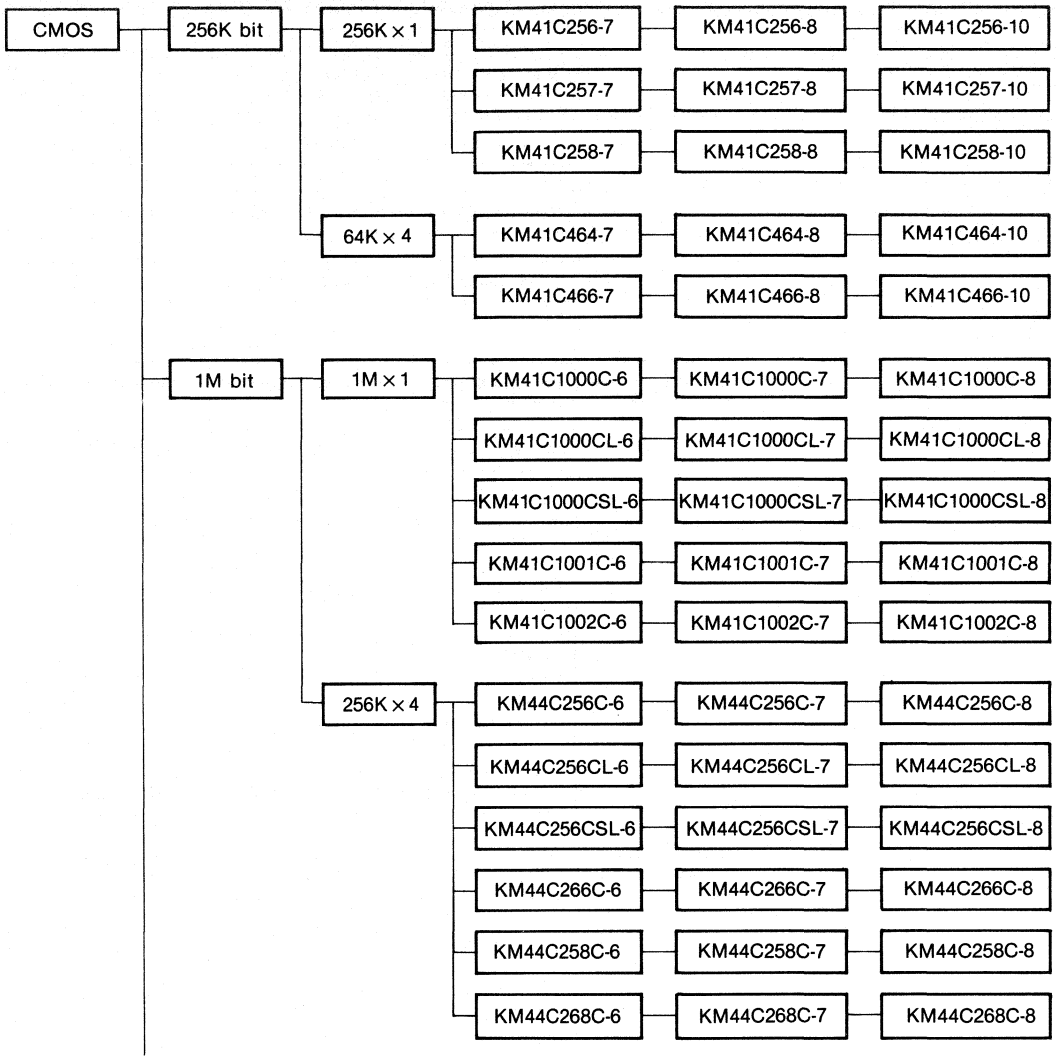
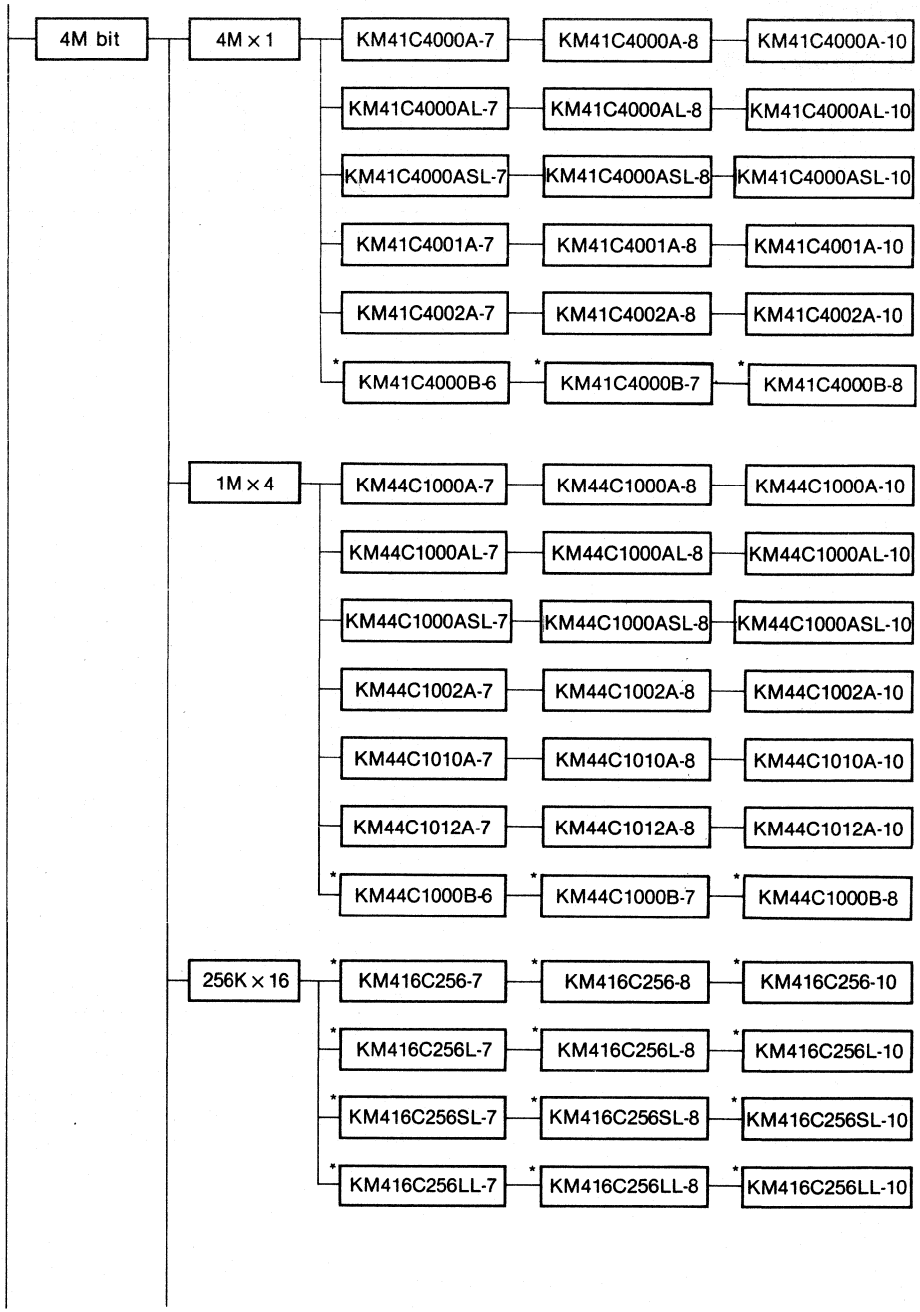
FUNCTION GUIDE 1



1. INTRODUCTION

1.1 Dynamic RAM

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4M × 1
KM41C4000A-7
KM41C4000A-8
KM41C4000A-10
KM41C4000AL-7
KM41C4000AL-8
KM41C4000AL-10
KM41C4000ASL-7
KM41C4000ASL-8
KM41C4000ASL-10
KM41C4001A-7
KM41C4001A-8
KM41C4001A-10
KM41C4002A-7
KM41C4002A-8
KM41C4002A-10
*KM41C4000B-6
*KM41C4000B-7
*KM41C4000B-8
1M × 4
KM44C1000A-7
KM44C1000A-8
KM44C1000A-10
KM44C1000AL-7
KM44C1000AL-8
KM44C1000AL-10
KM44C1000ASL-7
KM44C1000ASL-8
KM44C1000ASL-10
KM44C1002A-7
KM44C1002A-8
KM44C1002A-10
KM44C1010A-7
KM44C1010A-8
KM44C1010A-10
KM44C1012A-7
KM44C1012A-8
KM44C1012A-10
*KM44C1000B-6
*KM44C1000B-7
*KM44C1000B-8
256K × 16
*KM416C256-7
*KM416C256-8
*KM416C256-10
*KM416C256L-7
*KM416C256L-8
*KM416C256L-10
*KM416C256SL-7
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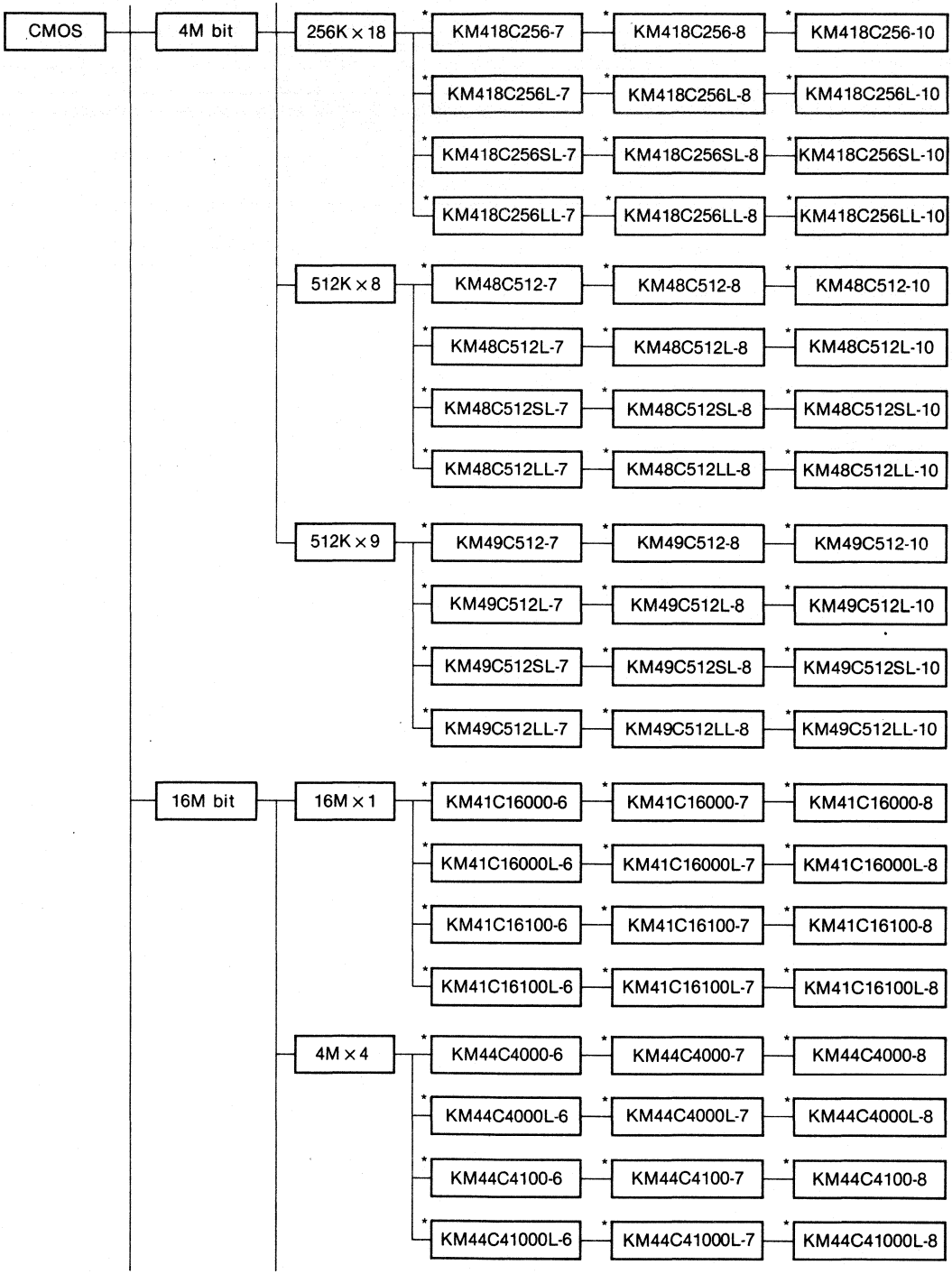
*KM416C256LL-10


CMOS
4M bit
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KM418C256-8
KM418C256-10
KM418C256L-7
KM418C256L-8
KM418C256L-10
KM418C256SL-7
KM418C256SL-8
KM418C256SL-10
KM418C256LL-7
KM418C256LL-8
KM418C256LL-10
512K × 8
KM48C512-7
KM48C512-8
KM48C512-10
KM48C512L-7
KM48C512L-8
KM48C512L-10
KM48C512SL-7
KM48C512SL-8
KM48C512SL-10
KM48C512LL-7
KM48C512LL-8
KM48C512LL-10
512K × 9
KM49C512-7
KM49C512-8
KM49C512-10
KM49C512L-7
KM49C512L-8
KM49C512L-10
KM49C512SL-7
KM49C512SL-8
KM49C512SL-10
KM49C512LL-7
KM49C512LL-8
KM49C512LL-10
16M bit
16M × 1
KM41C16000-6
KM41C16000-7
KM41C16000-8
KM41C16000L-6
KM41C16000L-7
KM41C16000L-8
KM41C16100-6
KM41C16100-7
KM41C16100-8
KM41C16100L-6
KM41C16100L-7
KM41C16100L-8
4M × 4
KM44C4000-6
KM44C4000-7
KM44C4000-8
KM44C4000L-6
KM44C4000L-7
KM44C4000L-8
KM44C4100-6
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KM44C41000L-7
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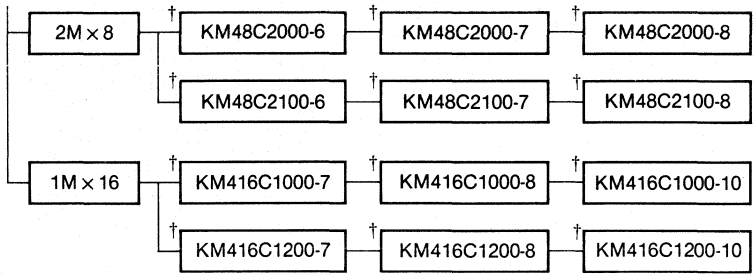
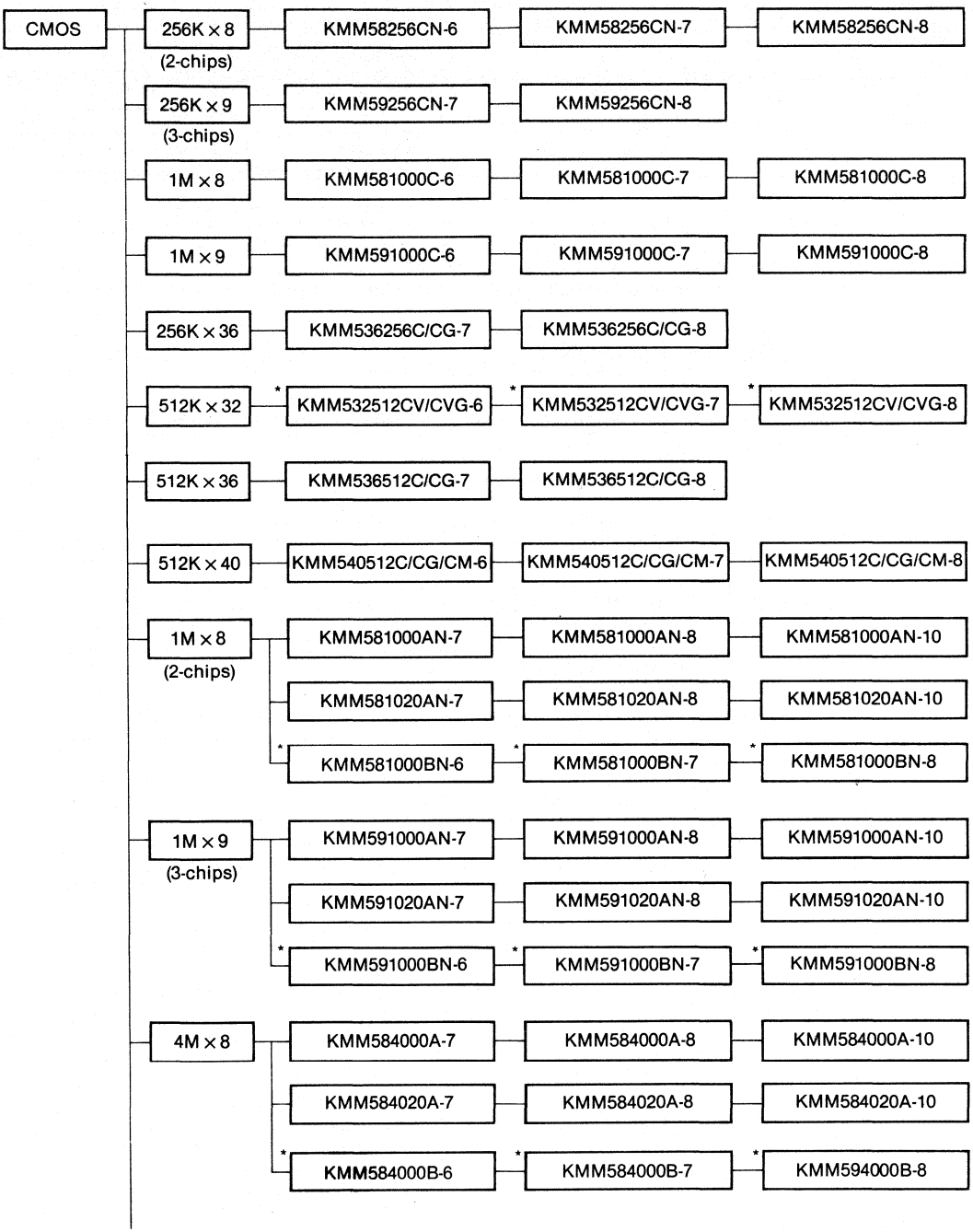
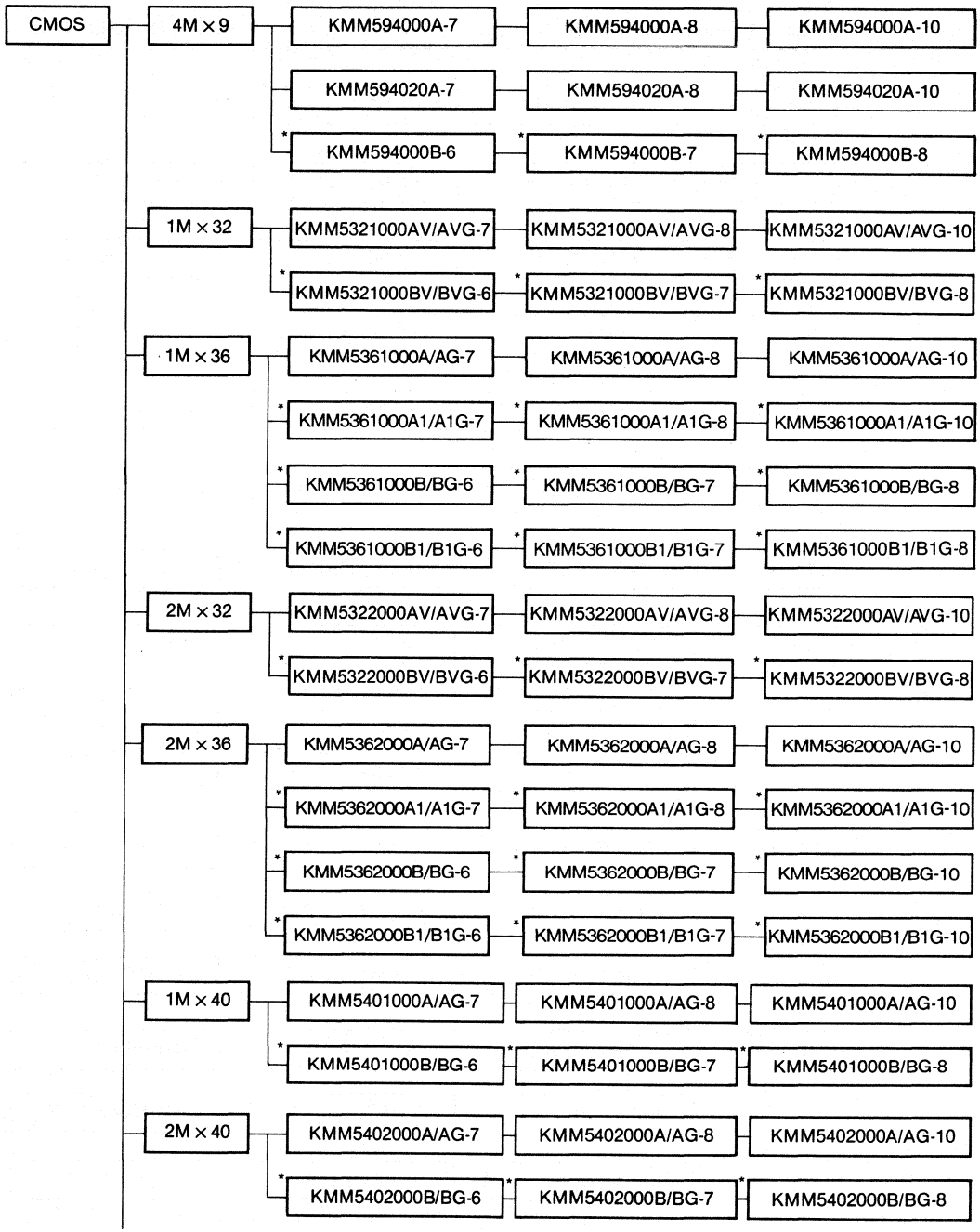
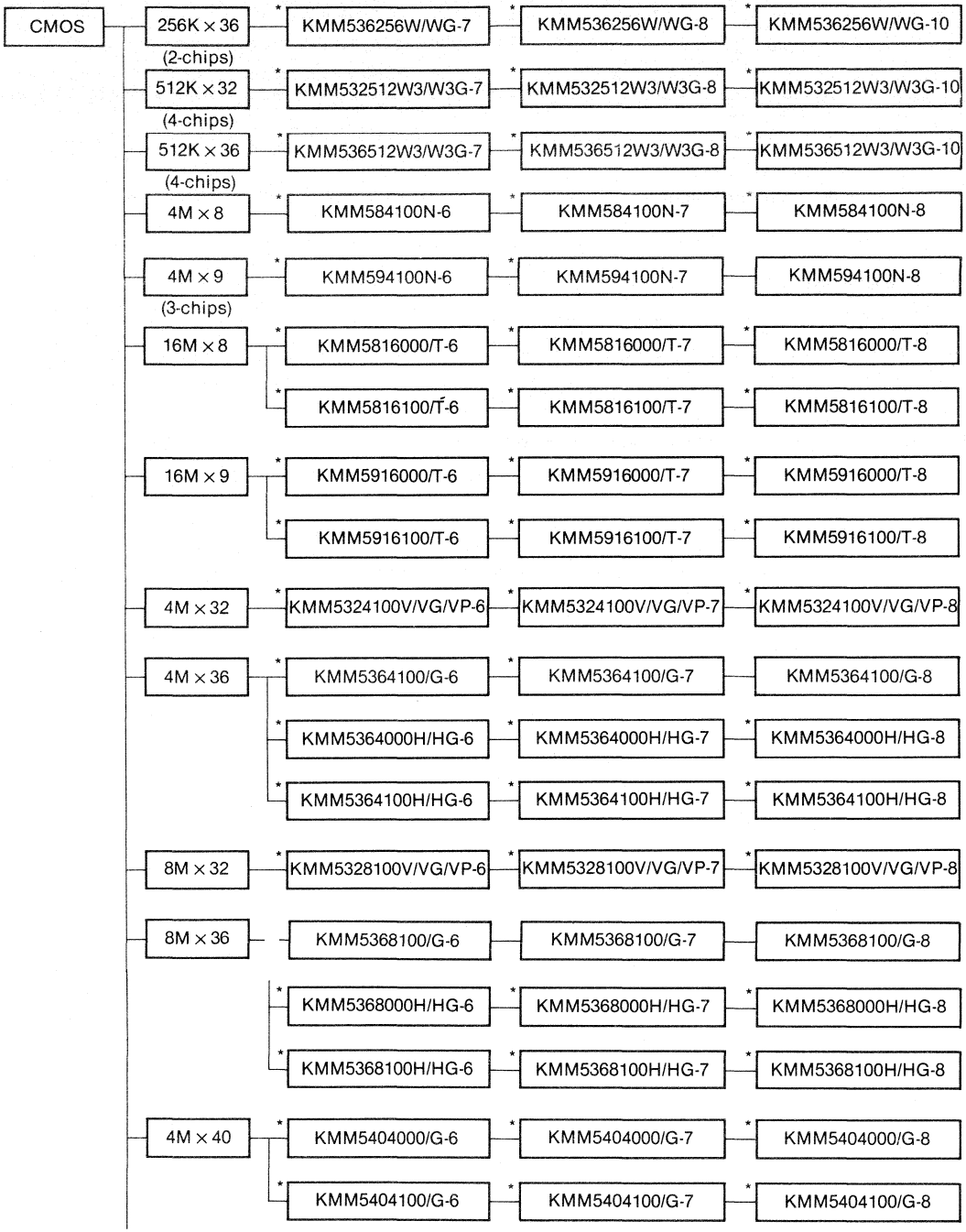


*: New Product
†: Preliminary Product
††: Under Development

1.2 Dynamic RAM Module




CMOS
4M x 9
KMM594000A-7
KMM594000A-8
KMM594000A-10
KMM594020A-7
KMM594020A-8
KMM594020A-10
*KMM594000B-6
*KMM594000B-7
*KMM594000B-8
1M x 32
KMM5321000AV/AVG-7
KMM5321000AV/AVG-8
KMM5321000AV/AVG-10
*KMM5321000BV/BVG-6
*KMM5321000BV/BVG-7
*KMM5321000BV/BVG-8
1M x 36
KMM5361000A/AG-7
KMM5361000A/AG-8
KMM5361000A/AG-10
*KMM5361000A1/A1G-7
*KMM5361000A1/A1G-8
*KMM5361000A1/A1G-10
*KMM5361000B/BG-6
*KMM5361000B/BG-7
*KMM5361000B/BG-8
*KMM5361000B1/B1G-6
*KMM5361000B1/B1G-7
*KMM5361000B1/B1G-8
2M x 32
KMM5322000AV/AVG-7
KMM5322000AV/AVG-8
KMM5322000AV/AVG-10
*KMM5322000BV/BVG-6
*KMM5322000BV/BVG-7
*KMM5322000BV/BVG-8
2M x 36
KMM5362000A/AG-7
KMM5362000A/AG-8
KMM5362000A/AG-10
*KMM5362000A1/A1G-7
*KMM5362000A1/A1G-8
*KMM5362000A1/A1G-10
*KMM5362000B/BG-6
*KMM5362000B/BG-7
*KMM5362000B/BG-10
*KMM5362000B1/B1G-6
*KMM5362000B1/B1G-7
*KMM5362000B1/B1G-10
1M x 40
KMM5401000A/AG-7
KMM5401000A/AG-8
KMM5401000A/AG-10
*KMM5401000B/BG-6
*KMM5401000B/BG-7
*KMM5401000B/BG-8
2M x 40
KMM5402000A/AG-7
KMM5402000A/AG-8
KMM5402000A/AG-10
*KMM5402000B/BG-6
*KMM5402000B/BG-7
*KMM5402000B/BG-8


CMOS
256K × 36
(2-chips)
KMM536256W/WG-7
KMM536256W/WG-8
KMM536256W/WG-10
512K × 32
(4-chips)
KMM532512W3/W3G-7
KMM532512W3/W3G-8
KMM532512W3/W3G-10
512K × 36
(4-chips)
KMM536512W3/W3G-7
KMM536512W3/W3G-8
KMM536512W3/W3G-10
4M × 8
KMM584100N-6
KMM584100N-7
KMM584100N-8
4M × 9
(3-chips)
KMM594100N-6
KMM594100N-7
KMM594100N-8
16M × 8
KMM5816000/T-6
KMM5816000/T-7
KMM5816000/T-8
KMM5816100/T-6
KMM5816100/T-7
KMM5816100/T-8
16M × 9
KMM5916000/T-6
KMM5916000/T-7
KMM5916000/T-8
KMM5916100/T-6
KMM5916100/T-7
KMM5916100/T-8
4M × 32
KMM5324100V/VG/VP-6
KMM5324100V/VG/VP-7
KMM5324100V/VG/VP-8
4M × 36
KMM5364100/G-6
KMM5364100/G-7
KMM5364100/G-8
KMM5364000H/HG-6
KMM5364000H/HG-7
KMM5364000H/HG-8
KMM5364100H/HG-6
KMM5364100H/HG-7
KMM5364100H/HG-8
8M × 32
KMM5328100V/VG/VP-6
KMM5328100V/VG/VP-7
KMM5328100V/VG/VP-8
8M × 36
KMM5368100/G-6
KMM5368100/G-7
KMM5368100/G-8
KMM5368000H/HG-6
KMM5368000H/HG-7
KMM5368000H/HG-8
KMM5368100H/HG-6
KMM5368100H/HG-7
KMM5368100H/HG-8
4M × 40
KMM5404000/G-6
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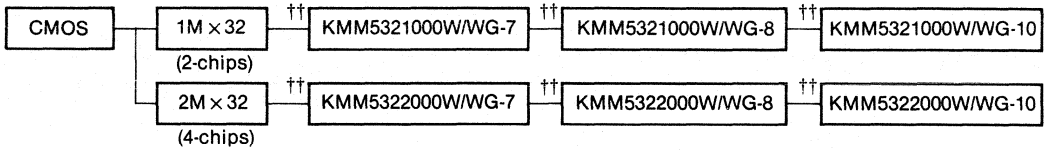
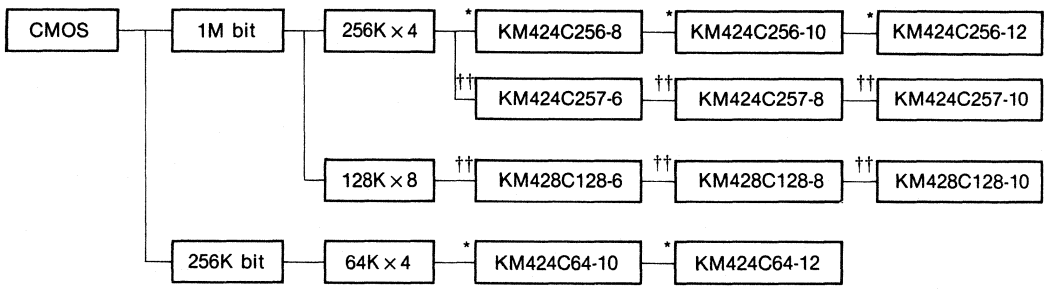
KMM5404000/G-8
KMM5404100/G-6
KMM5404100/G-7
KMM5404100/G-8



* New Product
†† Under Development

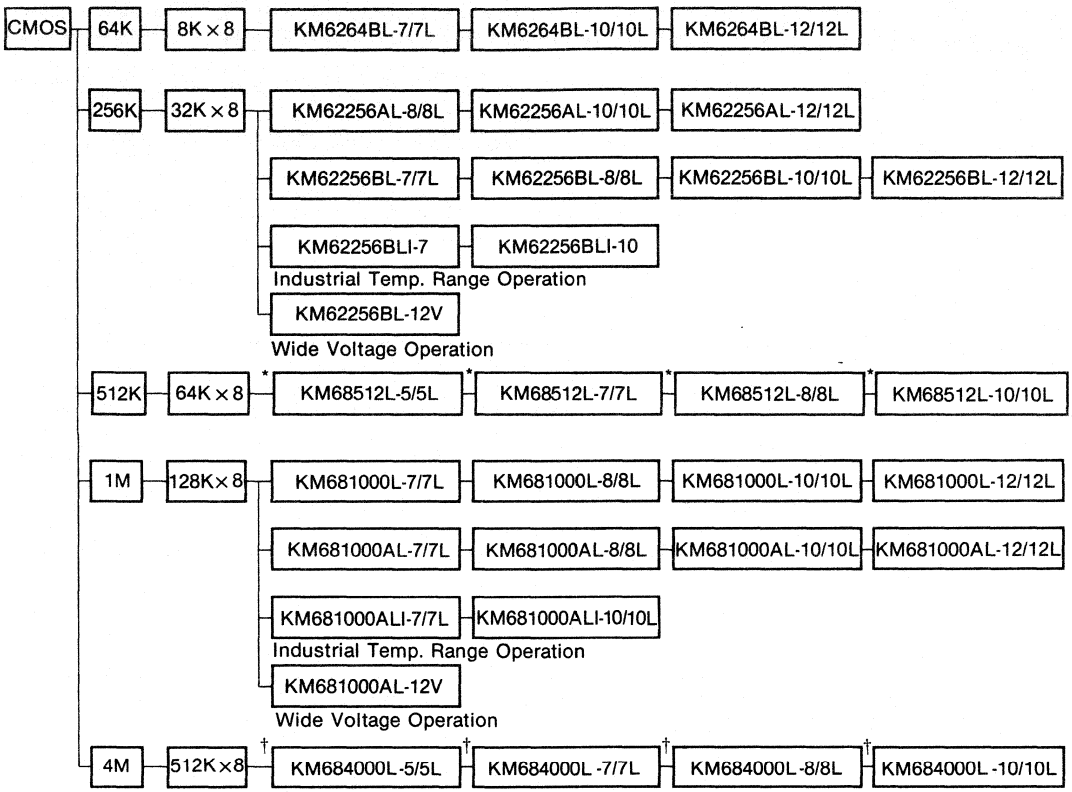
1.3 Video RAM



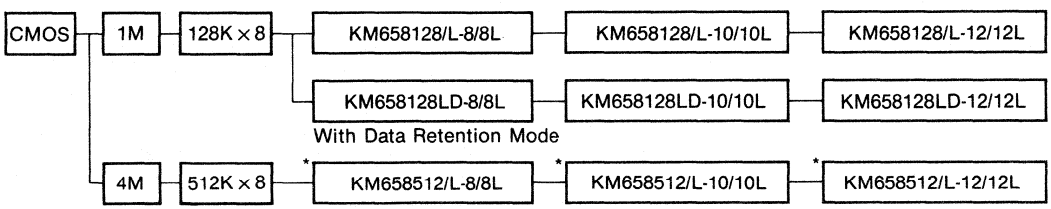
*: New Product
†: Preliminary Product
††: Under Development

1.4 Static RAM

Low Power SRAMs

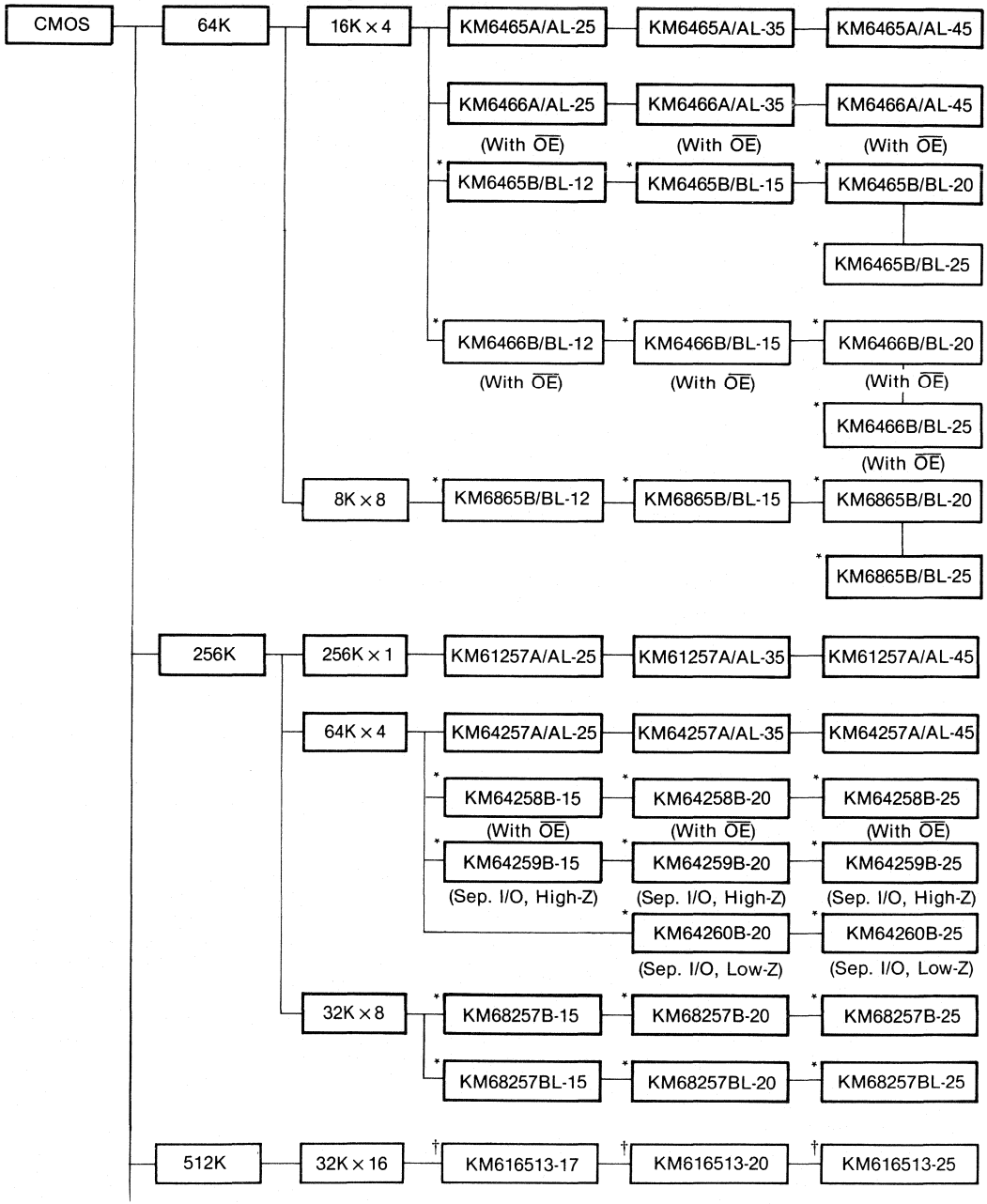


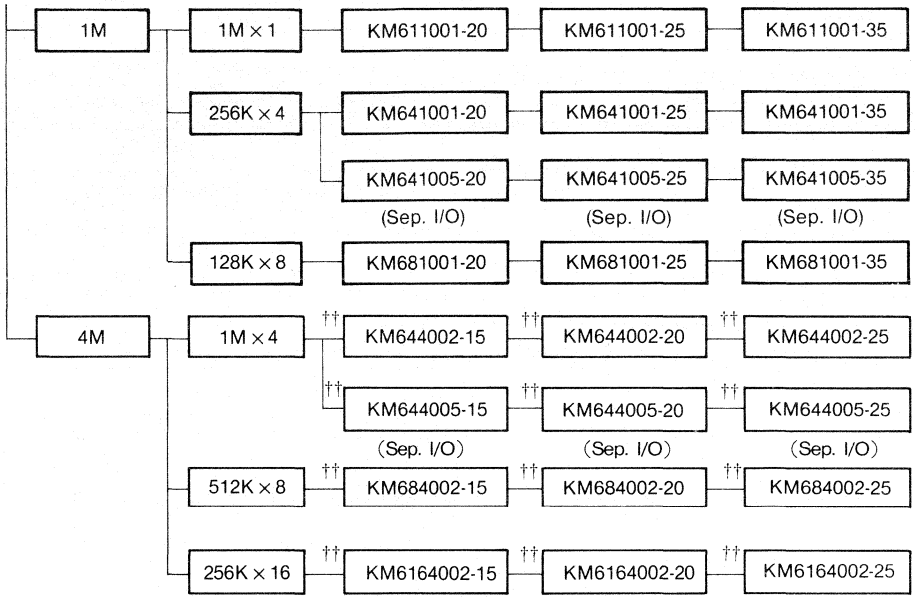
Pseudo SRAM Product Tree



* New Product
† Preliminary Product
†† Under Development

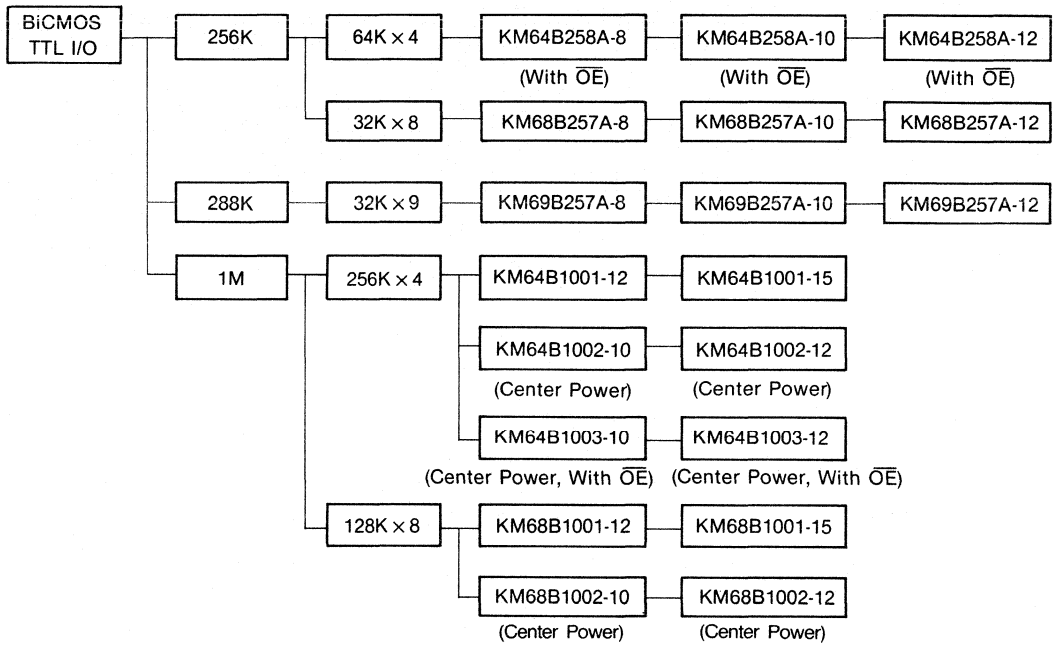
High Speed SRAM



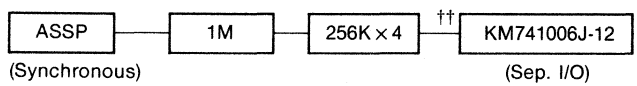

1M
1M × 1
KM611001-20
KM611001-25
KM611001-35
256K × 4
KM641001-20
KM641001-25
KM641001-35
KM641005-20
KM641005-25
KM641005-35
(Sep. I/O)
(Sep. I/O)
(Sep. I/O)
128K × 8
KM681001-20
KM681001-25
KM681001-35
4M
1M × 4
††
KM644002-15
KM644002-20
KM644002-25
KM644005-15
KM644005-20
KM644005-25
(Sep. I/O)
(Sep. I/O)
(Sep. I/O)
512K × 8
KM684002-15
KM684002-20
KM684002-25
256K × 16
KM6164002-15
KM6164002-20
KM6164002-25

1

*** BiCMOS SRAM**

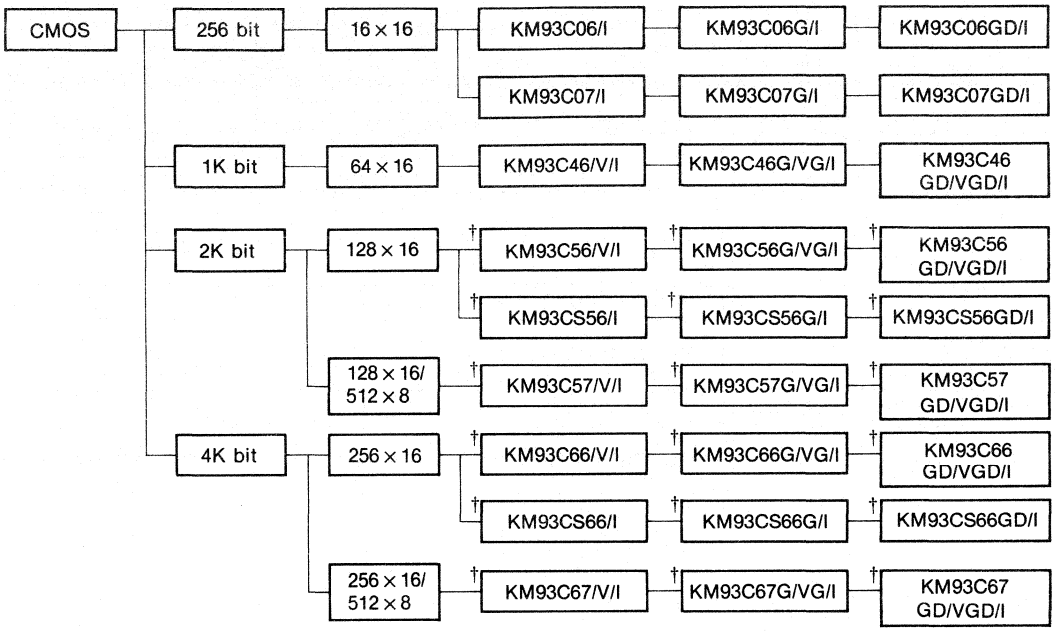


Specialty SRAM

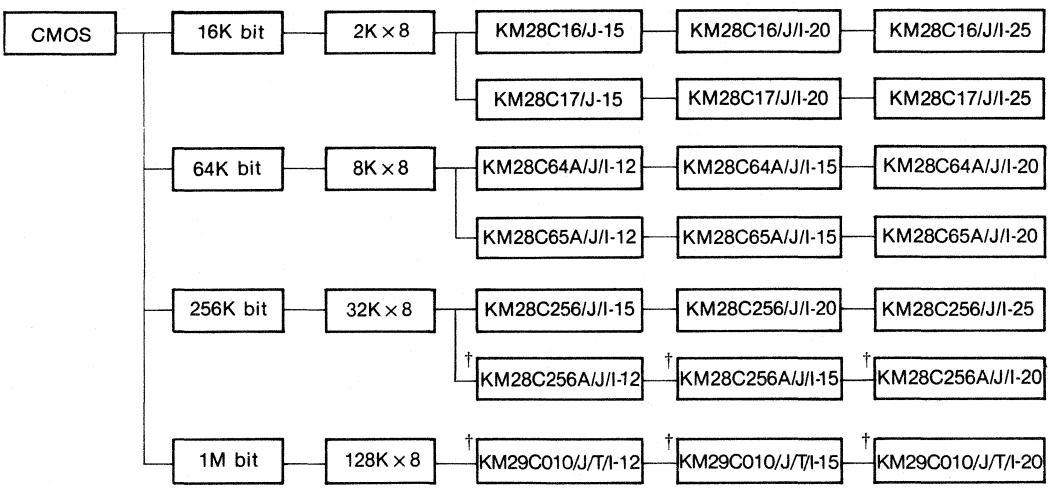


* New Product
† Preliminary Product
†† Under Development

1.5 Serial EEPROM

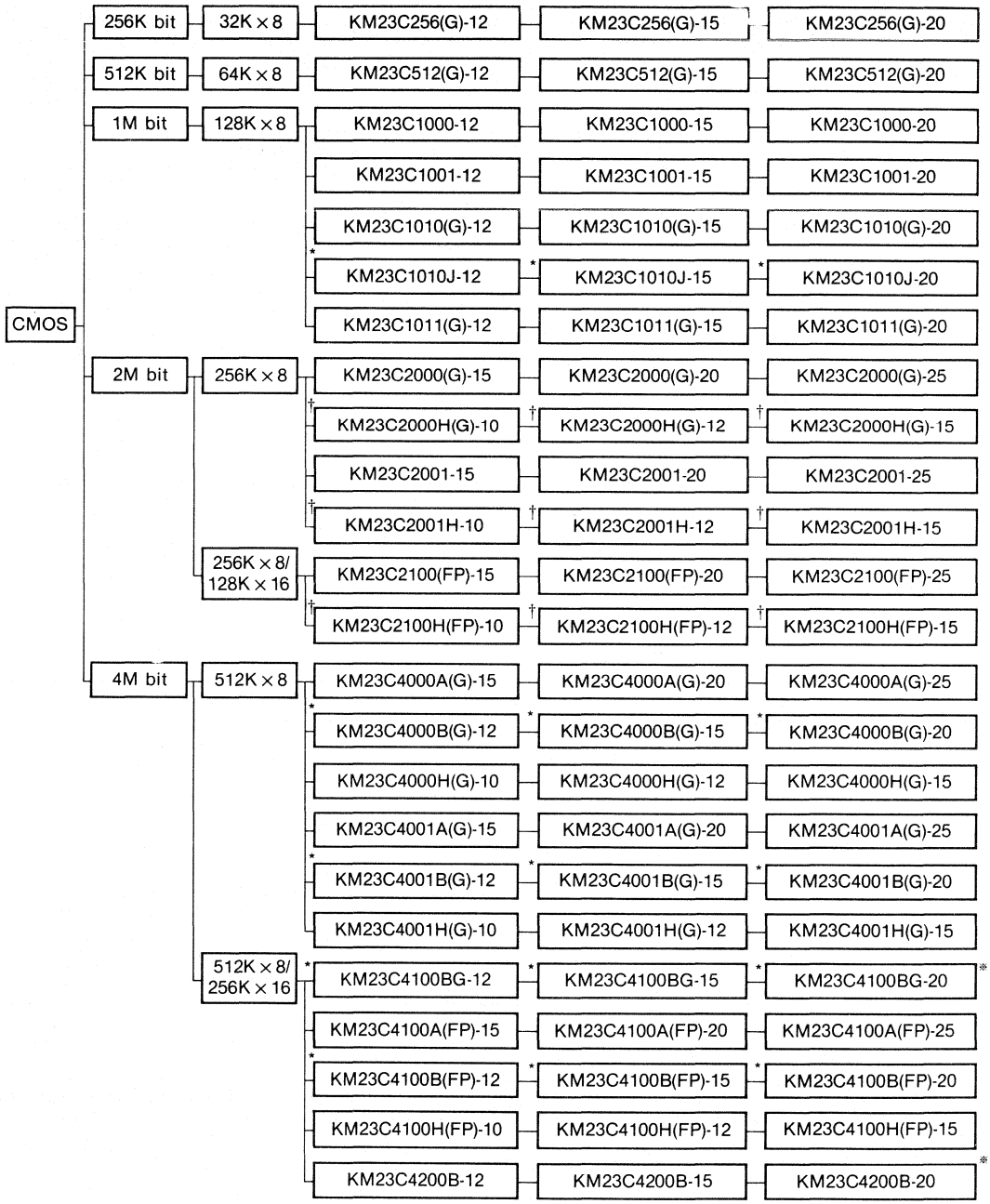


Parallel EEPROM



* New Product † Preliminary Product

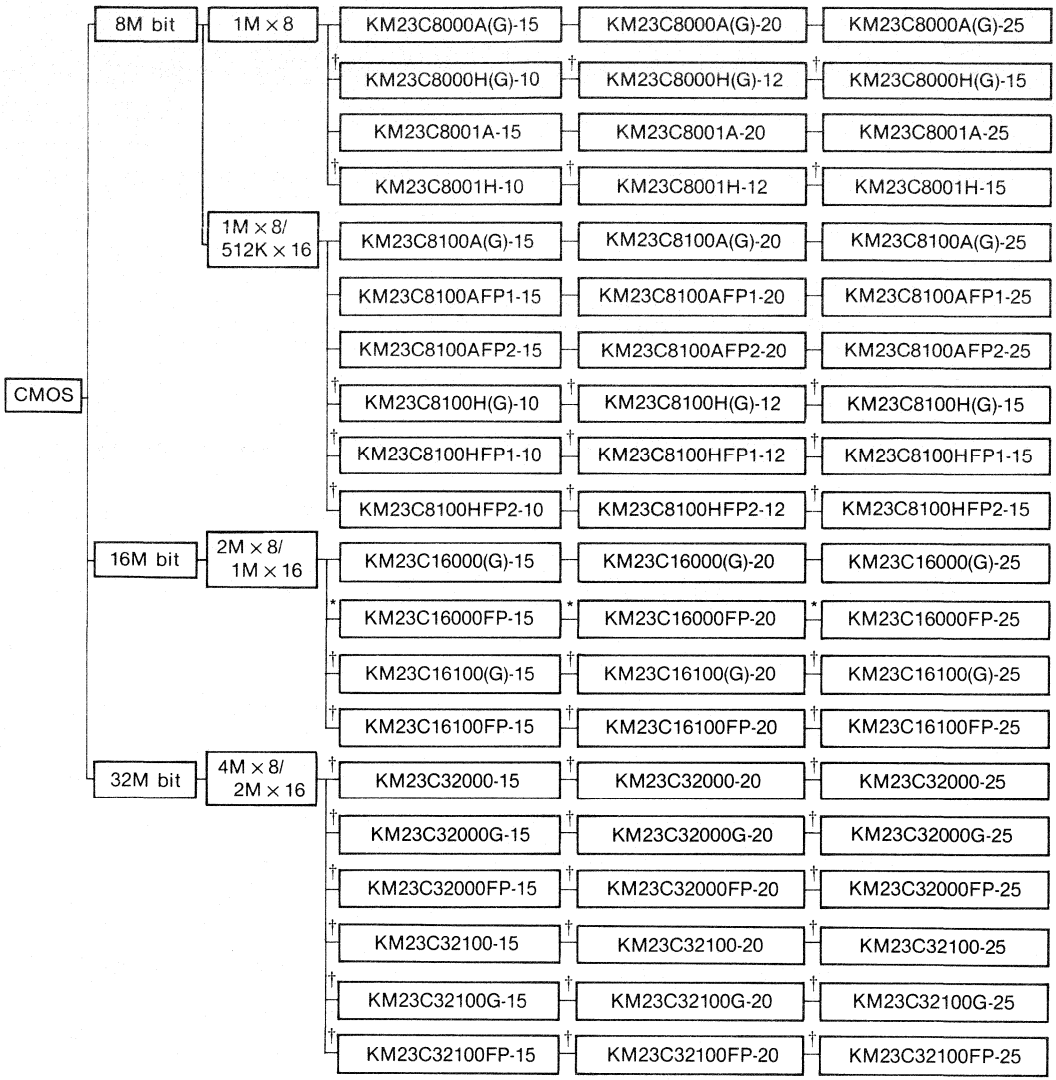
1.6 MASKROM- I (Low Density)



* New Product † Under Development

※ Both A and B ver. are available in 3Q '92

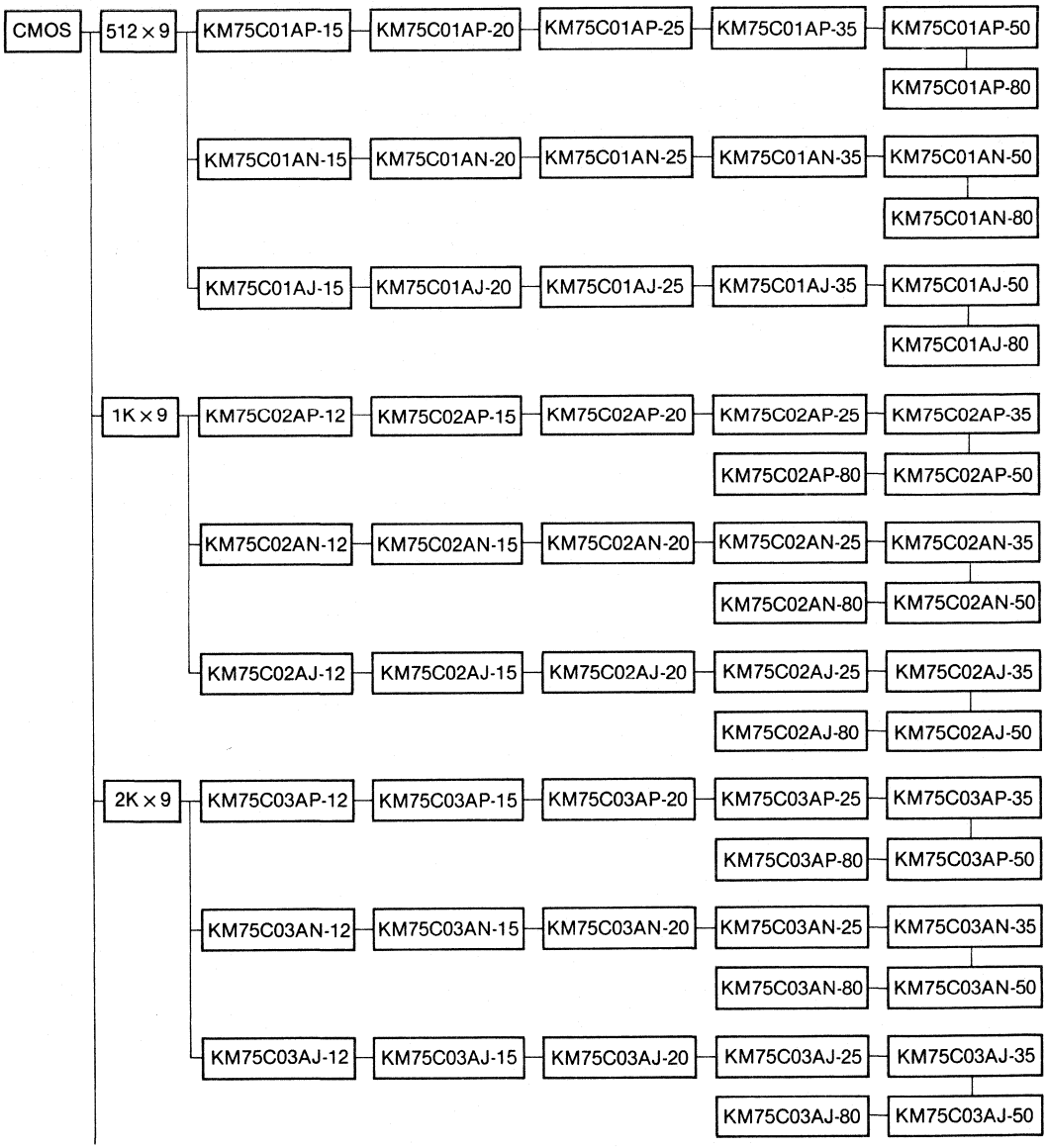
MASKROM-II (High Density)

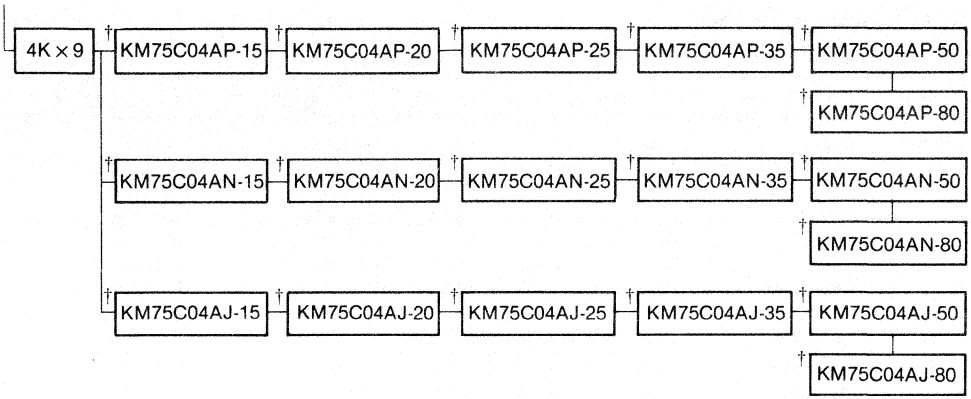


* New Product
† Under Development

1.7 Application Specific Memory

STANDARD FIFO





*AP: PDIP (0.6″)
AN: PDIP (0.3″)
AJ: PLCC
†: Preliminary Product

2. PRODUCT GUIDE

2.1 Dynamic RAM

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
256K bit	KM41C256P	256K x 1	70/80/100	CMOS	Fast Page	16 Pin DIP	Now
	KM41C256J	256K x 1	70/80/100	CMOS	Fast Page	18 Pin PLCC	Now
	KM41C256Z	256K x 1	70/80/100	CMOS	Fast Page	16 Pin ZIP	Now
	KM41C257P	256K x 1	70/80/100	CMOS	Nibble Mode	16 Pin DIP	Now
	KM41C257J	256K x 1	70/80/100	CMOS	Nibble Mode	18 Pin PLCC	Now
	KM41C257Z	256K x 1	70/80/100	CMOS	Nibble Mode	16 Pin ZIP	Now
	KM41C258P	256K x 1	70/80/100	CMOS	Static Column	16 Pin DIP	Now
	KM41C258J	256K x 1	70/80/100	CMOS	Static Column	18 Pin PLCC	Now
	KM41C258Z	256K x 1	70/80/100	CMOS	Static Column	16 Pin ZIP	Now
	KM41C464P	64K x 4	70/80/100	CMOS	Fast Page	18 Pin DIP	Now
	KM41C464J	64K x 4	70/80/100	CMOS	Fast Page	18 Pin PLCC	Now
	KM41C464Z	64K x 4	70/80/100	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C466P	64K x 4	70/80/100	CMOS	Static Column	18 Pin DIP	Now
	KM41C466J	64K x 4	70/80/100	CMOS	Static Column	18 Pin PLCC	Now
	KM41C466Z	64K x 4	70/80/100	CMOS	Static Column	20 Pin ZIP	Now
1M bit	KM41C1000CP	1M x 1	60/70/80	CMOS	Fast Page	18 Pin DIP	Now
	KM41C1000CJ	1M x 1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM41C1000CZ	1M x 1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C1000CV	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM41C1000CVR	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM41C1000CT	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM41C1000CTR	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM41C1000CLP	1M x 1	60/70/80	CMOS	Fast Page	18 Pin DIP	Now
	KM41C1000CLJ	1M x 1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM41C1000CLZ	1M x 1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C1000CLV	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM41C1000CLVR	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM41C1000CLT	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM41C1000CLTR	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM41C1000CSLP	1M x 1	60/70/80	CMOS	Fast Page	18 Pin DIP	Now
	KM41C1000CSLJ	1M x 1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM41C1000CSLZ	1M x 1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM41C1000CSLV	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM41C1000CSLVR	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM41C1000CSLT	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM41C1000CSLTR	1M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM41C1001CP	1M x 1	60/70/80	CMOS	Nibble Mode	18 Pin DIP	Now
	KM41C1001CJ	1M x 1	60/70/80	CMOS	Nibble Mode	20 Pin SOJ	Now
	KM41C1001CZ	1M x 1	60/70/80	CMOS	Nibble Mode	20 Pin ZIP	Now
	KM41C1001CV	1M x 1	60/70/80	CMOS	Nibble Mode	20 Pin TSOP-I(Forward)	Now
	KM41C1001CVR	1M x 1	60/70/80	CMOS	Nibble Mode	20 Pin TSOP-I(Reverse)	Now
	KM41C1001CT	1M x 1	60/70/80	CMOS	Nibble Mode	20 Pin TSOP-II(Forward)	Now
	KM41C1001CTR	1M x 1	60/70/80	CMOS	Nibble Mode	20 Pin TSOP-II(Reverse)	Now
	KM41C1002CP	1M x 1	60/70/80	CMOS	Static Column	18 Pin DIP	Now
	KM41C1002CJ	1M x 1	60/70/80	CMOS	Static Column	20 Pin SOJ	Now
	KM41C1002CZ	1M x 1	60/70/80	CMOS	Static Column	20 Pin ZIP	Now
	KM41C1002CV	1M x 1	60/70/80	CMOS	Static Column	20 Pin TSOP-I(Forward)	Now
	KM41C1002CVR	1M x 1	60/70/80	CMOS	Static Column	20 Pin TSOP-I(Reverse)	Now
	KM41C1002CT	1M x 1	60/70/80	CMOS	Static Column	20 Pin TSOP-II(Forward)	Now
	KM41C1002CTR	1M x 1	60/70/80	CMOS	Static Column	20 Pin TSOP-II(Reverse)	Now

Dynamic RAM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
1M bit	KM44C256CP	256K x 4	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	KM44C256CJ	256K x 4	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM44C256CZ	256K x 4	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM44C256CV	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM44C256CVR	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM44C256CT	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM44C256CTR	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM44C256CLP	256K x 4	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	KM44C256CLJ	256K x 4	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM44C256CLZ	256K x 4	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM44C256CLV	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM44C256CLVR	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM44C256CLT	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM44C256CLTR	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM44C256CSLP	256K x 4	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	KM44C256CSLJ	256K x 4	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	KM44C256CSLZ	256K x 4	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	KM44C256CSLV	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	KM44C256CSLVR	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	KM44C256CSLT	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	KM44C256CSLTR	256K x 4	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	KM44C266CP	256K x 4	60/70/80	CMOS	Fast Page with WPB	20 Pin DIP	Now
	KM44C266CJ	256K x 4	60/70/80	CMOS	Fast Page with WPB	20 Pin SOJ	Now
	KM44C266CZ	256K x 4	60/70/80	CMOS	Fast Page with WPB	20 Pin ZIP	Now
	KM44C266CV	256K x 4	60/70/80	CMOS	Fast Page with WPB	20 Pin TSOP-I(Forward)	Now
	KM44C266CVR	256K x 4	60/70/80	CMOS	Fast Page with WPB	20 Pin TSOP-I(Reverse)	Now
	KM44C266CT	256K x 4	60/70/80	CMOS	Fast Page with WPB	20 Pin TSOP-II(Forward)	Now
	KM44C266CTR	256K x 4	60/70/80	CMOS	Fast Page with WPB	20 Pin TSOP-II(Reverse)	Now
	KM44C258CP	256K x 4	60/70/80	CMOS	Static Column	20 Pin DIP	Now
	KM44C258CJ	256K x 4	60/70/80	CMOS	Static Column	20 Pin SOJ	Now
	KM44C258CZ	256K x 4	60/70/80	CMOS	Static Column	20 Pin ZIP	Now
	KM44C258CV	256K x 4	60/70/80	CMOS	Static Column	20 Pin TSOP-I(Forward)	Now
	KM44C258CVR	256K x 4	60/70/80	CMOS	Static Column	20 Pin TSOP-I(Reverse)	Now
	KM44C258CT	256K x 4	60/70/80	CMOS	Static Column	20 Pin TSOP-II(Forward)	Now
	KM44C258CTR	256K x 4	60/70/80	CMOS	Static Column	20 Pin TSOP-II(Reverse)	Now
	KM44C268CP	256K x 4	60/70/80	CMOS	Static Column with WPB	20 Pin DIP	Now
	KM44C268CJ	256K x 4	60/70/80	CMOS	Static Column with WPB	20 Pin SOJ	Now
	KM44C268CZ	256K x 4	60/70/80	CMOS	Static Column with WPB	20 Pin ZIP	Now
	KM44C268CV	256K x 4	60/70/80	CMOS	Static Column with WPB	20 Pin TSOP-I(Forward)	Now
	KM44C268CVR	256K x 4	60/70/80	CMOS	Static Column with WPB	20 Pin TSOP-I(Reverse)	Now
	KM44C268CT	256K x 4	60/70/80	CMOS	Static Column with WPB	20 Pin TSOP-II(Forward)	Now
	KM44C268CTR	256K x 4	60/70/80	CMOS	Static Column with WPB	20 Pin TSOP-II(Reverse)	Now
4M bit	*KM41C4000BP	4M x 1	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	*KM41C4000BJ	4M x 1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	*KM41C4000BZ	4M x 1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	*KM41C4000BV	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	*KM41C4000BVR	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	*KM41C4000BT	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	*KM41C4000BTR	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	*KM41C4000BLP	4M x 1	60/70/80	CMOS	Fast Page	20 Pin DIP	Now

Dynamic RAM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
4M bit	*KM41C4000BLJ	4M x 1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	*KM41C4000BLZ	4M x 1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	*KM41C4000BLV	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	*KM41C4000BLVR	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	*KM41C4000BLT	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	*KM41C4000BLTR	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
	*KM41C4000BSLP	4M x 1	60/70/80	CMOS	Fast Page	20 Pin DIP	Now
	*KM41C4000BSLJ	4M x 1	60/70/80	CMOS	Fast Page	20 Pin SOJ	Now
	*KM41C4000BSLZ	4M x 1	60/70/80	CMOS	Fast Page	20 Pin ZIP	Now
	*KM41C4000BSLV	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Forward)	Now
	*KM41C4000BSLVR	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-I(Reverse)	Now
	*KM41C4000BSLT	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Forward)	Now
	*KM41C4000BSLTR	4M x 1	60/70/80	CMOS	Fast Page	20 Pin TSOP-II(Reverse)	Now
4M B/W	*KM48C512J	512K x 8	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM48C512Z	512K x 8	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM48C512T	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM48C512TR	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM48C512LJ	512K x 8	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM48C512LZ	512K x 8	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM48C512LT	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM48C512LTR	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM48C512SLJ	512K x 8	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM48C512SLZ	512K x 8	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM48C512SLT	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM48C512SLTR	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM48C512LLJ	512K x 8	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM48C512LLZ	512K x 8	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM48C512LLT	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM48C512LLTR	512K x 8	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM49C512J	512K x 9	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM49C512Z	512K x 9	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM49C512T	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM49C512TR	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM49C512LJ	512K x 9	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM49C512LZ	512K x 9	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM49C512LT	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM49C512LTR	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM49C512SLJ	512K x 9	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM49C512SLZ	512K x 9	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM49C512SLT	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM49C512SLTR	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM49C512LLJ	512K x 9	70/80/100	CMOS	Fast Page	28 Pin SOJ	Now
	*KM49C512LLZ	512K x 9	70/80/100	CMOS	Fast Page	28 Pin ZIP	Now
	*KM49C512LLT	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Forward)	Now
	*KM49C512LLTR	512K x 9	70/80/100	CMOS	Fast Page	28 Pin TSOP-II(Reverse)	Now
	*KM416C256J	256K x 16	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM416C256Z	256K x 16	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now
	*KM416C256LJ	256K x 16	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM416C256LZ	256K x 16	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now
	*KM416C256SLJ	256K x 16	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM416C256SLZ	256K x 16	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now
	*KM416C256LLJ	256K x 16	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM416C256LLZ	256K x 16	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now

Dynamic RAM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
4M B/W	*KM418C256J	256K x 18	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM418C256Z	256K x 18	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now
	*KM418C256LJ	256K x 18	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM418C256LZ	256K x 18	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now
	*KM418C256SLJ	256K x 18	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM418C256SLZ	256K x 18	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now
	*KM418C256LLJ	256K x 18	70/80/100	CMOS	Fast Page	40 Pin SOJ	Now
	*KM418C256LLZ	256K x 18	70/80/100	CMOS	Fast Page	40 Pin ZIP	Now
16M	*KM41C16000J	16M x 1	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM41C16000T	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM41C16000TR	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM41C16000LJ	16M x 1	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM41C16000LT	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM41C16000LTR	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM41C16100J	16M x 1	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM41C16100T	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM41C16100TR	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM41C16100LJ	16M x 1	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM41C16100LT	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM41C16100LTR	16M x 1	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4000J	4M x 4	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM44C4000T	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4000TR	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4000LJ	4M x 4	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM44C4000LT	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4000LTR	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4100J	4M x 4	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM44C4100T	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4100TR	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4100LJ	4M x 4	60/70/80	CMOS	Fast Page	24 PIN SOJ	Now
	*KM44C4100LT	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
	*KM44C4100LTR	4M x 4	60/70/80	CMOS	Fast Page	24 Pin TSOP-II	Now
16M B/W	†KM48C2000J	2M x 8	60/70/80	CMOS	Fast Page	28 Pin SOJ	3Q, '92
	†KM48C2100J	2M x 8	60/70/80	CMOS	Fast Page	28 Pin SOJ	3Q, '92
	†KM416C1000J	1M x 16	70/80/100	CMOS	Fast Page	42 Pin SOJ	4Q, '92
	†KM416C1200J	1M x 16	70/80/100	CMOS	Fast Page	42 Pin SOJ	4Q, '92

*: New Product †: Preliminary Product

2.2 Dynamic RAM Module

Based Component	Part Number	Organization	Speed(ns)	Feature	Package	PCB height(In)	Remark
1M DRAM Base	KMM58256CN	256K x 8	60/70/80	Fast Page	S, 30 Pin SIMM	0.65	Now
	KMM59256CN	256K x 9	70/80	Fast Page	S, 30 Pin SIMM	0.65	Now
	KMM581000C	1M x 8	60/70/80	Fast Page	S, 30 Pin SIMM	0.805	Now
	KMM591000C	1M x 9	60/70/80	Fast Page	S, 30 Pin SIMM	0.805	Now
	KMM536256C/CG	256K x 36	70/80	Fast Page	S, 72 Pin SIMM	1.0	Now
	KMM532512CV/CVG	512K x 32	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	Now
	KMM536512C/CG	512K x 36	70/80	Fast Page	D, 72 Pin SIMM	1.0	Now
	KMM540512C/CG/CM	512K x 40	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	Now
4M DRAM Base	KMM581000AN	1M x 8	70/80/100	Fast Page	S, 30 Pin SIMM	0.65	Now
	KMM581020AN	1M x 8	70/80/100	Fast Page	S, 30 Pin SIMM	0.65	Now
	*KMM581000BN	1M x 8	60/70/80	Fast Page	S, 30 Pin SIMM	0.65	'92. 3Q
	KMM591000AN	1M x 9	70/80/100	Fast Page	S, 30 Pin SIMM	0.65	Now
	KMM591020AN	1M x 9	70/80/100	Fast Page	S, 30 Pin SIMM	0.65	Now
	*KMM591000BN	1M x 9	60/70/80	Fast Page	S, 30 Pin SIMM	0.65	'92. 3Q
	KMM584000A	4M x 8	70/80/100	Fast Page	S, 30 Pin SIMM	0.805	Now
	KMM584020A	4M x 8	70/80/100	Fast Page	S, 30 Pin SIMM	0.805	Now
	*KMM584000B	4M x 8	60/70/80	Fast Page	S, 30 Pin SIMM	0.805	'92. 3Q
	KMM594000A	4M x 9	70/80/100	Fast Page	S, 30 Pin SIMM	0.805	Now
	KMM594020A	4M x 9	70/80/100	Fast Page	S, 30 Pin SIMM	0.805	Now
	*KMM594000B	4M x 9	60/70/80	Fast Page	S, 30 Pin SIMM	0.805	'92. 3Q
	KMM5321000AV/AVG	1M x 32	70/80/100	Fast Page	S, 72 Pin SIMM	0.855	Now
	*KMM5321000BV/BVG	1M x 32	60/70/80	Fast Page	S, 72 Pin SIMM	0.855	Now
	KMM5361000A/AG	1M x 36	70/80/100	Fast Page	D, 72 Pin SIMM	1.0	Now
	KMM5361000A1/A1G	1M x 36	70/80/100	Fast Page	S, 72 Pin SIMM	1.0	Now
	*KMM5361000B/BG	1M x 36	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	'92. 3Q
	*KMM5361000B1/B1G	1M x 36	60/70/80	Fast Page	S, 72 Pin SIMM	1.0	'92. 3Q
	KMM5322000AV/AVG	2M x 32	70/80/100	Fast Page	D, 72 Pin SIMM	1.0	Now
	*KMM5322000BV/BVG	2M x 32	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	'92. 3Q
	KMM5362000A/AG	2M x 36	70/80/100	Fast Page	D, 72 Pin SIMM	1.25	Now
	*KMM5362000A1/A1G	2M x 36	70/80/100	Fast Page	D, 72 Pin SIMM	1.0	Now
	*KMM5362000B/BG	2M x 36	60/70/80	Fast Page	D, 72 Pin SIMM	1.25	'92. 3Q
	*KMM5362000B1/B1G	2M x 36	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	'92. 3Q
	KMM5401000A/AG/AM	1M x 40	70/80/100	Fast Page	S, 72 Pin SIMM	1.0	Now
	*KMM5401000B/BG/BM	1M x 40	60/70/80	Fast Page	S, 72 Pin SIMM	1.0	'92. 3Q
	KMM5402000A/AG/AM	2M x 40	70/80/100	Fast Page	D, 72 Pin SIMM	1.0	Now
	*KMM5402000B/BG/BM	2M x 40	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	'92. 3Q

2.2 Dynamic RAM Module (Continued)

Based Component	Part Number	Organization	Speed(ns)	Feature	Package	PCB height(In)	Remark
4M B/W Wide DRAM Base	*KMM536256W/WG	256K x 36	70/80/100	Fast Page	S, 72 Pin SIMM	0.65	Now
	*KMM532512W3/W3G	512K x 32	70/80/100	Fast Page	S, 72 Pin SIMM	1.0	Now
	*KMM536512W3/W3G	512K x 36	70/80/100	Fast Page	S, 72 Pin SIMM	1.0	Now
16M DRAM Base	*KMM584100N	4M x 8	60/70/80	Fast Page	S, 30 Pin SIMM	0.65	Now
	*KMM594100N	4M x 9	60/70/80	Fast Page	S, 30 Pin SIMM	0.65	Now
	*KMM5816000/T	16M x 8	60/70/80	Fast Page	D, 30 Pin SIMM	0.8	Now
	*KMM5816100/T	16M x 8	60/70/80	Fast Page	D, 30 Pin SIMM	0.8	Now
	*KMM5916000/T	16M x 9	60/70/80	Fast Page	D, 30 Pin SIMM	0.8	Now
	*KMM5916100/T	16M x 9	60/70/80	Fast Page	D, 30 Pin SIMM	0.8	Now
	*KMM5324100V/VG/VP	4M x 32	60/70/80	Fast Page	S, 72 Pin SIMM	1.0	Now
	*KMM5364100/G	4M x 36	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	Now
	*KMM5364000H/HG	4M x 36	60/70/80	Fast Page	S, 72 Pin SIMM	1.25	Now
	*KMM5364100H/HG	4M x 36	60/70/80	Fast Page	S, 72 Pin SIMM	1.25	Now
	*KMM5328100V/VG/VP	8M x 32	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	Now
	*KMM5368100/G	8M x 36	60/70/80	Fast Page	D, 72 Pin SIMM	1.375	Now
	*KMM5368000H/HG	8M x 36	60/70/80	Fast Page	D, 72 Pin SIMM	1.25	Now
	*KMM5368100H/HG	8M x 36	60/70/80	Fast Page	D, 72 Pin SIMM	1.25	Now
	*KMM5404000/G	4M x 40	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	Now
	*KMM5404100/G	4M x 40	60/70/80	Fast Page	D, 72 Pin SIMM	1.0	Now
16M B/W Wide DRAM Base	††KMM5321000W/WG	1M x 32	70/80/100	Fast Page	S, 72 Pin SIMM	0.65	'92. 4Q
	††KMM5322000W/WG	2M x 32	70/80/100	Fast Page	D, 72 Pin SIMM	0.8	'92. 4Q

Note: S: Single Side, D: Double Side
*: New Product, ††: Under Development

2.3 Video RAM

Capacity	Part Number	Organization	Speed (ns)	Technology	Features	Packages	Remark
1M bit	KM424C256J	256K x 4	RAM: 80/100/120 SAM: 25/25/35	CMOS	Minimum Feature	28 Pin SOJ	Now
	KM424C256Z	256K x 4	RAM: 80/100/120 SAM: 25/25/35	CMOS	Minimum Feature	28 Pin ZIP	Now
	††KM424C257J	256K x 4	RAM: 60/80/100 SAM: 20/20/25	CMOS	Extended Feature	28 Pin SOJ 44 Pin TSOP II	3Q, '92
	††KM424C257Z	256K x 4	RAM: 60/80/100 SAM: 20/20/25	CMOS	Extended Feature	28 Pin ZIP	3Q, '92
	††KM428C128Z	128K x 8	RAM: 60/80/100 SAM: 20/20/25	CMOS	Extended Feature	40 Pin ZIP 44 Pin TSOP II	4Q, '91
	††KM428C128J	128K x 8	RAM: 60/80/100 SAM: 20/20/25	CMOS	Extended Feature	40 Pin SOJ	4Q, '91
256K bit	KM424C64P	64K x 4	RAM: 100/120 SAM: 25/35	CMOS	Minimum Feature	24 Pin DIP	Now
	KM424C64Z	64K x 4	RAM: 100/120 SAM: 25/35	CMOS	Minimum Feature	24 Pin ZIP	Now

2.4 Static RAM

Slow SRAM Function Guide

Capacity	Part Name	Organization	Speed	Technology	Power Dissipation			Package	Remark
					Active(max.) TTL. DC	Active(max.) TTL. Min	Standby(max.) CMOS		
64K	KM6264BL	8K x 8	70/100/120	CMOS	15mA	55mA	100μA	DIP/SDIP/SOP	Now
	KM6264BL-L	8K x 8	70/100/120	CMOS	15mA	55mA	10μA	DIP/SDIP/SOP	Now
256K	KM62256AL	32K x 8	80/100/120	CMOS	45mA	70mA	100μA	DIP/SOP	Now
	KM62256AL-L	32K x 8	80/100/120	CMOS	45mA	70mA	50μA	DIP/SOP	Now
	KM62256BL	32K x 8	70/85/100/120	CMOS	15mA	70mA	100μA	DIP/SDIP/SOP	Now
	KM62256BL-L	32K x 8	70/85/100/120	CMOS	15mA	70mA	20μA	DIP/SDIP/SOP	Now
	*KM62256BLI	32K x 8	70/100	CMOS	20mA	70mA	50μA	DIP/SOP	Now
	*KM62256BL-V	32K x 8	240	CMOS	15mA	70mA	50μA	DIP/SDIP/SOP	Now
512K	*KM68512L	64K x 8	55/70/85/100	CMOS	15mA	70mA	100μA	SOP/TSOP	3Q.'92
	*KM68512L-L	64K x 8	55/70/85/100	CMOS	15mA	70mA	20μA	SOP/TSOP	3Q.'92
1M	KM681000L	128K x 8	70/85/100/120	CMOS	25mA	70mA	100μA	DIP/SOP	Now
	KM681000L-L	128K x 8	70/85/100/120	CMOS	25mA	70mA	20μA	DIP/SOP	Now
	*KM681000AL	128K x 8	70/85/100/120	CMOS	15mA	70mA	100μA	DIP/SOP/TSOP	Now
	*KM681000AL-L	128K x 8	70/85/100/120	CMOS	15mA	70mA	20μA	DIP/SOP/TOP	Now
	*KM681000ALI	128K x 8	70/100	CMOS	20mA	70mA	100μA	DIP/SOP	Now
	*KM681000ALI-L	128K x 8	70/100	CMOS	20mA	70mA	50μA	DIP/SOP	Now
	*KM681000AL-V	128K x 8	240	CMOS	15mA	70mA	50μA	DIP/SOP/TSOP	Now
4M	†KM684000L	512K x 8	55/70/85/100	CMOS	25mA	70A	100μA	DIP/SOP/TSOP	3Q.'92
	†KM684000L-L	512K x 8	55/70/85/100	CMOS	25mA	70mA	20μA	DIP/SOP/TSOP	3Q.'92

*: New Product †: Preliminary ††: Under Development

Pseudo SRAM Function Guide

Capacity	Part Name	Organization	Speed	Technology	Power Dissipation		Package	Remark
					Active(max.) TTL. Min	Standby(max.) CMOS		
1M	KM658128	128K x 8	80/100/120	CMOS	70mA	2mA	DIP/SDIP/SOP	Now
	KM658128L	128K x 8	80/100/120	CMOS	70mA	200μA	DIP/SDIP/SOP	Now
	KM658128L-L	128K x 8	80/100/120	CMOS	70mA	100μA	DIP/SDIP/SOP	Now
	KM658128LD	128K x 8	80/100/120	CMOS	70mA	200μA	DIP/SDIP/SOP	Now
	KM658128LD-L	128K x 8	80/100/120	CMOS	70mA	100μA	DIP/SDIP/SOP	Now
4M	*KM658512	512K x 8	80/100/120	CMOS	75mA	1mA	DIP/SOP/TSOP	3Q.'92
	*KM658128L	512K x 8	80/100/120	CMOS	75mA	200μA	DIP/SOP/TSOP	3Q.'92
	*KM658128L-L	512K x 8	80/100/120	CMOS	75mA	100μA	DIP/SOP/TSOP	3Q.'92

*: New Product †: Preliminary ††: Under Development

High Speed & Ultra High Speed SRAM

Capacity	Part Name	Organization	Speed (ns)	Technology	Power Dissipation		Package	Remark
					Active Max(mA)	Standby Max(mA)		
64K	KM6465A	16K × 4	25/35/45	CMOS	100	2	22SDIP	Now
	KM6465AL	16K × 4	25/35/45	CMOS	100	0.1	22SDIP	Now
	*KM6465B	16K × 4	12/15/20/25	CMOS	140	1	22SDIP	Now
	KM6465BL	16K × 4	12/15/20/25	CMOS	140	0.1	22DIP	Now
	KM6466A	16K × 4	25/35/45	CMOS	120	2	22SDIP/SOJ	Now
	KM6466AL	16K × 4	25/35/45	CMOS	120	0.1	22SDIP/SOJ	Now
	*KM6466B	16K × 4	12/15/20/25	CMOS	140	1	24SDIP/SOJ	Now
	KM6466BL	16K × 4	12/15/20/25	CMOS	140	0.1	24DIP/SOJ	Now
	*KM6865B	8K × 8	12/15/20/25	CMOS	140	1	28SDIP/SOJ	Now
	KM6865BL	8K × 8	12/15/20/25	CMOS	140	0.1	28DIP/SOJ	Now
256K	KM61257A	256K × 1	25/35/45	CMOS	100	2	24SDIP/SOJ	Now
	KM61257AL	256K × 1	25/35/45	CMOS	100	0.1	24SDIP/SOJ	Now
	KM64257A	64K × 4	25/35/45	CMOS	100	2	24SDIP/SOJ	Now
	KM64257AL	64K × 4	25/35/45	CMOS	100	0.1	24SDIP/SOJ	Now
	†KM64258B	64K × 4	15/20/25	CMOS	140	2	28SDIP/SOJ	Now
	†KM64B258A	64K × 4	8/10/12	BiCMOS	185	20	28SOJ	2Q '92
	*KM64259B	64K × 4	15/20/25	CMOS	140	2	28SDIP/SOJ	Now
	*KM64260B	64K × 4	20/25	CMOS	140	2	28SDIP/SOJ	Now
	*KM68257B	32K × 8	15/20/25	CMOS	150	2	28SDIP/SOJ	Now
	*KM68257BL	32K × 8	15/20/25	CMOS	130	0.1	28SDIP/SOJ	Now
	†KM68B257A	32K × 8	8/10/12	BiCMOS	185	20	28SOJ	2Q '92
	KM69B257A	32K × 9	8/10/12	BiCMOS	185	20	28SOJ	2Q '92
1M	*KM611001	1M × 1	20/25/35	CMOS	140	2	28SDIP/SOJ	Now
	*KM641001	256K × 4	20/25/35	CMOS	150	2	28SDIP/SOJ	Now
	*KM641005	256K × 4	20/25/35	CMOS	150	2	32SDIP/SOJ	Now
	†KM64B1001	256K × 4	12/15	BiCMOS	170	20	28SDIP/SOJ	3Q '92
	KM64B1002	256K × 4	10/12	BiCMOS	160	20	28SOJ	4Q '92
	KM64B1003	256K × 4	10/12	BiCMOS	160	20	28SOJ	4Q '92
	*KM681001	128K × 8	20/25/35	CMOS	160	2	32SDIP/SOJ	Now
	†KM68B1001	128K × 8	12/15	BiCMOS	180	20	32SDIP/SOJ	3Q '92
	KM68B1002	512K × 8	10/12	BiCMOS	180	20	28SOJ	4Q '92

Synchronous SRAM

Capacity	Part Name	Organization	Speed (ns)	Technology	Power Dissipation		Package	Remark
					Active Max(mA)	Standby Max(mA)		
1M	KM741006	256K × 4	12	CMOS	190	80	36SOJ	4Q '92

Synchronous

Capacity	Part Name	Organization	Speed (ns)	Technology	Power Dissipation		Package	Remark
					Active Max(mA)	Standby Max(mA)		
1M	††KM741006	256K × 4	10/12	CMOS	170	3	32SOJ	4Q '92
	††KM781006	128K × 8	10/12	CMOS	170	3	36SOJ	4Q '92
	††KM791006	128K × 9	10/12	CMOS	170	3	36SOJ	4Q '92

*: New Product †: Preliminary Product ††: Under Development

2.5 EEPROM

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remarks
256 bit	KM93C06/G/GD/I	16 x 16	1MHz	CMOS	Ext.-timed	8DIP/8SOP	Now
	KM93C07/G/GD/I	16 x 16	1MHz	CMOS	Self-timed	8DIP/8SOP	Now
1K bit	KM93C46/G/GD/I	64 x 16	1MHz	CMOS	Self-timed	8DIP/8SOP	Now
	KM93C46V/VG/VGD/I	64 x 16	250KHz	CMOS	3.0V Operation	8DIP/8SOP	Now
2K bit	KM93C56/G/GD/I	128 x 16	1MHz	CMOS	Auto Erase, Self-timed	8DIP/8SOP	3Q '92
	KM93CS56/G/GD/I	128 x 16	1MHz	CMOS	Data Protect	8DIP/8SOP	3Q '92
	KM93C57/G/GD/I	256 x 8/128 x 16	1MHz	CMOS	Select Organization	8DIP/8SOP	3Q '92
	KM93C56V/VG/VGD/I	128 x 16	1MHz	CMOS	2.0V Operation	8DIP/8SOP	4Q '92
	KM93C57V/VG/VGD/I	256 x 8/128 x 16	1MHz	CMOS	2.0V Operation	8DIP/8SOP	4Q '92
4K bit	KM93C66/G/GD/I	256 x 16	1MHz	CMOS	Auto Erase, Self-timed	8DIP/8SOP	3Q '92
	KM93CS66/G/GD/I	256 x 16	1MHz	CMOS	Data Protect	8DIP/8SOP	3Q '92
	KM93C67/G/GD/I	512 x 8/128 x 16	1MHz	CMOS	Select Organization	8DIP/8SOP	3Q '92
	KM93C66V/VG/VGD/1	256 x 16	1MHz	CMOS	2.0V Operation	8DIP/8SOP	4Q '92
	KM93C67V/VG/VGD/I	512 x 8/128 x 16	1MHz	CMOS	2.0V Operation	8DIP/8SOP	4Q '92
16K bit	KM28C16/J	2K x 8	150/200/250	CMOS	32B Page Mode, D-P	24DIP/32PLCC	Now
	KM28C16I/JI	2K x 8	200/250	CMOS	Industrial	24DIP/32PLCC	Now
	KM28C17/J	2K x 8	150/200/250	CMOS	32B Page Mode, D-P, R/B	28DIP/32PLCC	Now
	KM28C17I/JI	2K x 8	200/250	CMOS	Industrial	28DIP/32PLCC	Now
64K bit	KM28C64A/AJ	8K x 8	120/150/200	CMOS	64B Page Mode, D-P, T-B	28DIP/32PLCC	Now
	KM28C64AI/AJI	8K x 8	120/150/200	CMOS	Industrial	28DIP/32PLCC	Now
	KM28C65A/AJ	8K x 8	120/150/200	CMOS	64B Page Mode, D-P, R/B	28DIP/32PLCC	Now
	KM28C65AI/AJI	8K x 8	120/150/200	CMOS	Industrial	28DIP/32PLCC	Now
256K bit	KM28C256/J	32K x 8	150/200/250	CMOS	64B Page Mode, D-P, T-B	28DIP/32PLCC	Now
	KM28C256I/JI	32K x 8	150/200/250	CMOS	Industrial	28DIP/32PLCC	Now
	KM28C256A/AJ	32K x 8	120/150/200	CMOS	64B Page Mode, D-P, T-B	28DIP/32PLCC	4Q '92
	KM28C256AI/AJI	32K x 8	120/150/200	CMOS	Industrial	28DIP/32PLCC	4Q '92
1M bit	KM29C010/J/T	128K x 8	120/150/200	CMOS	128B Page Mode, D-P, T-B	32DIP/32PLCC	4Q '92
	KM29C010I/JI	128K x 8	120/150/200	CMOS	Industrial	32TSOP	4Q '92

*: D-P: Data-Polling, R/B: Ready/Busy, T-B: Toggle Bit

2.6 Mask ROM

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
256K bit	KM23C256(G)	32K x 8	120/150/200	CMOS	Programmable CE & OE	28DIP(32SOP)	Now
512K bit	KM23C512(G)	64K x 8	120/150/200	CMOS	Programmable CE & OE	28DIP(32SOP)	Now
1M bit	KM23C1000	128K x 8	120/150/200	CMOS	Programmable CE	28DIP	Now
	KM23C1001	128K x 8	120/150/200	CMOS	Programmable OE	28DIP	Now
	KM23C1010(G)	128K x 8	120/150/200	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	*KM23C1010J	128K x 8	120/150/200	CMOS	Programmable CE & OE	32PLCC	Now
	KM23C1011(G)	128K x 8	120/150/200	CMOS	Programmable OE	32DIP(32SOP)	Now
2M bit	KM23C2000(G)	256K x 8	150/200/250	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	†KM23C2000H(G)	256K x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	3Q '92
	KM23C2001	256K x 8	150/200/250	CMOS	Programmable OE	32DIP	Now
	†KM23C2001H	256K x 8	100/120/150	CMOS	Programmable OE	32DIP	3Q '92
	KM23C2100(FP)	256K x 8/ 128K x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44QFP)	Now
	†KM23C2100H(FP)	256K x 8/ 128K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44QFP)	3Q '92
4M bit	KM23C4000A(G)	512K x 8	150/200/250	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	*KM23C4000B(G)	512K x 8	120/150/200	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	KM23C4000H(G)	512K x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	KM23C4001A(G)	512K x 8	150/200/250	CMOS	Programmable OE	32DIP(32SOP)	Now
	*KM23C4001B(G)	512K x 8	120/150/200	CMOS	Programmable OE	32DIP(32SOP)	Now
	KM23C4001H(G)	512K x 8	100/120/150	CMOS	Programmable OE	32DIP(32SOP)	Now
	*KM23C4100BG	512K x 8/ 256K x 16	120/150/200	CMOS	Programmable CE & OE Word/Byte Mode	40SOP	Now
	KM23C4100A(FP)	512K x 8/ 256K x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44QFP)	Now
	†KM23C4100B(FP)	512K x 8/ 256K x x 16	120/150/200	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44QFP)	2Q '92
	KM23C4100H(FP)	512K x 8/ 256K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44QFP)	Now
	KM23C4200B	512K x 8/ 256K x 16	120/150/200	CMOS	Programmable CE & OE Word/Byte Mode	40DIP	Now

Mask ROM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Packages	Remark
8M bit	KM23C8000A(G)	1M x 8	150/200/250	CMOS	Programmable CE & OE	32DIP(32SOP)	Now
	†KM23C8000H(G)	1M x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	3Q '92
	KM23C8001A	1M x 8	150/200/250	CMOS	Programmable OE	32DIP	Now
	†KM23C8001H	1M x 8	100/120/150	CMOS	Programmable OE	32DIP	3Q '92
	KM23C8100A(G)	1M x 8/ 512K x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44SOP)	Now
	KM23C8100AFP1	1M x 8/ 512K x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	44QFP	Now
	KM23C8100AFP2	1M x 8/ 512K x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	64QFP	Now
	†KM23C8100H(G)	1M x 8/ 512K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(44SOP)	3Q '92
	†KM23C8100HFP1	1M x 8/ 512K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	44QFP	3Q '92
	†KM23C8100HFP2	1M x 8/ 512K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	64QFP	3Q '92
16M bit	KM23C16000(G)	2M x 8/ 1M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	42DIP(44SOP)	Now
	*KM23C16000FP	2M x 8/ 1M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	64QFP	Now
	†KM23C16100(G)	2M x 8/ 1M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	42DIP(44SOP)	3Q '92
	†KM23C16100FP	2M x 8/ 1M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	64QFP	3Q '92
32M bit	†KM23C32000	2M x 16	150/200/250	CMOS	Programmable CE & OE	42DIP	4Q '92
	†KM23C32000G	4M x 8/ 2M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	44SOP	4Q '92
	†KM23C32000FP	4M x 8/ 2M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	64QFP	4Q '92
	†KM23C32100	2M x 16	150/200/250	CMOS	Programmable CE & OE	42DIP	4Q '92
	†KM23C32100G	4M x 8/ 2M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	44SOP	4Q '92
	†KM23C32100FP	4M x 8/ 2M x 16	150/200/250	CMOS	Programmable CE & OE Word/Byte Mode	64QFP	4Q '92

*: New Product †: Under Development

2.7 FIFO

Capacity	Part Number	Organization	Speed	Technology	Features	Package	Remark
Standard FIFO	KM75C01AP	512 x 9	15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.6")	Now
	KM75C01AN	512 x 9	15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.3")	Now
	KM75C01AJ	512 x 9	15/20/25/ 35/50/80	CMOS	Parallel FIFO	32PLCC	Now
	KM75C02AP	1K x 9	12/15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.6")	Now
	KM75C02AN	1K x 9	12/15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.3")	Now
	KM75C02AJ	1K x 9	12/15/20/25/ 35/50/80	CMOS	Parallel FIFO	32PLCC	Now
	KM75C03AP	2K x 9	12/15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.6")	Now
	KM75C03AN	2K x 9	12/15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.3")	Now
	KM75C03AJ	2K x 9	12/15/20/25/ 35/50/80	CMOS	Parallel FIFO	32PLCC	Now
	KM75C04AP	4K x 9	15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.6")	4Q '92
	KM75C04AN	4K x 9	15/20/25/ 35/50/80	CMOS	Parallel FIFO	28PDIP (0.3")	4Q '92
	KM75C04AJ	4K x 9	15/20/25/ 35/50/80	CMOS	Parallel FIFO	32PLCC	4Q '92

*: New Product
†: Preliminary Product

3. CROSS REFERENCE GUIDE

3.1 DRAM

Density	Org.	Mode	Samsung	Toshiba	Hitachi	Fujitsu	NEC	Oki
256K	×1	F. Page	KM41C256	TC51256	HM51256	MB81256	μPD41256	MSM51C256
		Nibble	KM41C257	TC51257	—	MB81257	—	MSM41257
		S. Column	KM41C258	TC51258	HM51258	MB81258	—	—
	×4	F. Page	KM41C464	TC51464	HM50464	MB81464	μPD41464	MSM41464
		S. Column	KM41C466	TC51466	—	MB81466	—	—
1M	×1	F. Page	KM41C1000	TC511000	HM511000	MB81C1000	μP0421000	MSM511000
		Nibble	KM41C1001	TC511001	HM511001	MB81C1001	μP0421001	MSM511001
		S. Column	KM41C1002	TC511002	HM511002	MB81C1002	μP0421002	MSM511002
	×4	F. Page	KM44C256	TC514256	HM514256	MB81C4256	μP0424256	MSM514256
		S. Column	KM44C258	TC514258	HM514258	MB81C4258	μP0424258	MSM514258
4M	×1	F. Page	KM41C4000	TC514100	HM514100	MB814100	μPD424100	MSM514100
		Nibble	KM41C4001	TC514101	HM514101	MB814101	μPD424101	MSM514101
		S. Column	KM41C4002	TC514102	HM514102	MB814102	μPD424102	MSM514102
	×4	F. Page	KM44C1000	TC514400	HM514400	MB814400	μPD424400	MSM514400
		S. Column	KM44C1002	TC514402	HM514402	MB814402	μPD424402	MSM514402
	×8	F. Page	KM48C512	TC514800A	HM514800	MB814800A	μPD424800	—
	×9	F. Page	KM49C512	TC514900A	HM514900	—	μPD424900	—
	×16	F. Page	KM416C256	TC514170B	HM514170	MB814170A	μPD424170	—
	×18	F. Page	KM418C256	TC514280B	HM514280	—	μPD424280	—
16M	×1	F. Page	KM41C16000	TC5116100	HM5116100	MB8116100	μPD4216100	—
	×4	F. Page	KM44C4000	TC5116400	HM5116400	MB8116400	μPD4216400	—

3.2 DYNAMIC RAM MODULE

Density	Organization	Samsung	Toshiba	Hitachi	NEC
2M bit	256K × 8(2C)	KMM58256CN	THM82500	HB56025608	—
2.3M bit	256K × 9(3C)	KMM59256CN	THM92500	HB56025609	—
8M bit	1M × 8	KMM581000	THM81000	HB56A18	MC-421000A8
9M bit	1M × 9	KMM591000	THM91000	HB56A19	MC-421000A9
8M bit	256K × 32	KMM532256	THM322500	HB56025632	—
9M bit	256K × 36	KMM536256	—	—	—
16M bit	512K × 32	KMM532512	THM325120	HB56051232	—
18M bit	512K × 36	KMM536512	—	HB56051236	—
20M bit	512K × 40	KMM540512	—	—	—
8M bit	1M × 8(2C)	KMM581000AN	—	HB56G18	—
9M bit	1M × 9(3C)	KMM591000AN	—	HB56G19	—
32M bit	4M × 8	KMM584000	THM84000	HB56A48	MC-424100A8
36M bit	4M × 9	KMM594000	THM94000	HB56A49	MC-424100A9
32M bit	1M × 32	KMM5321000	THM321000	HB56D132	—
36M bit	1M × 36	KMM5361000	THM5361020	HB56D136	MC-421000A36
64M bit	2M × 32	KMM5322000	THM322020	HB56D232	—
72M bit	2M × 36	KMM5362000	THM362020	HB56D236	MC-422000A36
40M bit	1M × 40	KMM5401000	THM401020	HB56A140	—
80M bit	2M × 40	KMM5402000	THM402020	—	—

3.3 VIDEO RAM

Density	Feature	Org.	Samsung	Toshiba	NEC	Hitachi	TI	Mitsubishi
256K	Minimum Feature	64K × 4	KM424C64		μPD41264 μPD42264	HM53461	TMS4461	M5M4C264
1M	Minimum Feature	256K × 4	KM424C256	TC524256 TC524256A/B	μPD42273	HM534251	TM544C250	
	Extended Feature	256K × 4	KM424C257	TC524258A/B TC524259B	μPD42274	HM534253 HM534252	TMS44C251	M5M442256
	Extended Feature	128K × 8	KM428C128	TC528126A/B TC528128A/B	μPD42275	HM538121 HM538122 HM538123	TMS48C121	M5M482128

3.4 Static RAM

Slow SRAM Cross Reference

Density	Org.	SAMSUNG	HITACHI	SONY	TOSHIBA	MITSUBISHI	NEC
64K	8K × 8	KM6264BL/BL-L	HM6264AL/AL-L	CXK5864BL	TC5565AL	M5M5165	μPD4364L/L-L
256K	32K × 8	KM62256AL/AL-L KM62256BL/BL-L	HM62256L/L-L	CXK58257L/L-L	TC55257L	M5M5265	μPD43256AL
512K	64K × 8	KM68512L/L-L	—	—	—	—	—
1M	128K × 8	KM681000L/L-L KM681000AL/AL-L	HM628128L/L-L	CXK581000L CXK581001L	TC551001L	M5M51000	μPD431000L
4M	512K × 8	KM684000L/L-L	HM628512	CXK584000L	TC554001L	M5M5408	μPD434000

Pseudo SRAM Cross Reference

Density	Org.	SAMSUNG	HITACHI	TOSHIBA	NEC	OKI	MOTOROLA
1M	128K × 8	KM658128/L/L-L	HM658128	TC518128A	μPD428128	MSM548128	MCM518128
4M	512K × 8	KM658512L/L-L	HM658512	TC518512	μPD428512	MSM548512	—

Fast SRAM

Density	Organization	Samsung	Hitachi	Cypress	Fujitsu	Micron	IDT	Motorola	Toshiba	Sony
64K	16K x 4	KM6465A/AL KM6465B/BL	HM6288/L	CY7C164 CY7C164A	MB81C74	MT5C6404	IDT7188	MCM6288	TC55416	CXK5464
	16K x 4 (With $\overline{OE}$)	KM6466A/AL KM6466B/BL	HM6289/L	CY7C166 CY7C166A	MB81C75	MT5C6405	IDT7189	MCM6290	TC55417	CXK5465
	8K x 8	KM6865B/BL		CY7C186A	MB81C78	MT5C6308	IDT7164	MCM6264	TC5588	CXK5863
256K	256K x 1	KM61257A/AL	HM6207H/L	CY7C197	MB81C81A	MT5C2561	IDT71257	MCM6207		CXK51256
	64K x 4	KM64257A/AL	HM6208H/L	CY7C194	MB81C84	MT5C2564	IDT71258	MCM6208	TC55464	CXK54256
	64K x 4 (With $\overline{OE}$)	KM64258B		CY7C196		MT5C2565	IDT61298	MCM6209	TC55465	
	64K x 4 (Sep. I/O, H-Z)	KM64259B		CY7C191	MB81C86		IDT71282			
	64K x 4 (Sep. I/O, L-Z)	KM64260B		CY7C192			IDT71281			
	32K x 8	KM68257B/BL	HM63832UH/L	CY7C199		MT5C2568	IDT71256	MCM6206	TC55328	CXK58258B
512K	32K x 16	KM616513							TC551632	
1M	1M x 1	KM611001	HM61100A/L	CY7C107		MT5C1001	IDT71027			
	256K x 4	KM641001	HM624256A/L	CY7C106		MT5C1005	IDT71028	MCM6229W		
	256K x 4 (Sep. I/O)	KM641005	HM624257A/L	CY7C101						CXK541000
	128K x 8	KM681001		CY7C108		MT5C1008	IDT71024	MCM6226W		CXK581020

BiCMOS SRAM

Density	Organization	Samsung	Hitachi	Cypress	Toshiba	Fijitsu	IDT	Motorola
256K	64K x 4(With OE)	KM64B258A	HM6709A	CY7B195	TC55B465		IDT61B298	MCM6709/A
	32K x 8	KM68B257A	HM628325H	CY7B199	TC55B328		IDT71B256	MCM6706/A
288K	32K x 9	KM69B257A			TC55B329			
1M	256K x 4	KM64B1001			TC55B4256	MB82B005	IDT71B028	
	256K x 4 (Center Power)	KM64B1002			TC55B4256			MCM6728
	256K x 4 (Center Power, with OE)	KM64B1003			TC55B4257			MCM6729
	128K x 8	KM68B1001			TC55B8128		IDT71B024	
	128K x 8 (Center Power)	KM68B1002			TC55B8128			MCM6726

3.5 EEPROM

Serial I/O EEPROM

Density	Samsung	N.S.	Exar	Micro Chip	SGSThomson	Catalyst	Rohm	AsahiKasai
256	KM93C06	NM9306		93C46	ST93C06			AK93C06
	KM93C07	NM9307		ER59256				
1K	KM93C46	NM9346	XRM93C46A	93C46	ST93C46T	CAT93C46A	BR93C46	AK93C46
	KM93CS46	NM93CS46			ST93C46		BR93CS46	
	KM93C46V	NM93C46L						
2K	KM93C56	NM93C56	XRM93C56A				BR93C56A	AK93C57
	KM93C57			93C56	ST93C56	CAT36C102		
	KM93CS56	NM93CS56			ST93CS56			
	KM93C56V	NM93C56L					BR93C56B	
	KM93C57V							
4K	KM93C66	NM93C66	XRM93C66B				BR93C66A	AK93C67
	KM93C67			93C66		CAT35C104		
	KM93CS66	NM93CS66			ST93CS66			
	KM93C66V	NM93C66L					BR93C66B	
	KM93C67V					CAT33T104		

Parallel EEPROM

Density	Samsung	Xicor	Seeq	Exel	Atmel	Hitachi	Oki	Catalyst
16K	KM28C16	X2816B X2816C	DQ2816A DQ5516A	XL2816A	AT28C16		MSM28C16A	CAT28C16A
	KM28C17		DQ2817A DQ5517A	XL2817A	AT28C17			CAT28C17A
64K	KM28C64A	X2864A/B X28C64	DQ28C64	XL2864 XL28C64A	AT28C64	HN58064	MSM28C64A	CAT28C65A
	KM28C65A		DQ28C65 DQ2864	XL2865 XL28C65A		HN58C65/66		CAT28C65A
256K	KM28C256	X28256 X28C256	DQ28C256		AT28C256	HN28C256	MSM28C256	CAT28C256
	KM28C256A	X28256 X28C256	DQ28C256		AT28C256	HN28C256	MSM28C256	CAT28C256
1M	KM29C010				AT29C010			

3.6 Mask ROM Cross Reference Guide-1

Density	Package	Org.	Samsung	NEC	Hitachi	Toshiba	Sharp	Mitsubishi	Fujitsu	Sony
256K	28 DIP	x8	KM23C256		HN623257P HN623257PZ HN623258P		LH23255D LH53259D	M5M23256P	MB83256	
	32 SOP	x8	KM23C256G							
512K	28 DIP	x8	KM23C512			TC53512CP	LH23512D LH53514D LH53515D		MB83512	
	32 DIP	x8	KM23C512G							
1M	28 DIP	x8	KM23C1000	μPD23C1000A	HN62321P HN62321BP HN62331P	TC531000CP	LH231000BD LH531000AD	M5M23C100 M5M231000	MB831000 MB831124	
			KM23C1001	μPD23C1010A	HN62321EP HN62331EP			M5M231001		
	32 DIP	x8	KM23C1010	μPD23C1001E μPD23C1000EA	HN62321AP HN62331AP	TC531001CP	LH231100BD LH530800D LH530900D			
			KM23C1011							
	32 SOP	x8	KM23C1010G		HN62321AF HN62331AF	TC531001CF				
			KM23C1011G							
2M	32 DIP	x8	KM23C2000	μPD23C2001			LH532300D LH532100BD LH532200BD LH532400D		MB832000 MB832001	CXK382001
			KM23C2001							
	32 SOP	x8	KM23C2000G							
	40 DIP	x8/x16	KM23C2100	μPD23C2000 μPD23C2000A	HN62412P HN62422P		LH532000BD LH532500D			
	44 QFP	x8/x16	KM23C2100FP		HN62412FP HN62422FP					

Mask ROM Cross Reference Guide—II

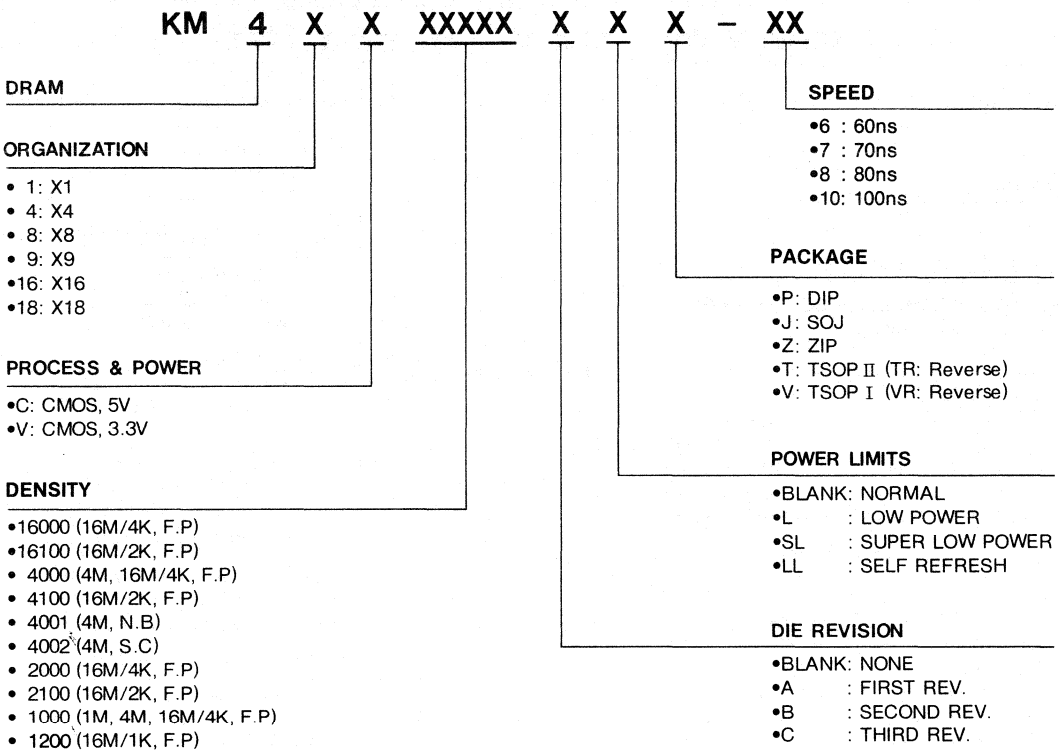
Density	Package	Org.	Samsung	NEC	Hitachi	Toshiba	Sharp	Mitsubishi	Fujitsu	Sony
4M	32 DIP	x8	KM23C4000A	μPD23C4001E	HN62304BP HN62314BP HN62324BP HN62344BP	TC534000P TC534000AP	LH534100BD	M5M23C401AP	MB834000A	CXK384001
			KM23C4001A				LH534200BD LH534300D LH534400D			
	32 SOP	x8	KM23C4000AG	μPD23C4001E	HN62304BF HN62314BF HN62324BF HN62344BF	TC534000F TC534000AF	LH534100BN	M5M23401AFP		
			KM23C4001HG				LH534200BN			
	40 DIP	X8/x16	KM23C4100A	μPD23C4000 μPD23C4000A	HN62404P HN62414P HN62424P HN62444P	TC534200P	LH534000BD LH534500D	M5M23C400AP	MB834100A MB834200A	
	40 SOP	x8/x16	KM23C4100BG			TC534200F				
	44 QFP	x8/x16	KM23C4100AFP		HN62404FP HN62414FP HN62424FP HN62444FP				MB834200A	
8M	32 DIP	x8	KM23C8000A KM23C8001A	μPD23C8001E	HN62308BP		LH538100D LH538200D	M5M23801P	MB838000	CXK388000
	32 SOP	x8	KM23C8000AG		HN62308BF			M5M23801FP		
	42 DIP	x8/x16	KM23C8100A	μPD23C8000	HN62408P	TC538200P	LH538000D	M5M23800P	MB838200	
	44 SOP	x8/x16	KM23C8100AG			TC538200F	LH538000N	M5M23800FP		
	44 QFP	x8/x16	KM23C8100AFP1		HN62408FP					
	64 QFP	x8/x16	KM23C8100AFP2				LH538000M		MB838200	
16M	42 DIP	x8/x16	KM23C16000	μPD23C16000	HN624016P HN624017P	TC5316200P		M5M23160P	MB831620P	
			KM23C16100					M5M23168P		
	44 SOP	x8/x16	KM23C16000G KM23C16100G		HN624017FB	TC5316200F		M5M23160FP M5M23168FP	MB831620PF	
	64 QFP	x8/x16	KM23C16000FP KM23C16100FP				LH5316000M			
32M	42 DIP	x16	KM23C32000							
	44 SOP	x8/x16	KM23C32000G				LH5332000N			
	64 QFP	x8/x16	KM23C32000FP				LH5332000M			

3.7 FIFO

Capacity	Org.	Samsung	AMD	IDT	Sharp	Cypress	TI
Standard FIFO	512 x 9	KM75C01A	Am7201	IDT7201SA/LA	LH5496/D	CY7C420(1)	74ACT7201A
	1K x 9	KM75C02A	Am7202	IDT7202SA/LA	LH5497/D	CY7C424(5)	74ACT7202
	2K x 9	KM75C03A	Am7203	IDT7203S/L	LH5498/DKM7	CY7C428(9)	
	4K x 9	KM75C04A	Am7204	IDT7204S/L	LH5499/D		

4. ORDERING INFORMATION

4.1 DRAM



4.2 DRAM MODULE

MODULE PART NUMBERING SYSTEM

KM M W WW XXXX Y Y Y Y Y Y —ZZ

MEMORY

MODULE

PIN/EDGE CONNECTOR

- •5: DRAM SIMM (EDGE CONNECTOR)
- •4: DRAM SIP (PINS)

ORGANIZATION

- •8 : X8 bits wide
- •9 : X9 bits wide
- •18 : X18 bits wide
- •32 : X32 bits wide
- •33 : X33 bits wide
- •36 : X36 bits wide
- •40 : X40 bits wide
- •144: X144 bits wide

DENSITY & MODE/FEATURE

16000: 16M F. Page, 4K refresh
16100: 16M F. Page, 2K refresh
8000: 8M F. Page, 4K refresh
8100: 8M F. Page, 2K refresh
4000: 4M F. Page, 1K/4K refresh
4001: 4M Nibble
4002: 4M S. Column
4020: 4M F. Page (Low Power)
4040: 4M F. Page (S. Low Power)
4100: 4M F. Page, 1K/2K refresh
1000: 1M F. Page
1001: 1M Nibble
1002: 1M S. Column
1010: 1M F. Page, L. Profile (.505")
1020: 1M F. Page (Low Power)
1040: 1M F. Page (S. Low Power)
1005: 1M Slugger Module
512: 512K Page
514: 512K S. Column
532: 512K Page (Low Power)
256: 256K Page
258: 256K S. Column
276: 256K Page (Low Power)

DIE (COMPONENT) REVISION

- •BLANK: NONE
- •A : FIRST REV.
- •B : SECOND REV.
- •C : THIRD REV.

PACKAGE (COMPONENT) TYPE

- •BLANK: SOJ OR PLCC
- •*T : TSOP

PACKAGE (PCB) REVISION

- •BLANK: NONE
- •1 : FIRST REV.
- •2: SECOND REV.

NUMBER OF COMPONENTS

- •BLANK: MORE THAN 7 CHIPS
- •N : LESS THAN 8 CHIPS
- •W : BYTE-WORD WIDE BASE

× 32 & × 33 ONLY PCB

- •V: × 32 & × 33 ONLY

LEAD FINISH/SPEC CUSTOMER

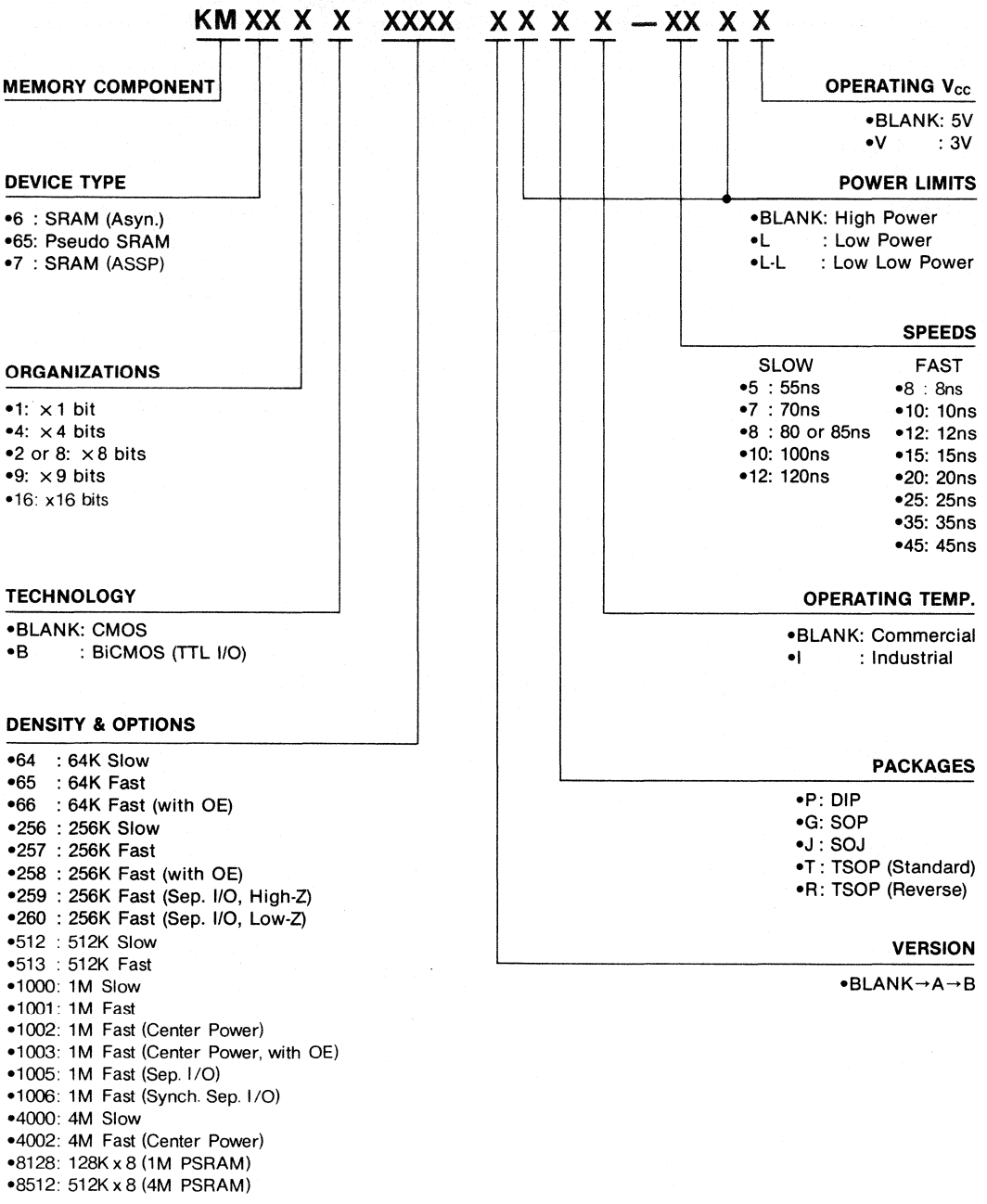
—STD. MODULE
- •BLANK: SOLDER
- •G : GOLD

—CUSTOMER
- •D: DEC
- •P: APPLE
- •H: HP
- •Q: COMPAQ
- •M: IBM

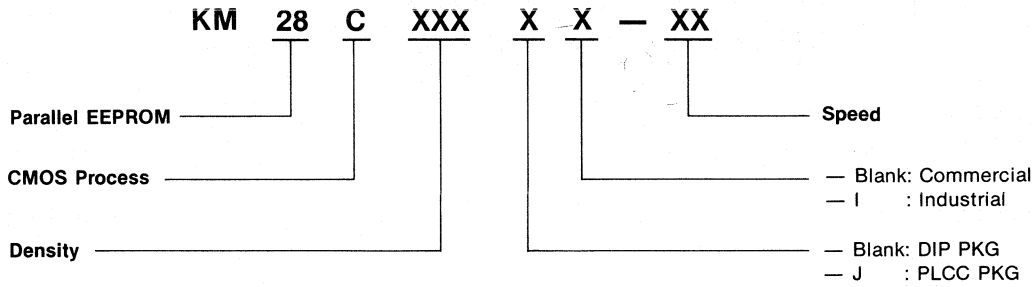
SPEED

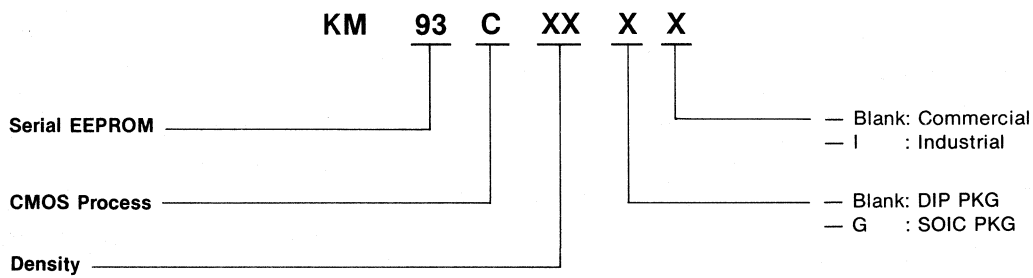
- •5 : 50ns
- •6 : 60ns
- •7 : 70ns
- •8 : 80ns
- •10: 100ns

4.3 SRAM ORDERING INFORMATION

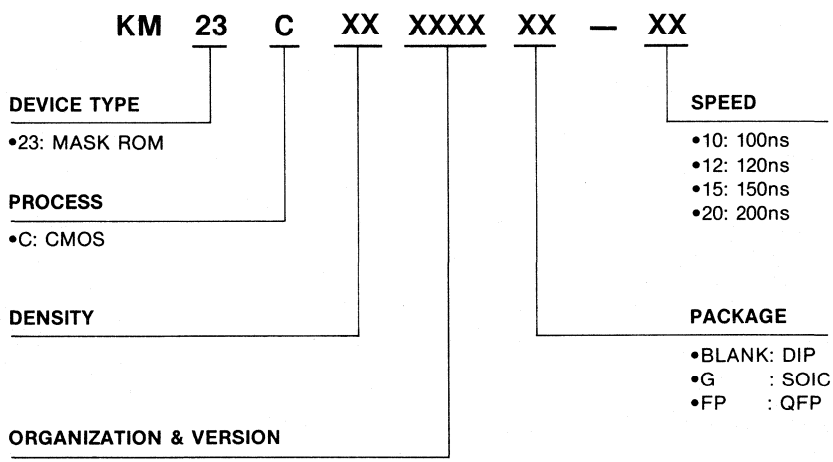


4.4 EEPROM

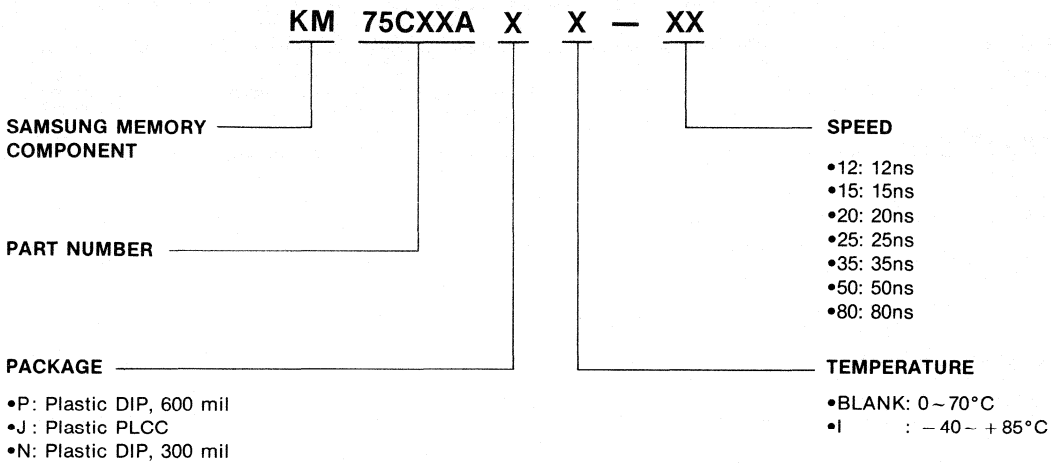




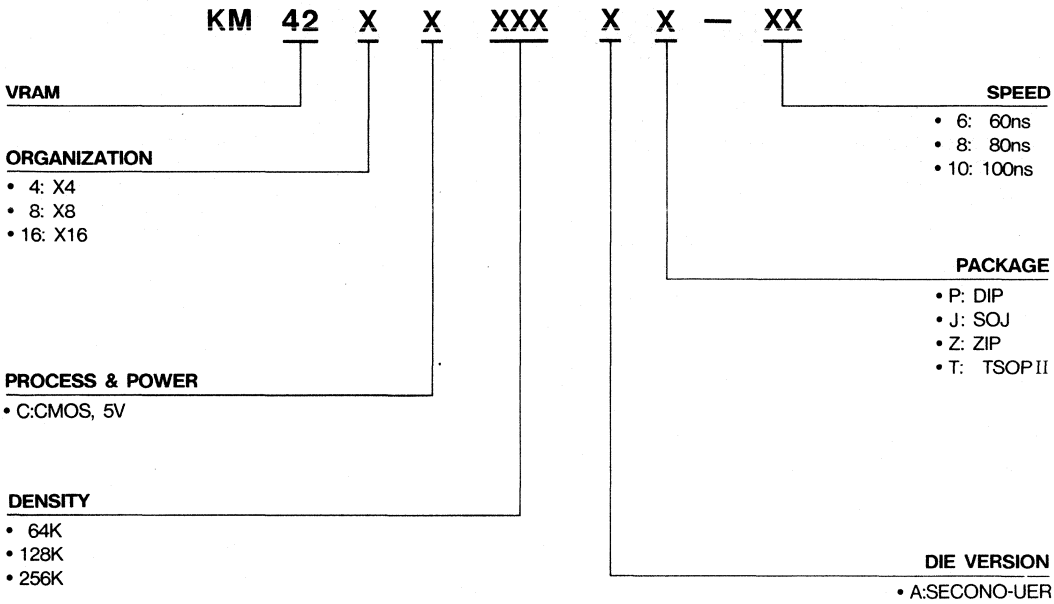
4.5 MASK ROM

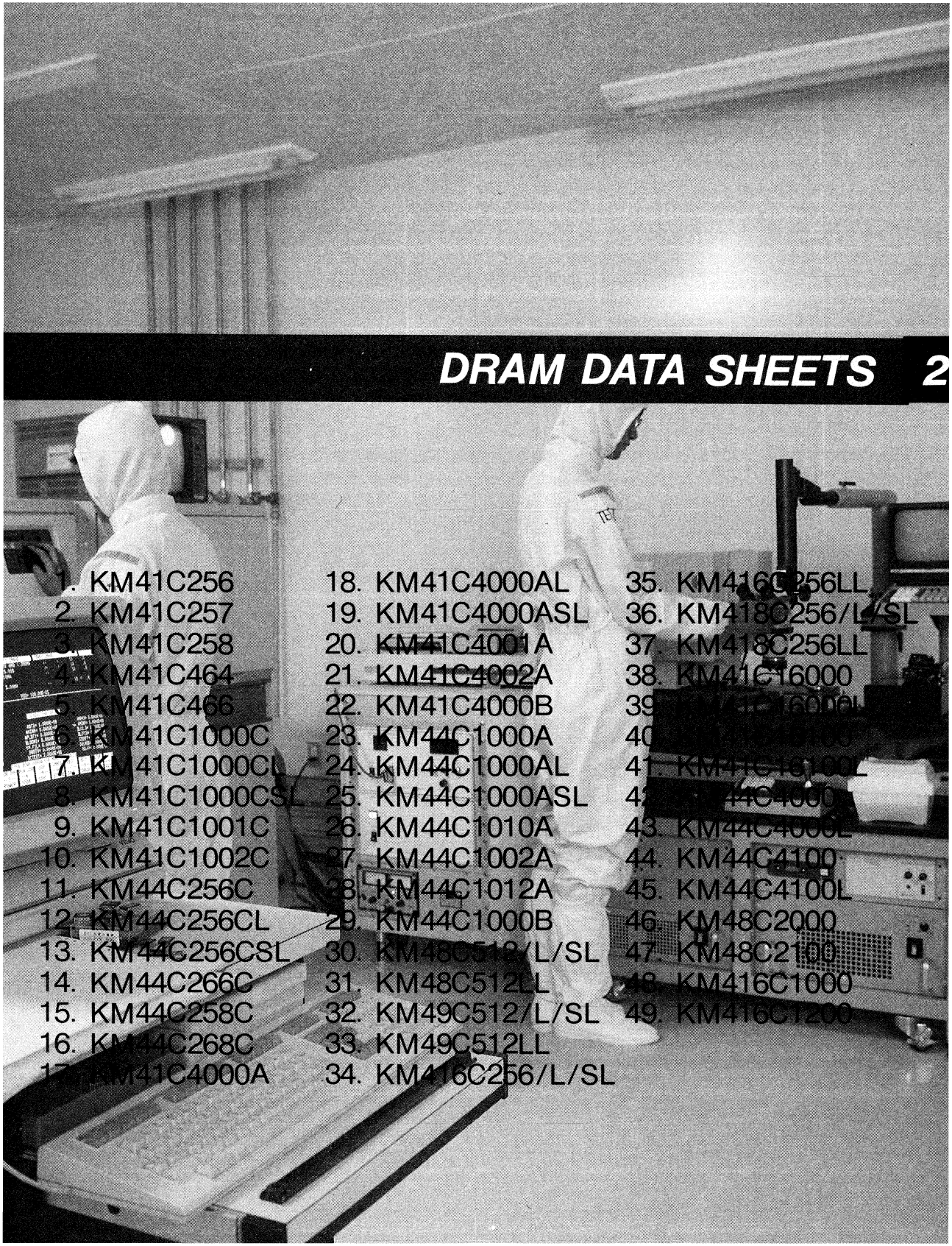


4.6 FIFO


KM 75CXXA X X — XX
SAMSUNG MEMORY COMPONENT
PART NUMBER
PACKAGE
•P: Plastic DIP, 600 mil
•J : Plastic PLCC
•N: Plastic DIP, 300 mil
SPEED
•12: 12ns
•15: 15ns
•20: 20ns
•25: 25ns
•35: 35ns
•50: 50ns
•80: 80ns
TEMPERATURE
•BLANK: 0~70°C
•I : −40~+85°C

4.7 VRAM


KM 42 X X XXX X X — XX
VRAM
ORGANIZATION
• 4: X4
• 8: X8
• 16: X16
PROCESS & POWER
• C:CMOS, 5V
DENSITY
• 64K
• 128K
• 256K
SPEED
• 6: 60ns
• 8: 80ns
• 10: 100ns
PACKAGE
• P: DIP
• J: SOJ
• Z: ZIP
• T: TSOP II
DIE VERSION
• A:SECONO-UER



DRAM DATA SHEETS 2

1. KM41C256
2. KM41C257
3. KM41C258
4. KM41C464
5. KM41C466
6. KM41C1000C
7. KM41C1000CL
8. KM41C1000CSL
9. KM41C1001C
10. KM41C1002C
11. KM44C256C
12. KM44C256CL
13. KM44C256CSL
14. KM44C266C
15. KM44C258C
16. KM44C268C
17. KM41C4000A
18. KM41C4000AL
19. KM41C4000ASL
20. KM41C4001A
21. KM41C4002A
22. KM41C4000B
23. KM44C1000A
24. KM44C1000AL
25. KM44C1000ASL
26. KM44C1010A
27. KM44C1002A
28. KM44C1012A
29. KM44C1000B
30. KM48C512/L/SL
31. KM48C512LL
32. KM49C512/L/SL
33. KM49C512LL
34. KM416C256/L/SL
35. KM416C256LL
36. KM418C256/L/SL
37. KM418C256LL
38. KM41C16000
39. KM41C16000L
40. KM41C16100
41. KM41C16100L
42. KM44C4000
43. KM44C4000L
44. KM44C4100
45. KM44C4100L
46. KM48C2000
47. KM48C2100
48. KM416C1000
49. KM416C1200

256K x 1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C256- 7	70ns	20ns	130ns
KM41C256- 8	80ns	20ns	150ns
KM41C256-10	100ns	25ns	180ns

- **Fast Page Mode capability**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Write**
- **Single +5V ± 10% power supply**
- **256 cycles/4ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic DIP, PLCC or ZIP**

GENERAL DESCRIPTION

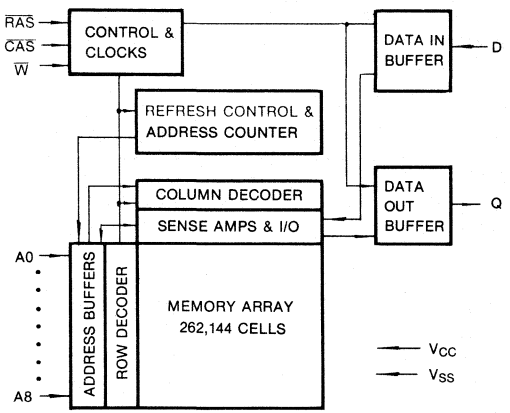
The Samsung KM41C256 is a CMOS high speed 262,144 bit x 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C256 features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and output are fully TTL compatible.

The KM41C256 is fabricated using Samsung's advanced CMOS process.

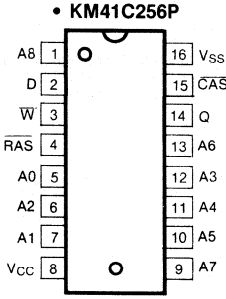
2

FUNCTIONAL BLOCK DIAGRAM

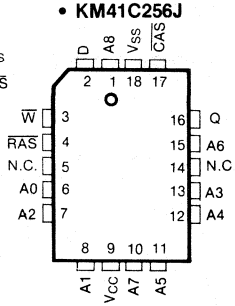


PIN CONFIGURATION (Top Views)

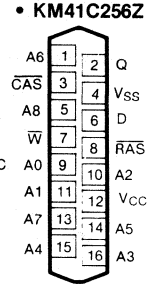
- **KM41C256P**



- **KM41C256J**



- **KM41C256Z**



Pin Name	Pin Function
A_0-A_8	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

*Note: Permanent device damage may occur of "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM41C256- 7	I_{CC1}	—	65	mA
	KM41C256- 8		—	55	mA
	KM41C256-10		—	45	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min.)	KM41C256- 7	I_{CC3}	—	65	mA
	KM41C256- 8		—	55	mA
	KM41C256-10		—	45	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling @ t_{PC}=min.)	KM41C256- 7	I_{CC4}	—	40	mA
	KM41C256- 8		—	35	mA
	KM41C256-10		—	30	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM41C256- 7	I_{CC6}	—	65	mA
	KM41C256- 8		—	55	mA
	KM41C256-10		—	45	mA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0V \leq V_{IN} \leq 6.5V$, all other pins not under test = 0 volts.)	I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0 \leq V_{OUT} \leq 5.5V$)	I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)	V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)	V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

CAPACITANCE (T_A = 25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	—	5	pF
Input Capacitance (A_0-A_8)	C_{IN2}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN3}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM41C256-7		KM41C256-8		KM41C256-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	155		175		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	25	0	25	0	25	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	

AC CHARACTERISTICS (Continued)

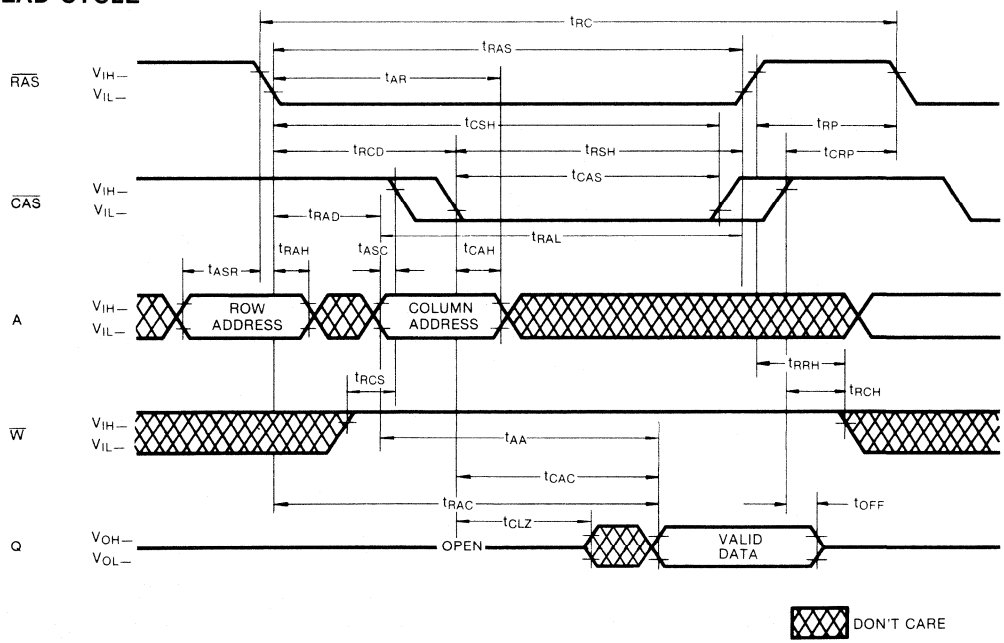
Standard Operation	Symbol	KM41C256-7		KM41C256-8		KM41C256-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	20	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		65		75		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (256 cycles)	t_{REF}		4		4		4	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	20		20		25		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	70		80		100		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		50		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20		25		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Refresh counter test $\overline{CAS}$ precharge	t_{CPT}	35		40		50		ns	
Fast Page mode cycle time	t_{PC}	45		50		60		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
Fast page mode read-modify-write	t_{PRWC}	70		75		90		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures the t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} < t_{RWD}$(min) and $_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

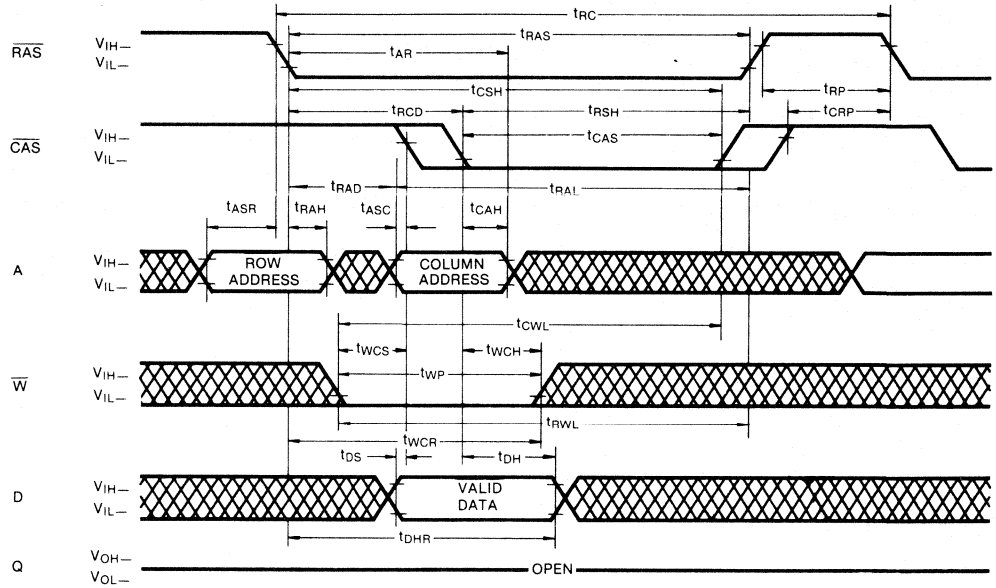
TIMING DIAGRAMS

READ CYCLE

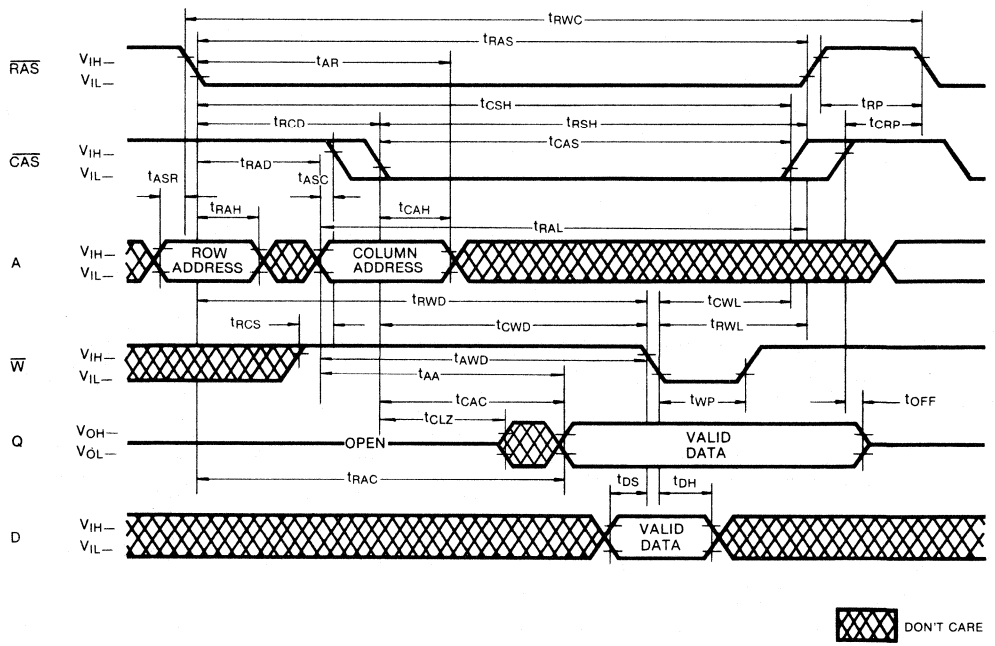


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

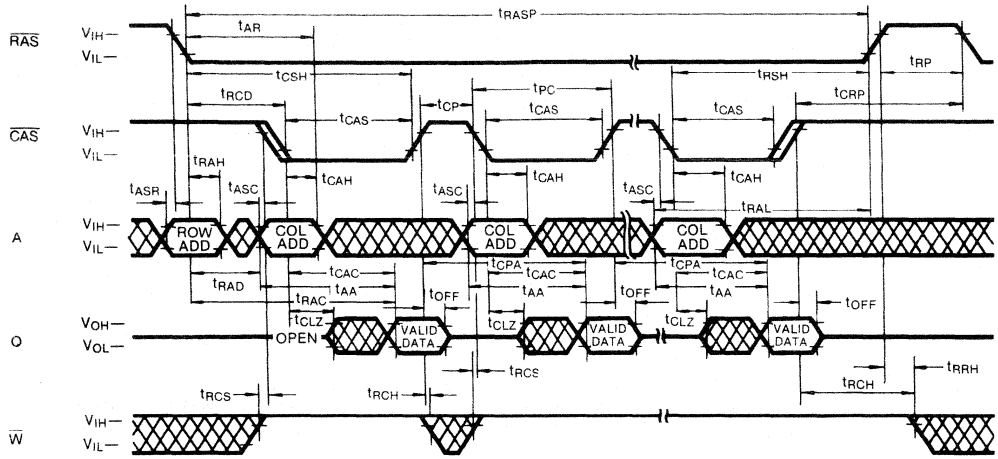


READ-WRITE/READ-MODIFY-WRITE CYCLE

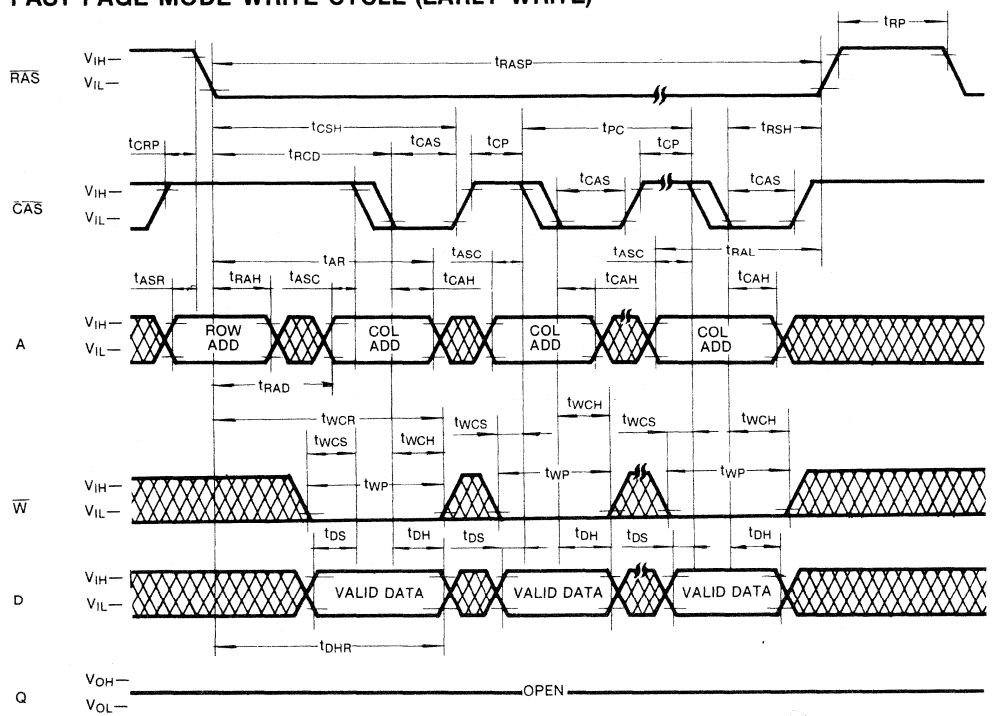


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE

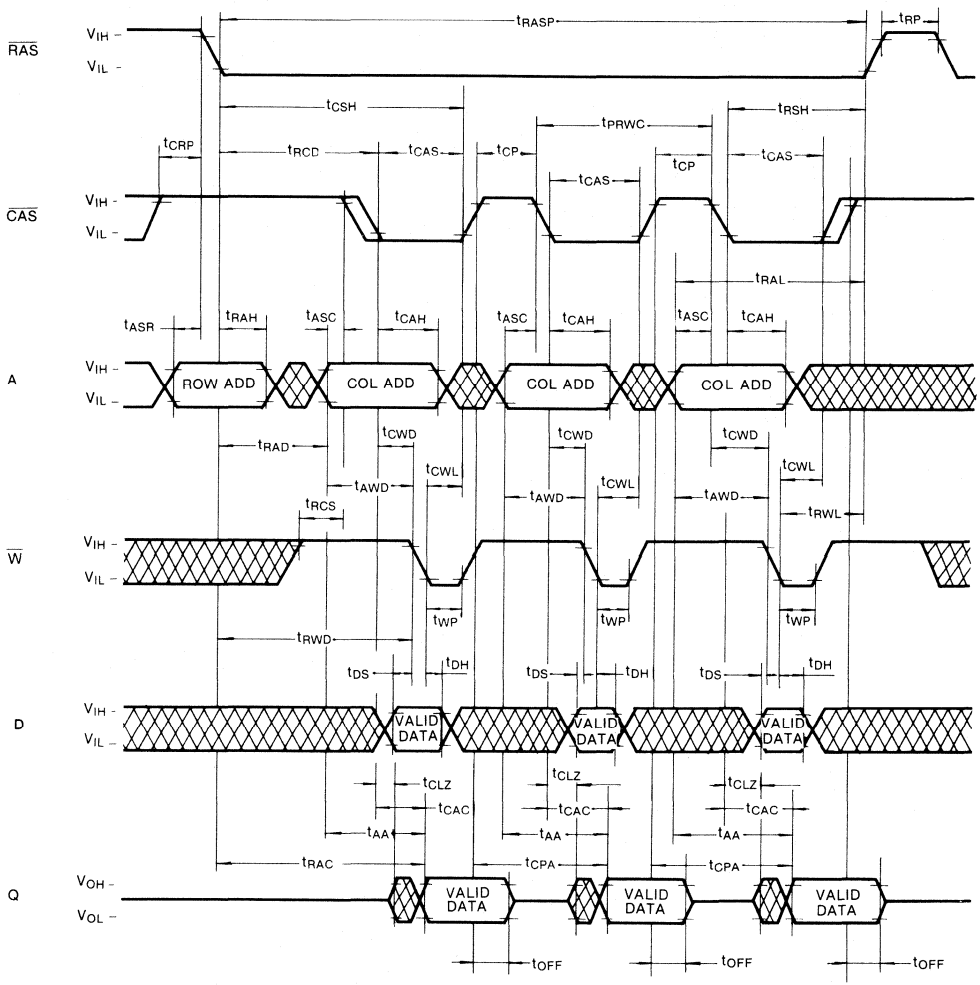


FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

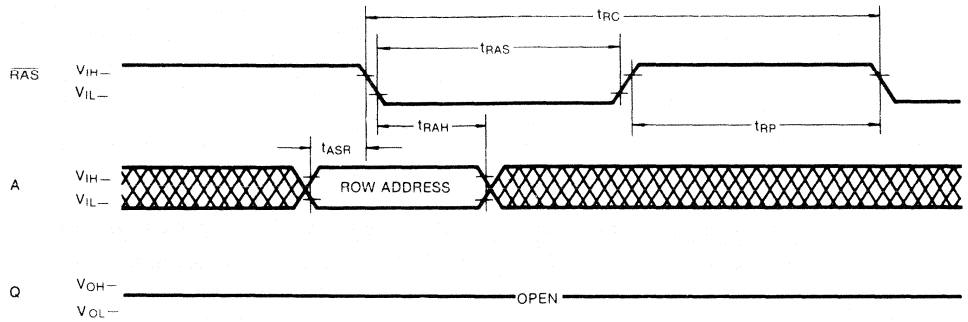
FAST PAGE MODE READ-WRITE CYCLE



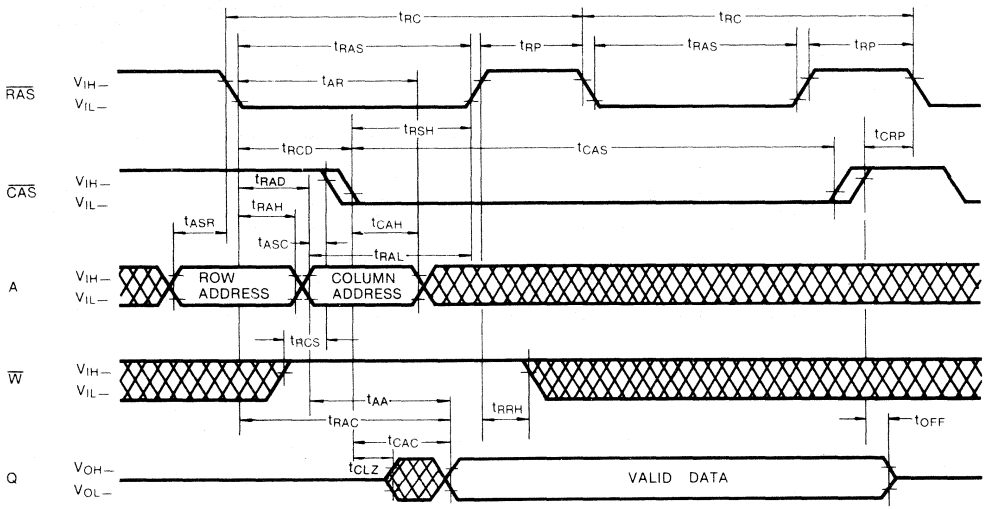
TIMING DIAGRAMS (Continued)

$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{CAS}$ = V_{IH}, $\overline{W}$,D, A_8 = Don't Care

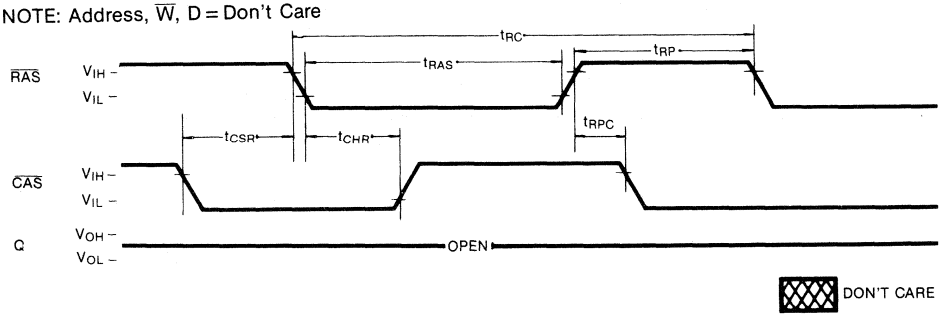


HIDDEN REFRESH CYCLE



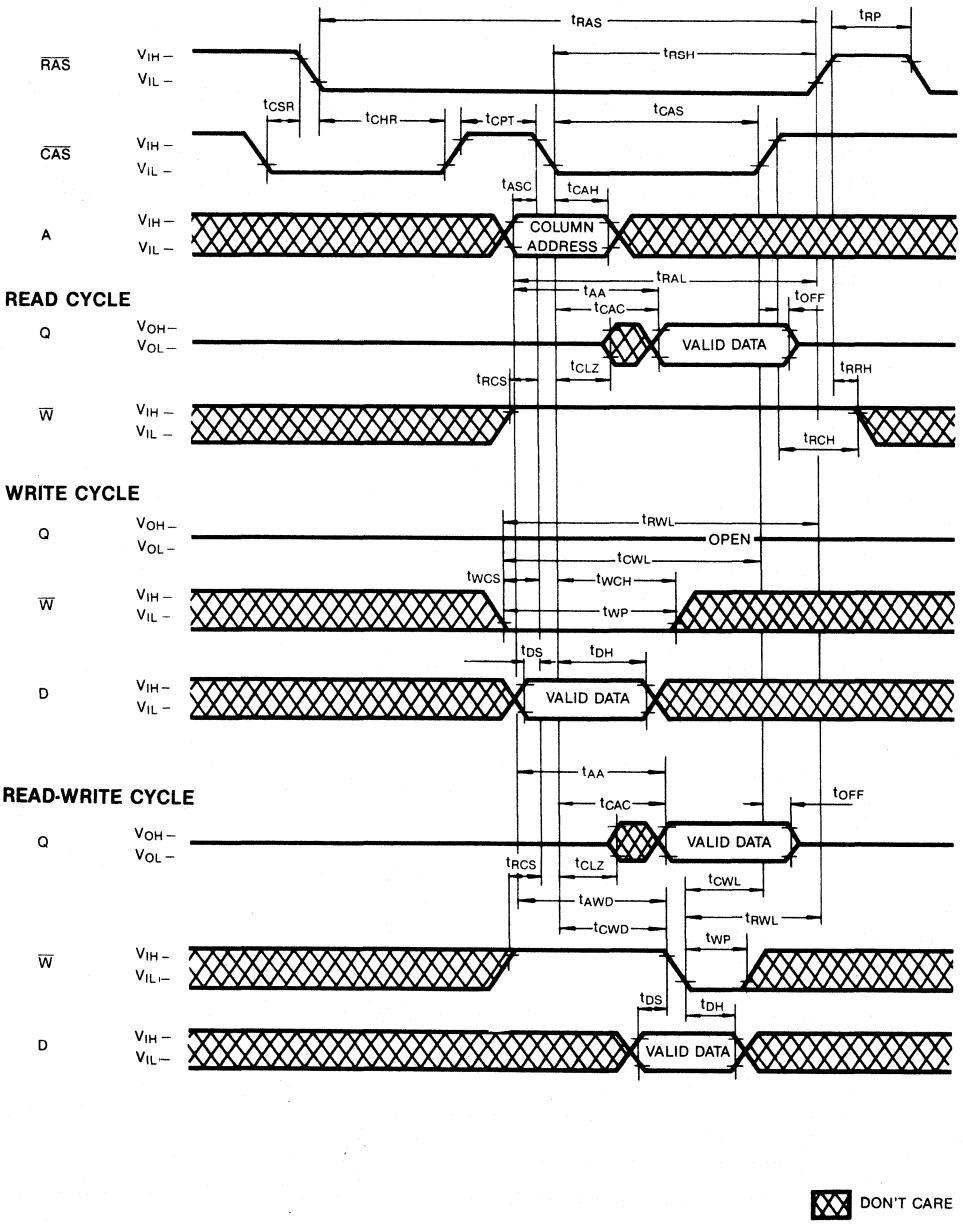
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address, $\overline{W}$, D = Don't Care



TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM41C256 contains 262,144 memory locations. Eighteen address bits are required to address a particular memory array. Since the KM41C256 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM41C256 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C256 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the RAS precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C256 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41C256 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cells. Throughout the early write cycle the outputs remain in the Hi-Z state. The cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cells appears at the outputs before and during the time that data is being written into the same cell locations. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters t_{CWD} and t_{AWD}, are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C256 has a three-state output buffers which are controlled by $\overline{CAS}$. When either $\overline{CAS}$ is high (V_{IH}) the output are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C256 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Refresh

The data in the KM41C256 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 4 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C256 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes

DEVICE OPERATION (Continued)

low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C256 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C256 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-RAS refresh is the preferred method.

Fast Page Mode

The KM41C 256 has Fast Page mode capability. Fast Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In Fast Page mode, it is possible to perform read, write or readmodify-write cycles. As long as the applicable timingg requirements are observed, it is possible to mix these cycles in any order. A Fast Page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page. Up to 512 memory cells can be accessed with the same row address.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 9 row address bits and 9 column address bits defined as follows:

Row Address—Bits A_0 through A_7 are supplied by the on-chip refresh counter. The A_8 bit is set High internally.

Column Address—Bits A_0 through A_8 are strobed-in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.

2. Write a test pattern of "lows" int the memory cells at a single column address and 256 row addresses. (The row addresses are supplied by the on-chip refresh counter.)

3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 256 times so that highs are written into the 256 memory cells.

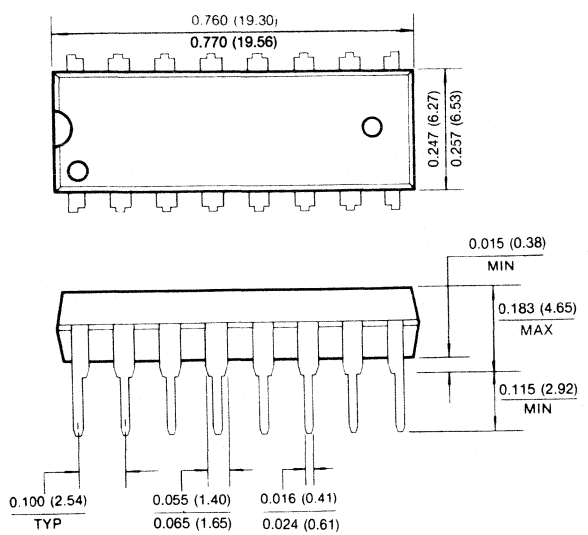
4. Read the "highs" written during step 3.

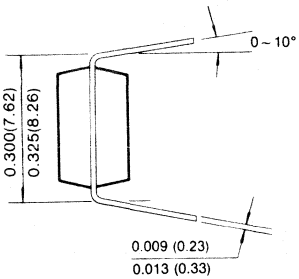
5. Complement the test pattern and repeat steps 2, 3 and 4.

PACKAGE DIMENSIONS

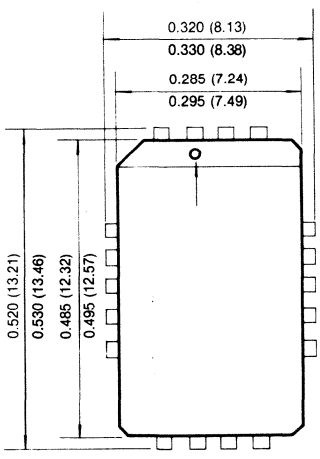
16-LEAD PLASTIC DUAL IN-LINE PACKAGE

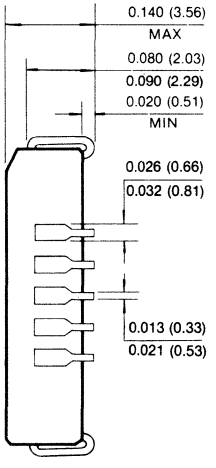
Units: Inches (millimeters)

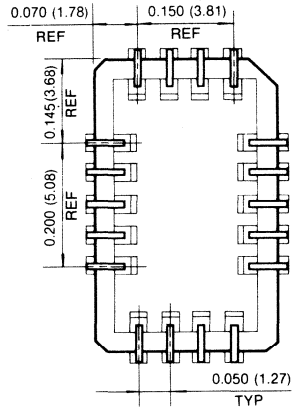




18- LEAD PLASTIC CHIP CARRIER



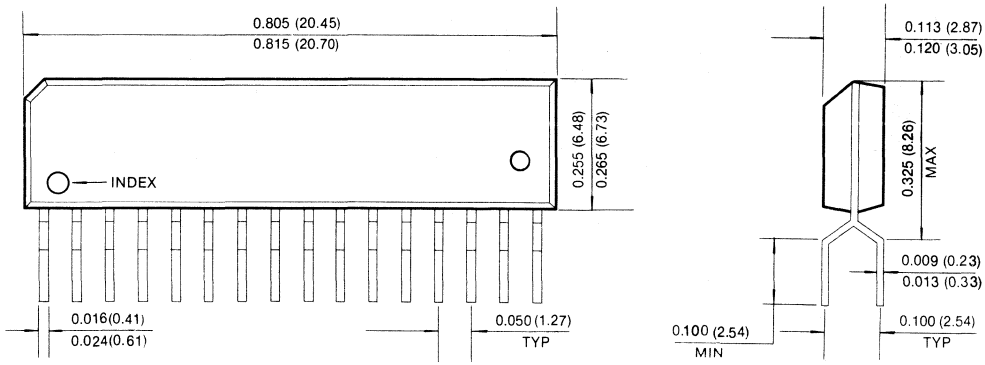




PACKAGE DIMENSIONS (Continued)

16-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE

Units: Inches (millimeters)



256K x 1 Bit CMOS Dynamic RAM with Nibble Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C257-7	70ns	20ns	130ns
KM41C257-8	80ns	20ns	150ns
KM41C257-10	100ns	25ns	180ns

- **Nibble Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Write**
- **Single +5V ± 10% power supply**
- **256 cycles/4ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic DIP, PLCC or ZIP**

GENERAL DESCRIPTION

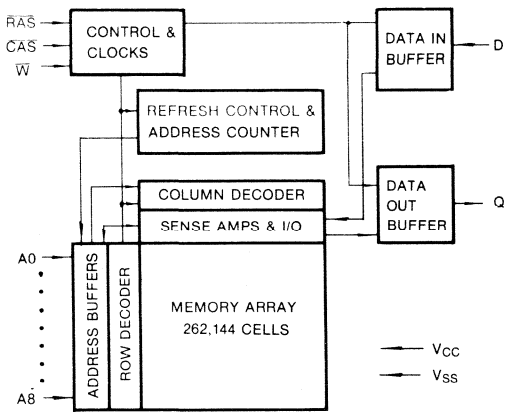
The Samsung KM41C257 is a CMOS high speed 262,144 bit x 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C257 features Nibble Mode operation which allows high speed serial access of up to 4 bits of data. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and output are fully TTL compatible.

The KM41C257 is fabricated using Samsung's advanced CMOS process.

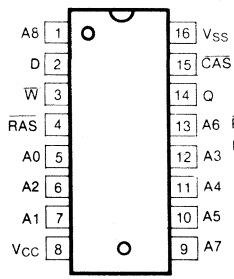
2

FUNCTIONAL BLOCK DIAGRAM

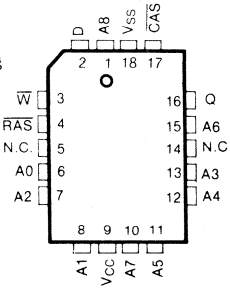


PIN CONFIGURATION (Top Views)

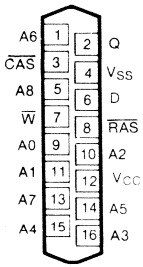
- **KM41C257P**



- **KM41C257J**



- **KM41C257Z**



Pin Name	Pin Function
A_0-A_8	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

*Note: Permanent device damage may occur of "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	$V_{CC}+1$	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC}=min.)	KM41C257-7	I_{CC1}	—	65	mA
	KM41C257-8		—	55	mA
	KM41C257-10		—	45	mA
Standby Current ($\overline{RAS}=\overline{CAS}=V_{IH}$)		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}=V_{IH}$, $\overline{RAS}$ Cycling @t_{RC}=min.)	KM41C257-7	I_{CC3}	—	65	mA
	KM41C257-8		—	55	mA
	KM41C257-10		—	45	mA
Nibble Mode Current* ($\overline{RAS}=V_{IL}$, $\overline{CAS}$ Address Cycling @t_{NC}=min.)	KM41C257-7	I_{CC4}	—	40	mA
	KM41C257-8		—	35	mA
	KM41C257-10		—	30	mA
Standby Current ($\overline{RAS}=\overline{CAS}=V_{CC}-0.2V$)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	KM41C257-7	I_{CC6}	—	65	mA
	KM41C257-8		—	55	mA
	KM41C257-10		—	45	mA
Input Leakage Current (Any input $0V \le V_{IN} \le 6.5V$, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0 \le V_{OUT} \le 5.5V$)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

CAPACITANCE (T_A = 25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	—	5	pF
Input Capacitance (A_0-A_8)	C_{IN2}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN3}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{CC} = 5.0V ± 10%. See notes 1, 2)

Parameter	Symbol	KM41C257-7		KM41C257-8		KM41C257-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	155		175		210		ns	
Nibble mode cycle time	t_{NC}	40		40		45		ns	
Nibble mode read-write cycle time	t_{NRWC}	65		65		75		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Nibble mode access time	t_{NCAC}		20		20		25	ns	3
Access time from column address	t_{AA}		35		40		50	ns	3
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	25	0	25	0	30	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	20	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		65		75		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	

STANDARD OPERATION (Continued)

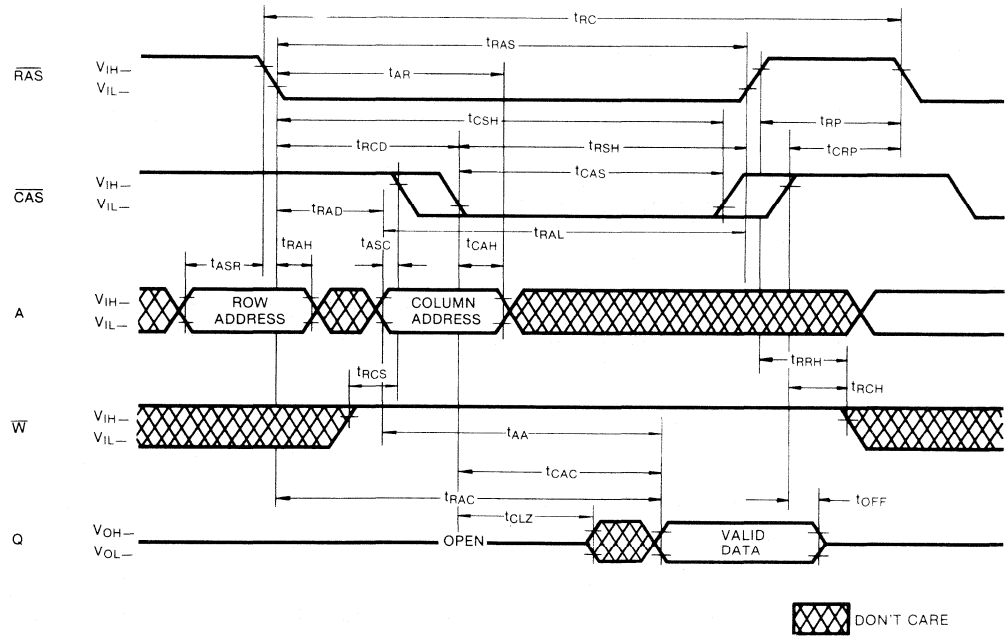
Parameter	Symbol	KM41C257-7		KM41C257-8		KM41C257-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	15		20		20		ns	10
Data hold referenced to $\overline{RAS}$	t_{DHR}	55		65		75		ns	6
Refresh period (256 cycles)	t_{REF}		4		4		4	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	20		20		25		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	70		80		100		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		50		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$ Before $\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ Before $\overline{RAS}$ refresh)	t_{CHR}	20		25		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Refresh counter test $\overline{CAS}$ precharge time	t_{CPT}	35		40		50		ns	
Nibble mode $\overline{CAS}$ pulse width	t_{NCAS}	20		20		25		ns	
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	10		10		10		ns	
Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	20		20		25		ns	
Nibble mode $\overline{CAS}$ to $\overline{W}$ delay time	t_{NCWD}	20		20		25		ns	
Nibble mode $\overline{W}$ to $\overline{RAS}$ lead time	t_{NRWL}	20		20		25		ns	
Nibble mode $\overline{W}$ to $\overline{CAS}$ lead time	t_{NCWL}	20		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures the t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} < t_{RWD}$(min) and $_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

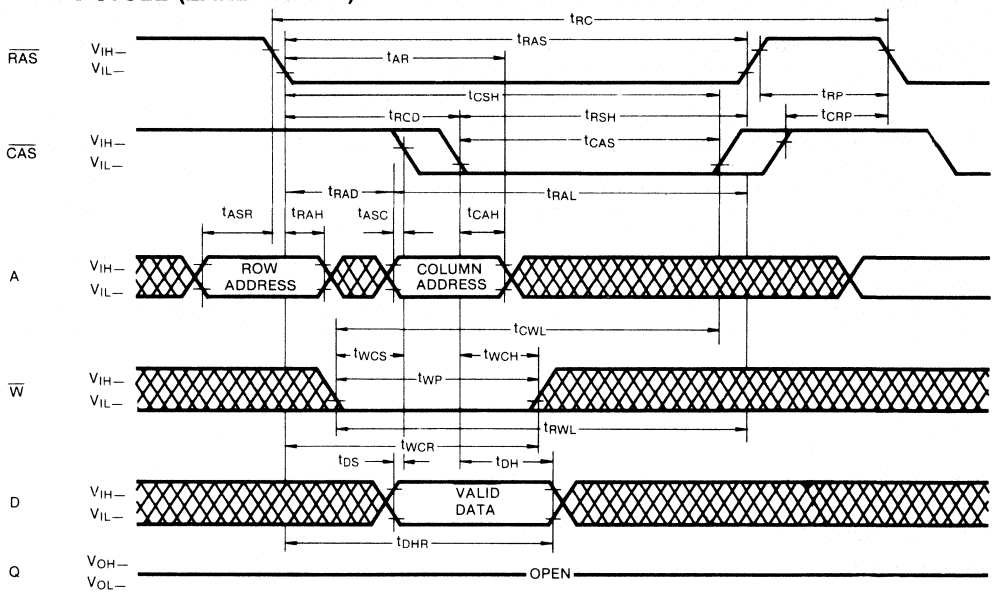
TIMING DIAGRAMS

READ CYCLE

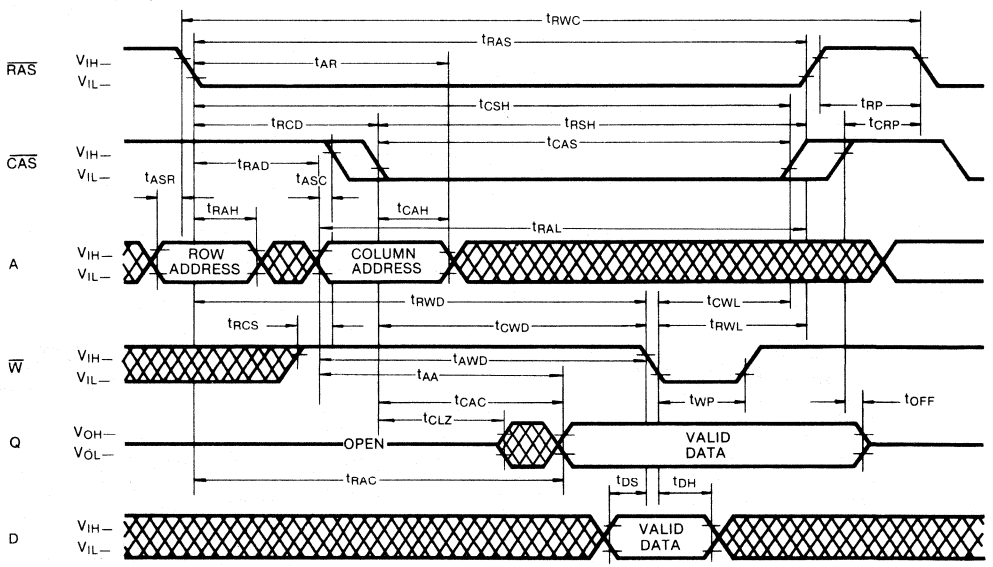


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



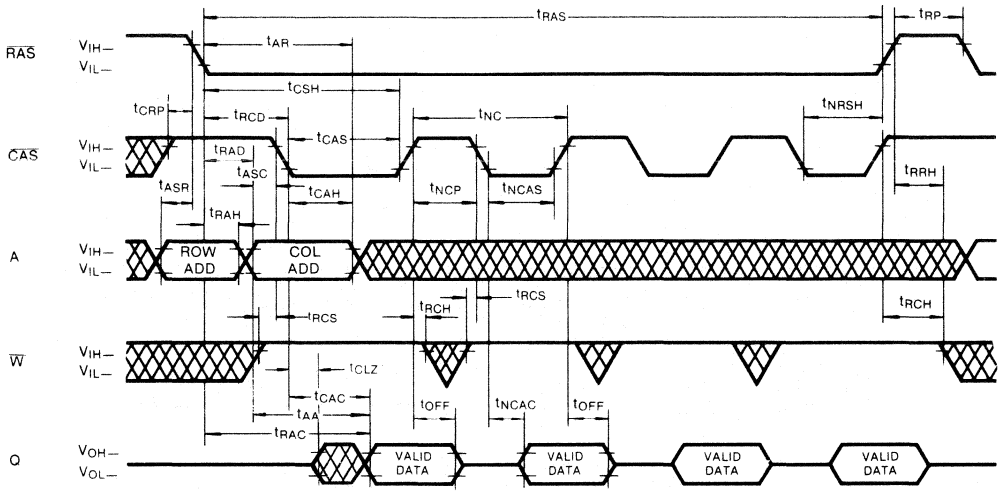
READ-WRITE/READ-MODIFY-WRITE CYCLE



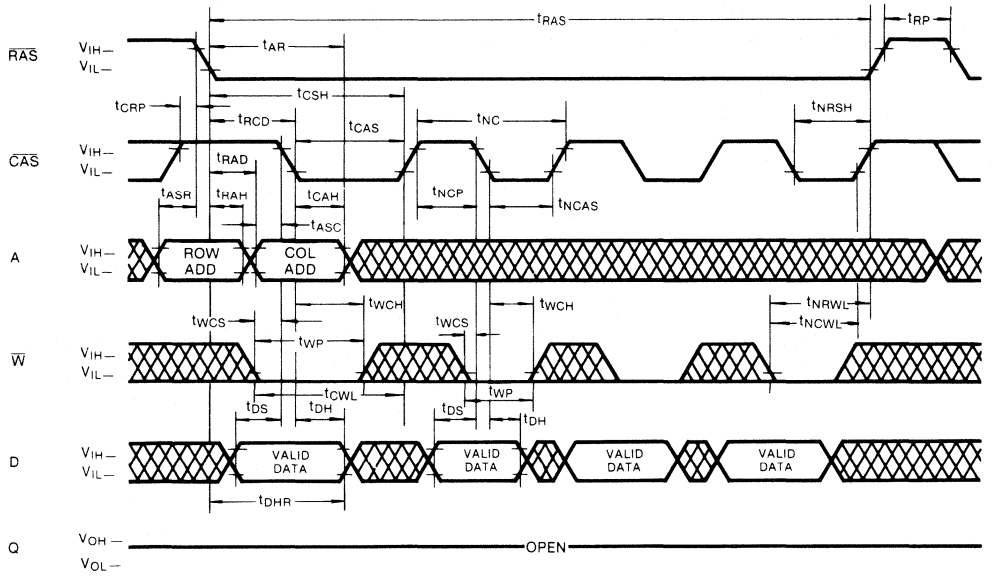
DON'T CARE

TIMING DIAGRAMS (Continued)

NIBBLE MODE READ CYCLE



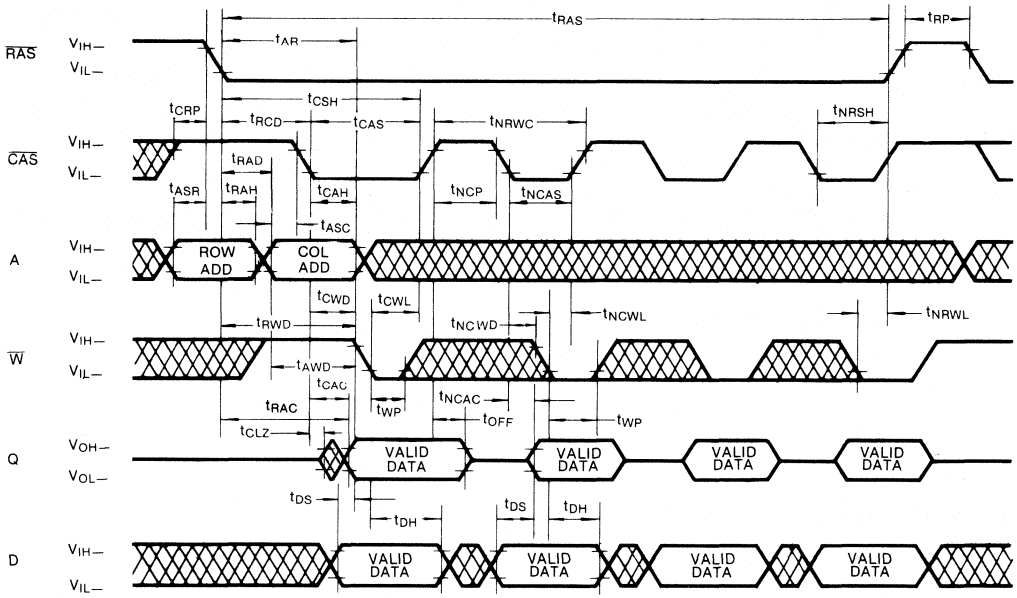
NIBBLE MODE WRITE CYCLE (EARLY WRITE)



DON'T CARE

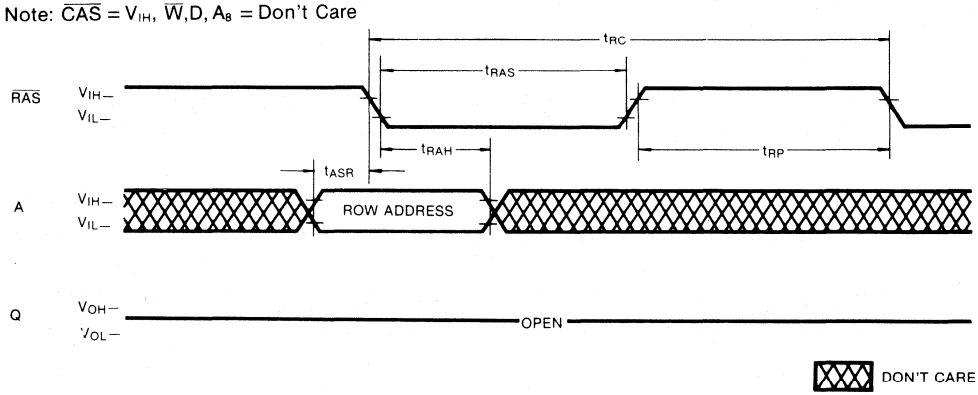
TIMING DIAGRAMS (Continued)

NIBBLE MODE READ-WRITE CYCLE



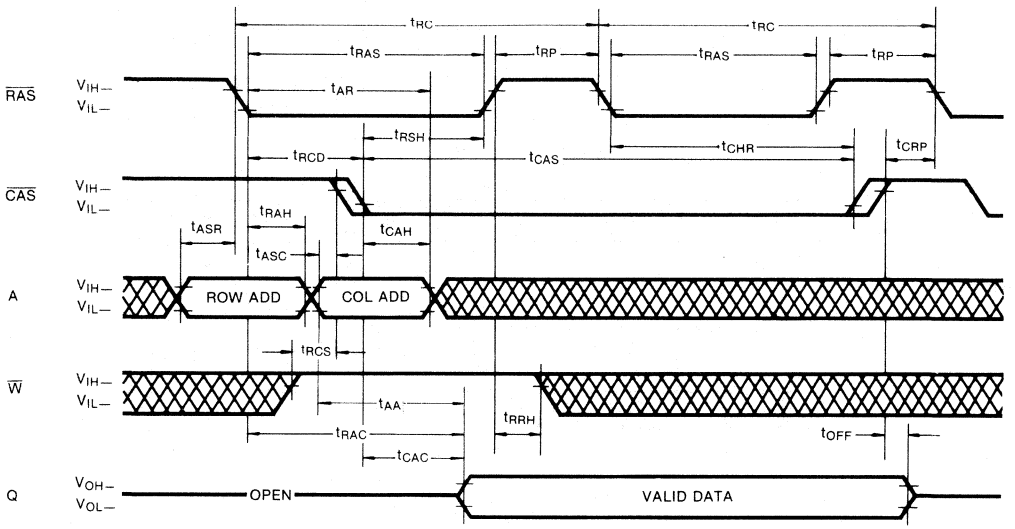
RAS-ONLY REFRESH CYCLE

Note: $\overline{CAS}$ = V_{IH}, $\overline{W}$,D, A_8 = Don't Care



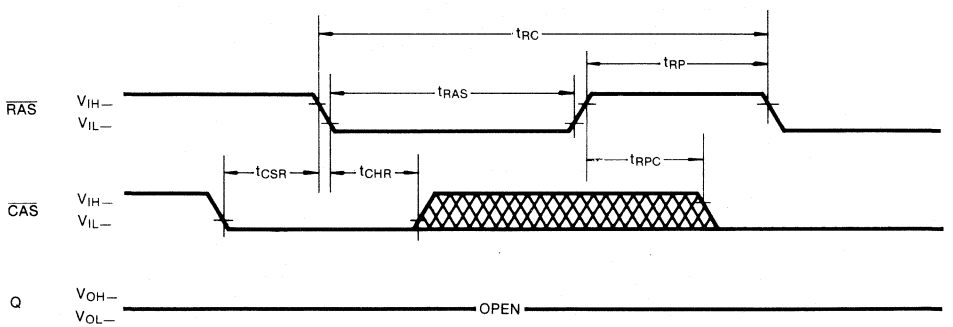
TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE



CAS-BEFORE-RAS REFRESH CYCLE

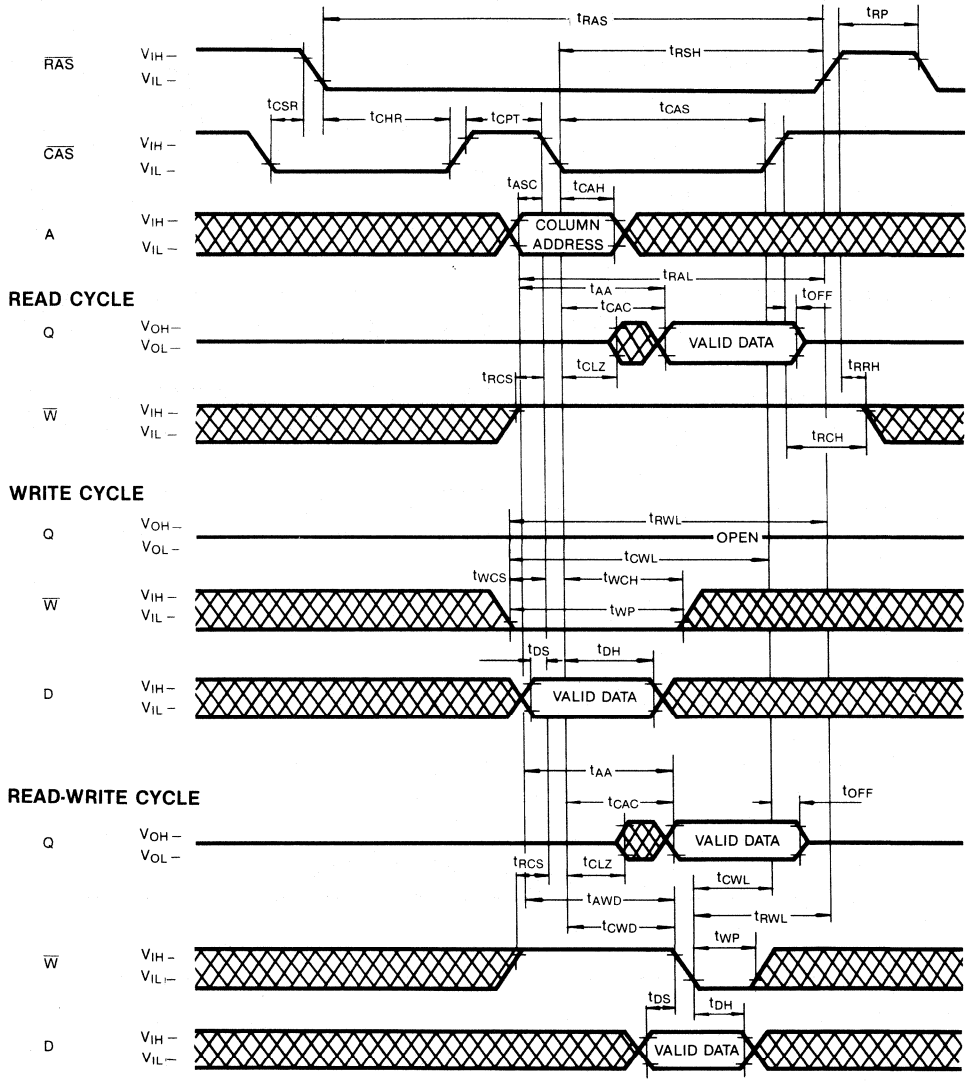
NOTE: Address, W, D = Don't Care



DON'T CARE

TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM41C257 contains 262,144 memory locations. Eighteen address bits are required to address a particular 4-bit word in the memory array. Since the KM41C257 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM41C257 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C257 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C257 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41C257 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cells. Throughout the early write cycle the outputs remain in the Hi-Z state. The cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cells appears at the outputs before and during the time that data is being written into the same cell locations. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters t_{CWD} and t_{AWD}, are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C257 has a three-state output buffers which are controlled by $\overline{CAS}$. When either $\overline{CAS}$ is high (V_{IH}) the output are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C257 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Nibble Mode Read, Nibble Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Nibble Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Refresh

The data in the KM41C257 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 4 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C257 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An inter

DEVICE OPERATION (Continued)

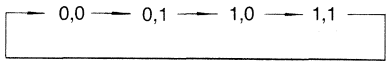
nal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C257 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C257 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$ before-$\overline{RAS}$ refresh is the preferred method.

Nibble Mode

The KM41C257 has Nibble mode capability. Nibble mode operation allows high speed serial read, write or read-write access of 4 consecutive bits. The first of 4 bits is accessed in the usual manner. The remaining nibble bits are accessed by toggling $\overline{CAS}$ high then low while $\overline{RAS}$ remains low.



The 4 bits of data that may be accessed during Nibble mode are determined by the lower 8 row address bits (R_{A0}-R_{A7}) and 8 column address bits (C_{A0}-C_{A7}). The two address bits, C_{A8} and R_{A8}, are used to select 1 of the 4 nibble bits for initial access. The remaining nibble bits are accessed by toggling $\overline{CAS}$ with $\overline{RAS}$ held low. Each high-low $\overline{CAS}$ transition will internally increment the nibble address (C_{A8}, R_{A8}) as shown in the following diagram with R_{A8} being the least significant bit.

If more than 4 bits are accessed during Nibble mode, the address sequence will wrap around and repeat. If any bit is written during Nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on a subsequent access, the new data will be written into the selected cell location.

A Nibble mode cycle can be a read, write, or read-modify-write cycle. Any combinations of reads and writes or read-modify-writes are allowed.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 9 row address bits and 9 column address bits defined as follows:

Row Address—Bits A_0 through A_7 are supplied by the on-chip refresh counter. The A_8 bit is set High internally.

Column Address—Bits A_0 through A_8 are strobed-in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 cycles.

2. Write a test pattern of "lows" int the memory cells at a single column address and 256 row addresses. (The row addresses are supplied by the on-chip refresh counter.)

3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 256 times so that highs are written into the 256 memory cells.

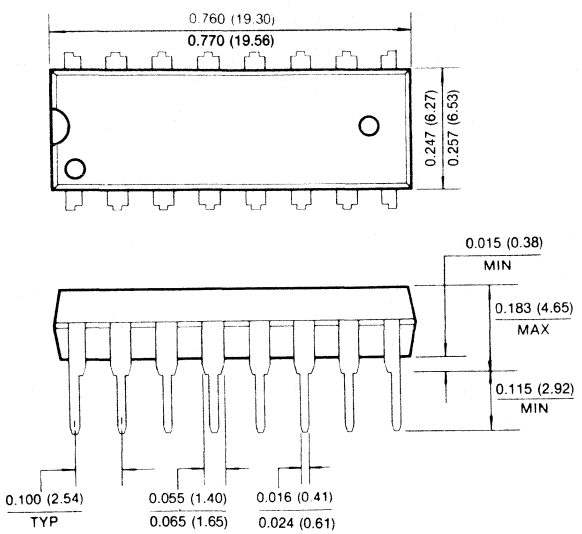
4. Read the "highs" written during step 3.

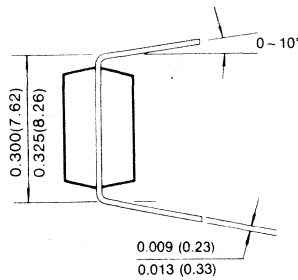
5. Complement the test pattern and repeat steps 2, 3 and 4.

PACKAGE DIMENSIONS

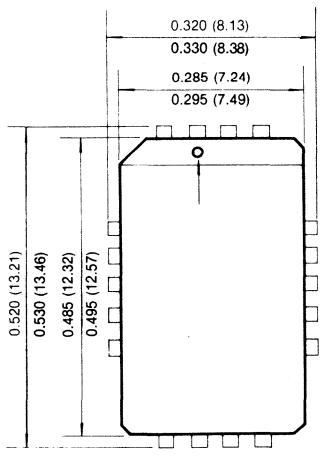
16-LEAD PLASTIC DUAL IN-LINE PACKAGE

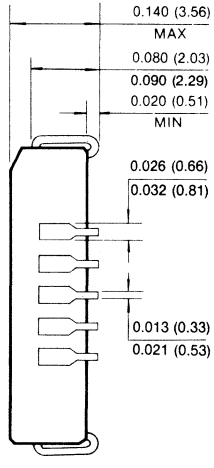
Units: Inches (millimeters)

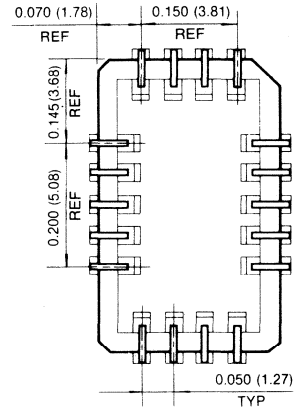




18- LEAD PLASTIC CHIP CARRIER



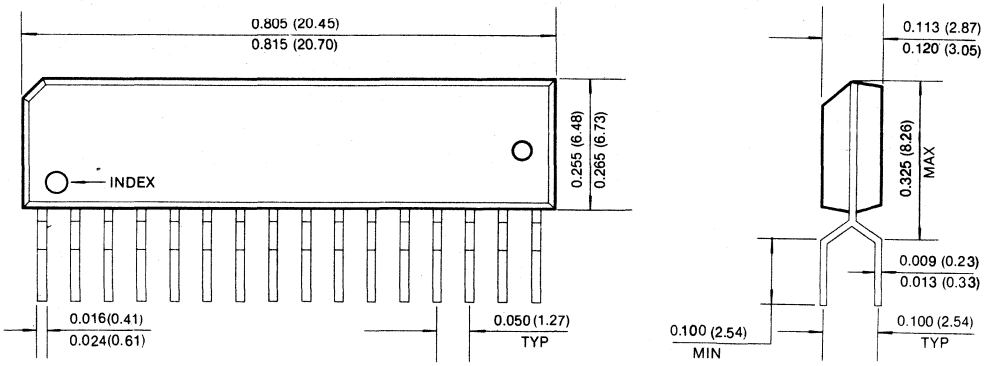




PACKAGE DIMENSIONS (Continued)

16-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE

Units: Inches (millimeters)



256K x 1 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C258-7	70ns	20ns	130ns
KM41C258-8	80ns	20ns	150ns
KM41C258-10	100ns	25ns	180ns

- **Static Column Mode operation**
- **$\overline{CS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Write**
- **Single +5V ± 10% power supply**
- **256 cycles/4ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic DIP, PLCC or ZIP**

GENERAL DESCRIPTION

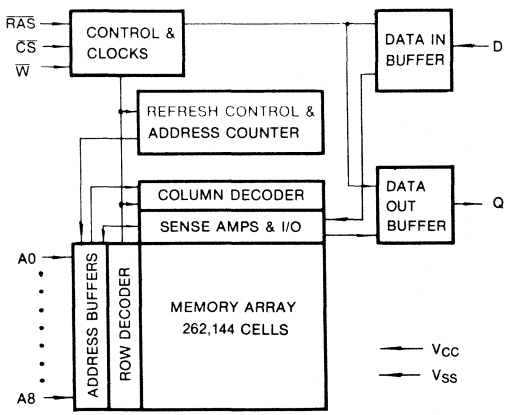
The Samsung KM41C258 is a CMOS high speed 262,144 bit x 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C258 features Static Column Mode operation which allows high speed random or sequential cells within a row. Static Column Mode operation offers high performance while relaxing many critical system timing requirements for fast usable speed.

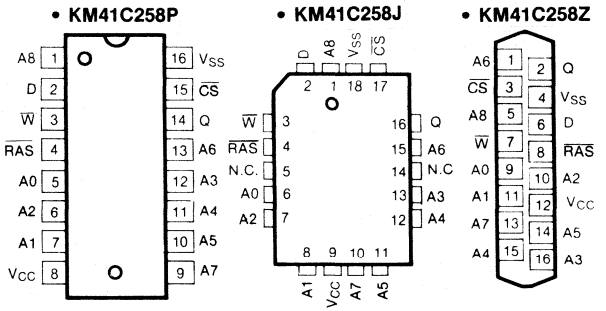
$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM41C258 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A_0-A_8	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

*Note: Permanent device damage may occur of "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	$V_{CC}+1$	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CS}$, Address Cycling @ t_{HC} = min.)	KM41C258-7	I_{CC1}	—	65	mA
	KM41C258-8		—	55	mA
	KM41C258-10		—	45	mA
Standby Current ($\overline{RAS} = \overline{CS} = V_{IH}$)		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CS} = V_{IH}$, $\overline{RAS}$ Cycling @ t_{RC} = min.)	KM41C258-7	I_{CC3}	—	65	mA
	KM41C258-8		—	55	mA
	KM41C258-10		—	45	mA
Static Column Mode Current* ($\overline{RAS} = \overline{CS} = V_{IL}$, Address Cycling: t_{SC} = min.)	KM41C258-7	I_{CC4}	—	40	mA
	KM41C258-8		—	35	mA
	KM41C258-10		—	30	mA
Standby Current ($\overline{RAS} = \overline{CS} = V_{CC} - 0.2V$)		I_{CC5}	—	1	mA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @ t_{RC} = min.)	KM41C258-7	I_{CC6}	—	65	mA
	KM41C258-8		—	55	mA
	KM41C258-10		—	45	mA
Input Leakage Current (Any input $0V \leq V_{IN} \leq 6.5V$, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0 \leq V_{OUT} \leq 5.5V$)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

CAPACITANCE (T_A = 25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	—	5	pF
Input Capacitance (A_0-A_8)	C_{IN2}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$)	C_{IN3}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{CC} = 5.0V ± 10%. See notes 1, 2)

Parameter	Symbol	KM41C258-7		KM41C258-8		KM41C258-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	155		175		210		ns	
Static column mode cycle time	t_{SC}	40		45		55		ns	
Static column mode read-write cycle time	t_{SRWC}	70		80		100		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
Access time from last write	t_{ALW}		65		75		95	ns	3,12
$\overline{CS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	25	0	25	0	30	ns	7
Output data hold time from column address	t_{AOH}	5		5		5		ns	7
Output data enable time from $\overline{W}$	t_{OW}		45		50		70	ns	
Output data hold time from $\overline{W}$	t_{WOH}	0		0		0		ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width (static column mode)	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CS}$ pulse width	t_{CS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	20	100,000	20	100,000	25	100,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	20	40	20	50	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
$\overline{CS}$ precharge time (static column mode)	t_{CP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		20		ns	
Write address hold time referenced to $\overline{RAS}$	t_{AWR}	55		65		75		ns	6
Column address hold time referenced to $\overline{RAS}$	t_{AR}	85		95		115		ns	

STANDARD OPERATION (Continued)

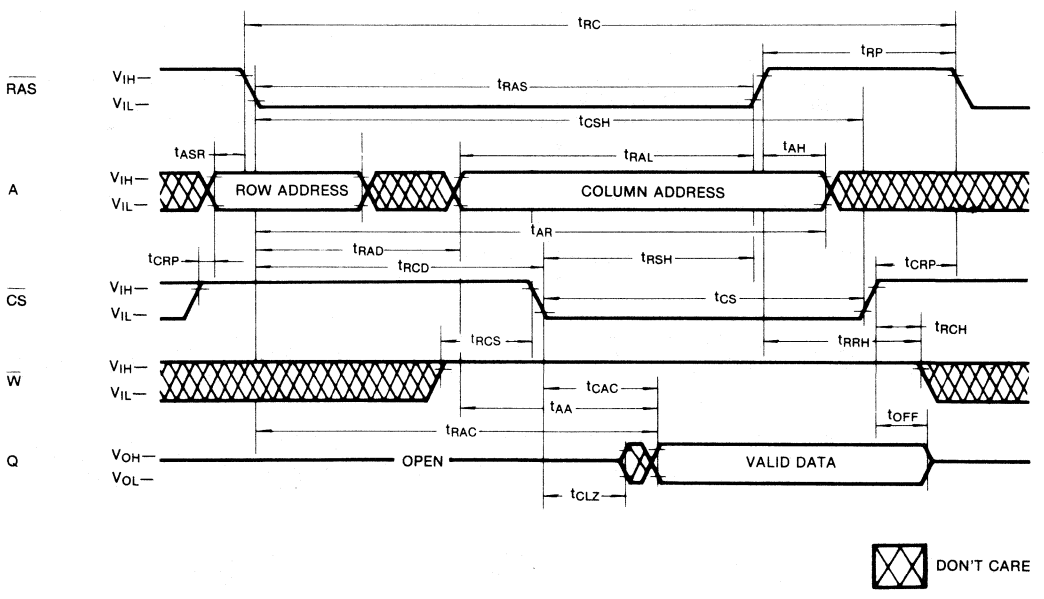
Parameter	Symbol	KM41C258-7		KM41C258-8		KM41C258-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Column address hold time referenced to $\overline{RAS}$ rise	t_{AH}	10		10		10		ns	
Last write to column address delay time	t_{LWAD}	20	30	25	35	25	45	ns	
Last write to column address hold time	t_{AHLW}	65		75		95		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		20		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		20		20		ns	
Write command inactive time	t_{WI}	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	15		20		20		ns	10
Data hold referenced to $\overline{RAS}$	t_{DHR}	55		65		75		ns	6
Refresh period (256 cycles)	t_{REF}		4		4		4	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CS}$ to $\overline{W}$ delay time	t_{CWD}	20		20		25		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	70		80		100		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		50		ns	8
$\overline{CS}$ set-up time ($\overline{CS}$ Before $\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CS}$ hold time ($\overline{CS}$ Before $\overline{RAS}$ refresh)	t_{CHR}	20		25		30		ns	
$\overline{RAS}$ precharge to $\overline{CS}$ hold time	t_{RPC}	10		10		10		ns	
Refresh counter test $\overline{CS}$ precharge time	t_{CPT}	35		40		50		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures the t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} < t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the W leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. Operation within the t_{LWAD}(max) limit insures that t_{ALW}(max) can be met. t_{LWAD}(max) is specified as a reference point only. If t_{LWAD} is greater than the specified t_{LWAD}(max) limit, then access time is controlled by t_{AA}.

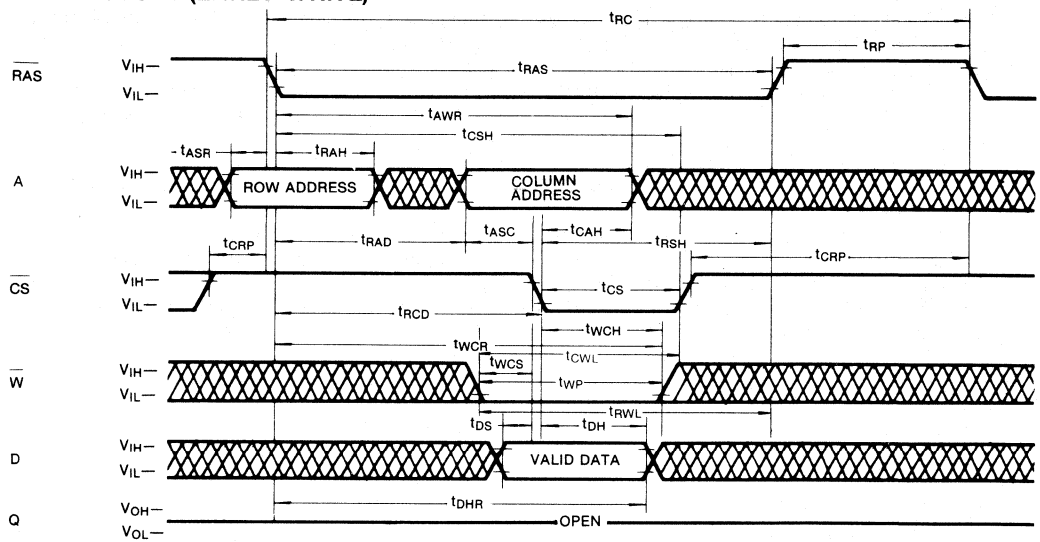
TIMING DIAGRAMS (Continued)

READ CYCLE

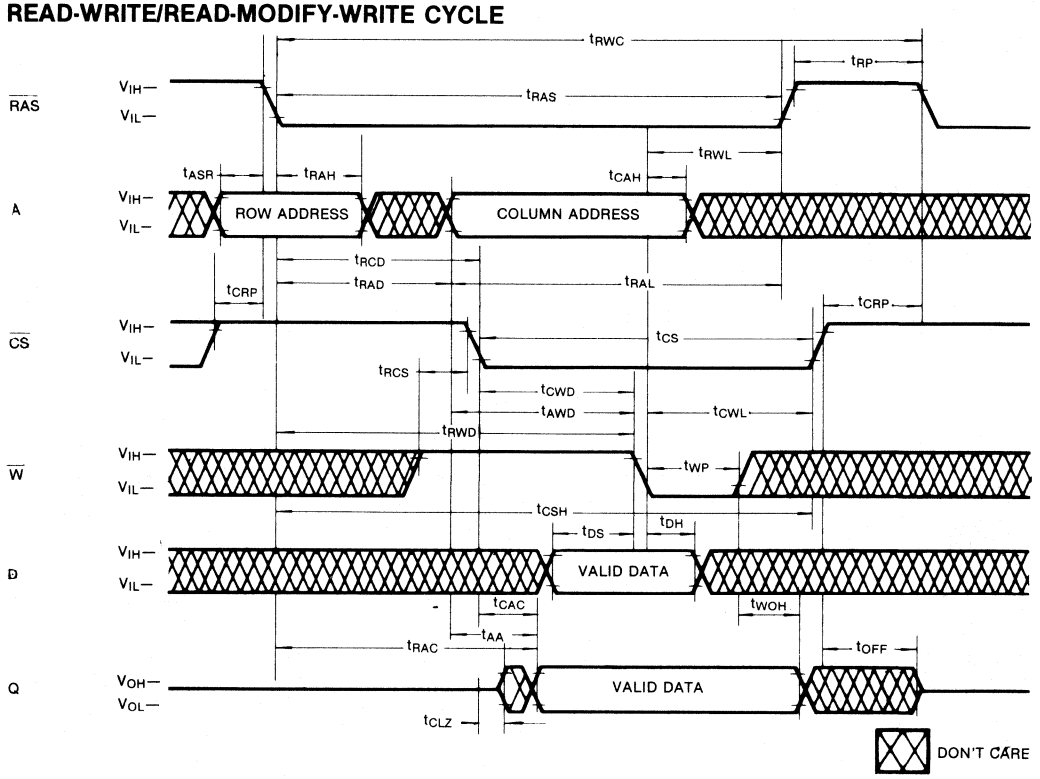


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

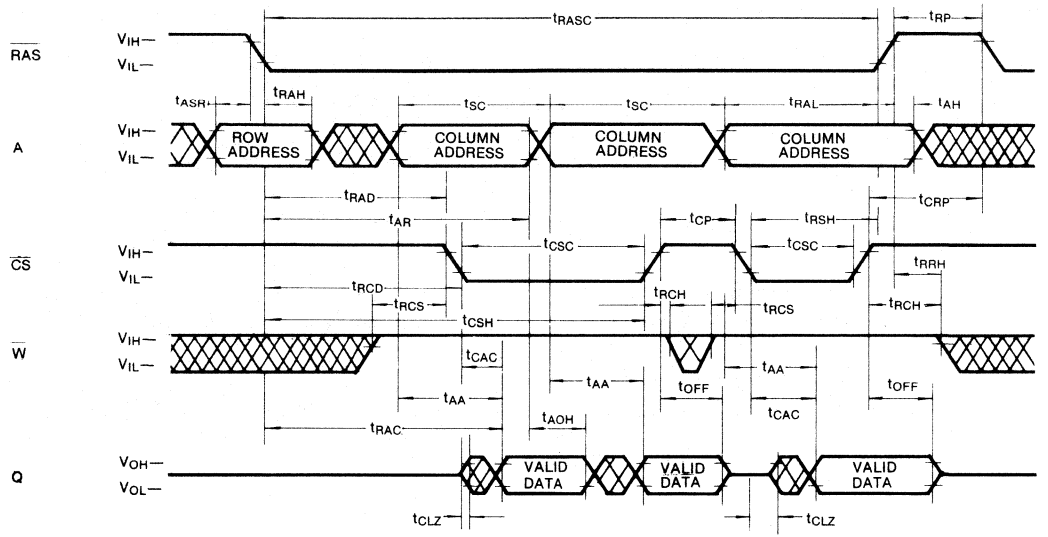


READ-WRITE/READ-MODIFY-WRITE CYCLE

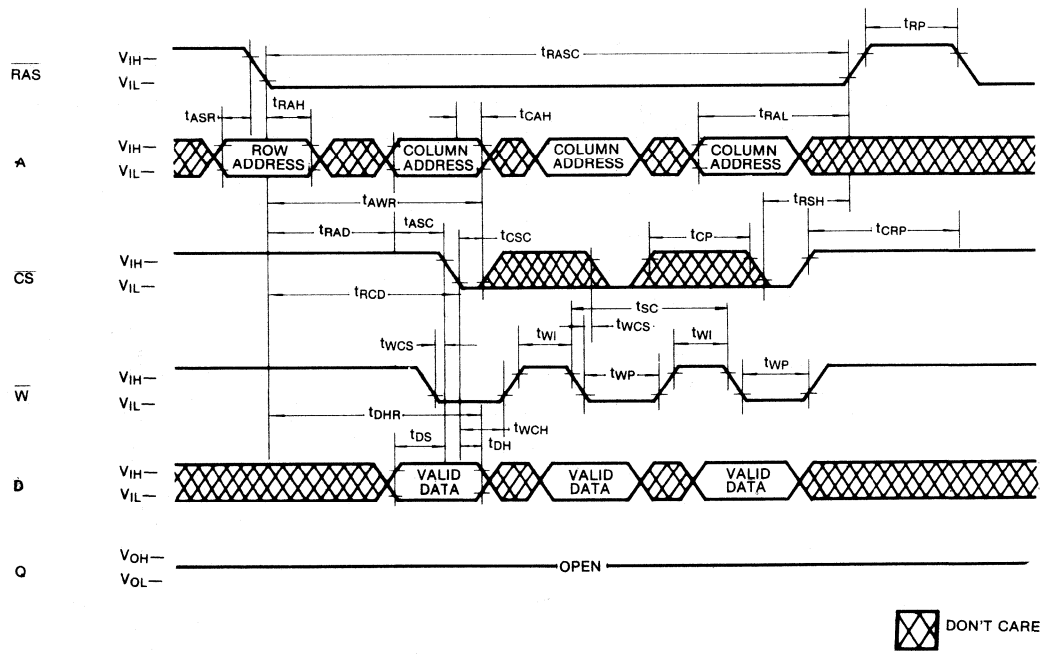


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ CYCLE

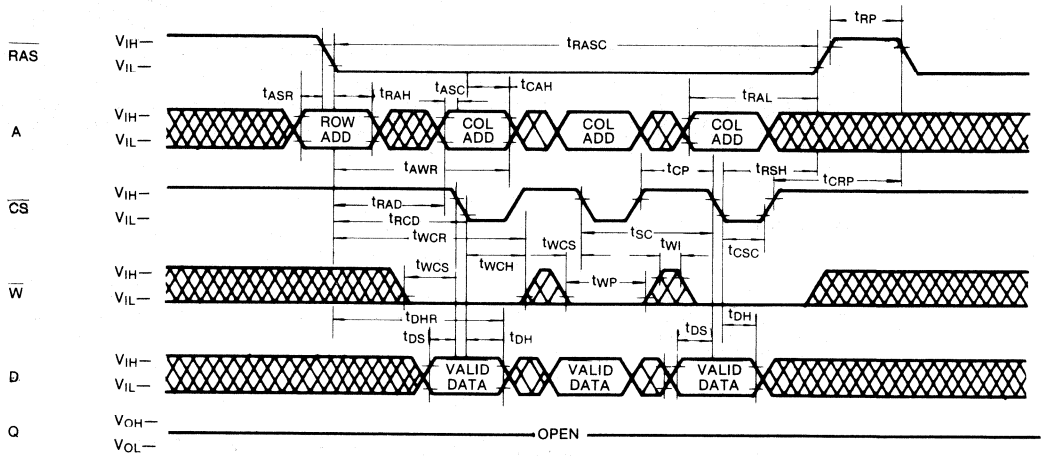


STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ controlled early write)

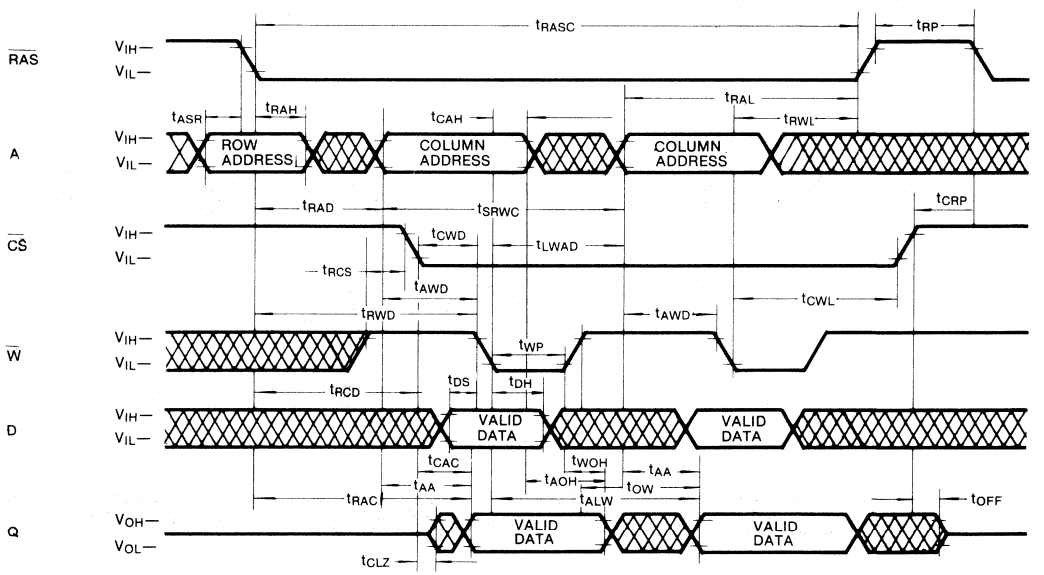


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ controlled early write)

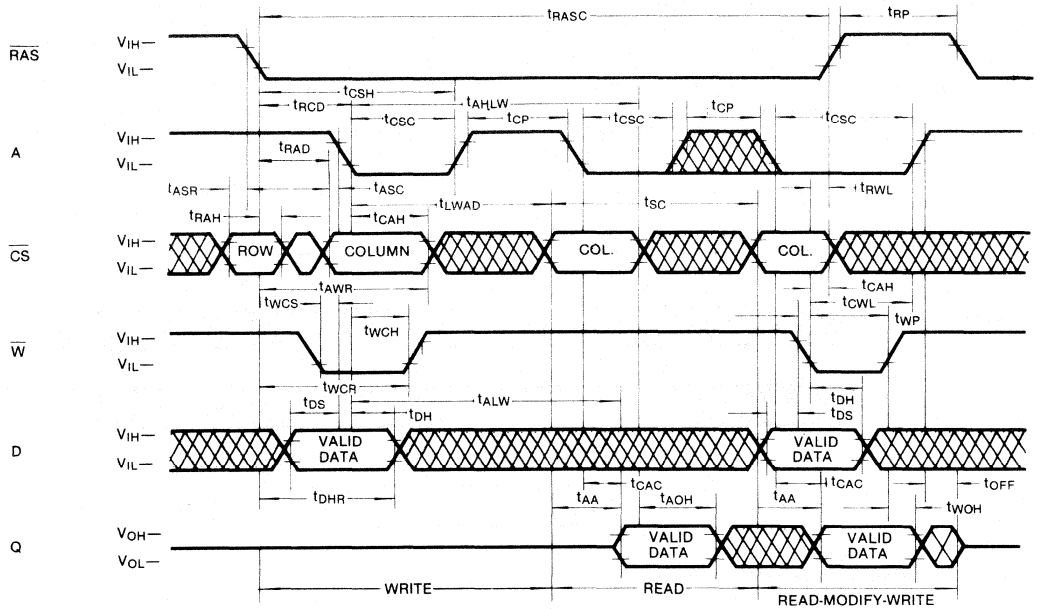


STATIC COLUMN MODE READ-WRITE CYCLE



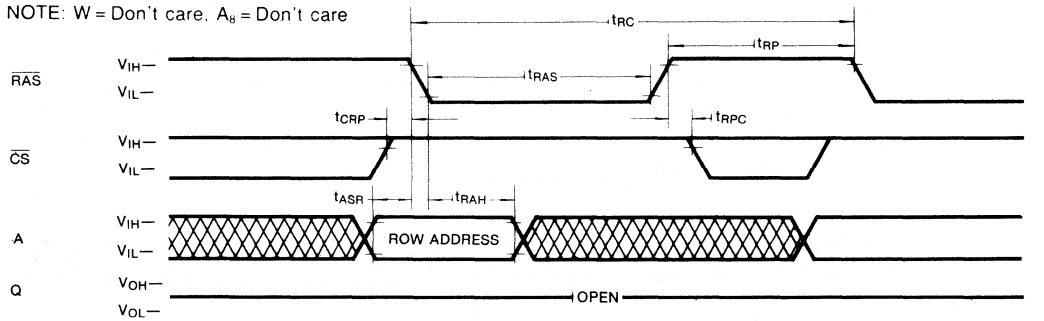
TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE MIXED CYCLE



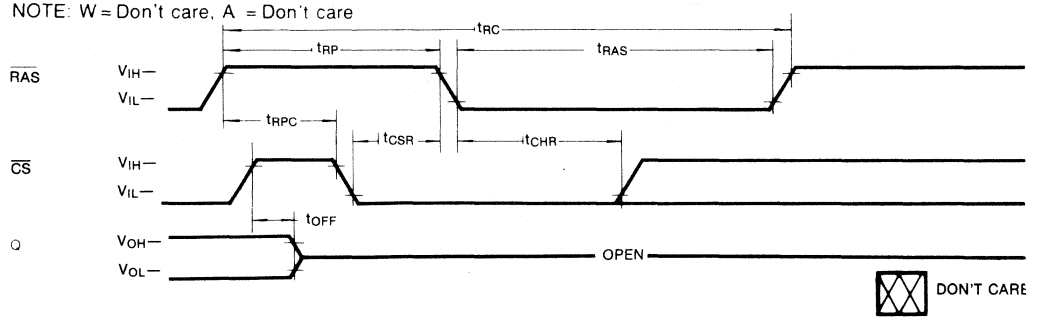
RAS-ONLY REFRESH CYCLE

NOTE: W = Don't care, A_8 = Don't care



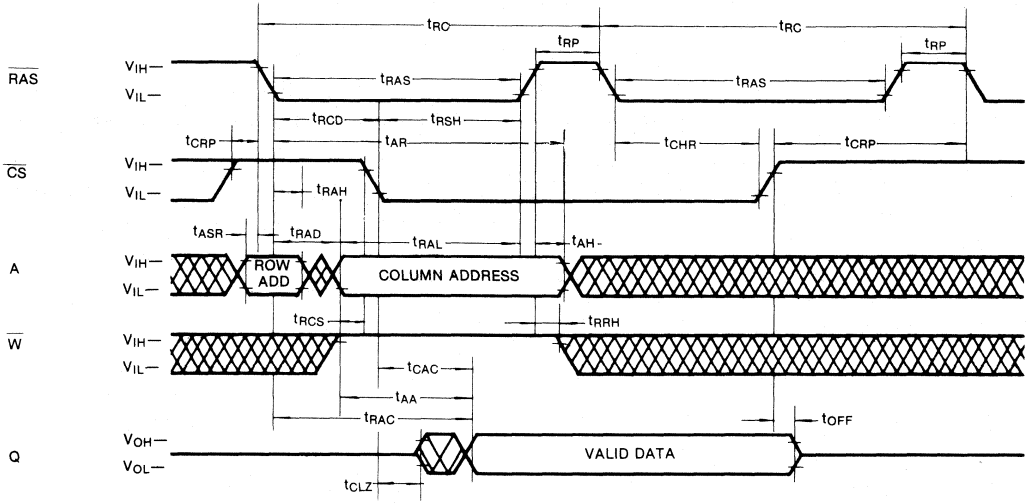
CS-BEFORE-RAS REFRESH CYCLE

NOTE: W = Don't care, A = Don't care

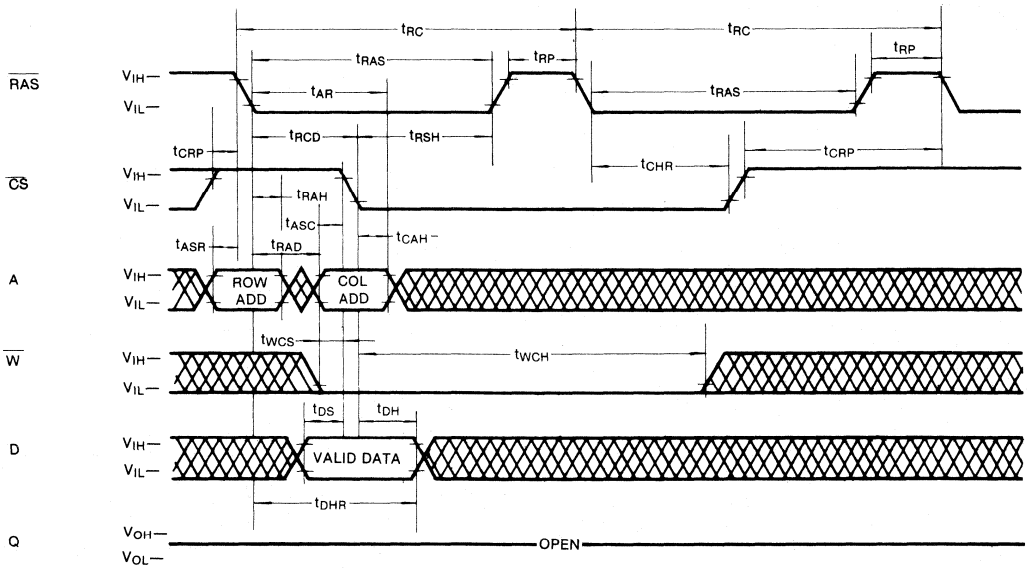


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



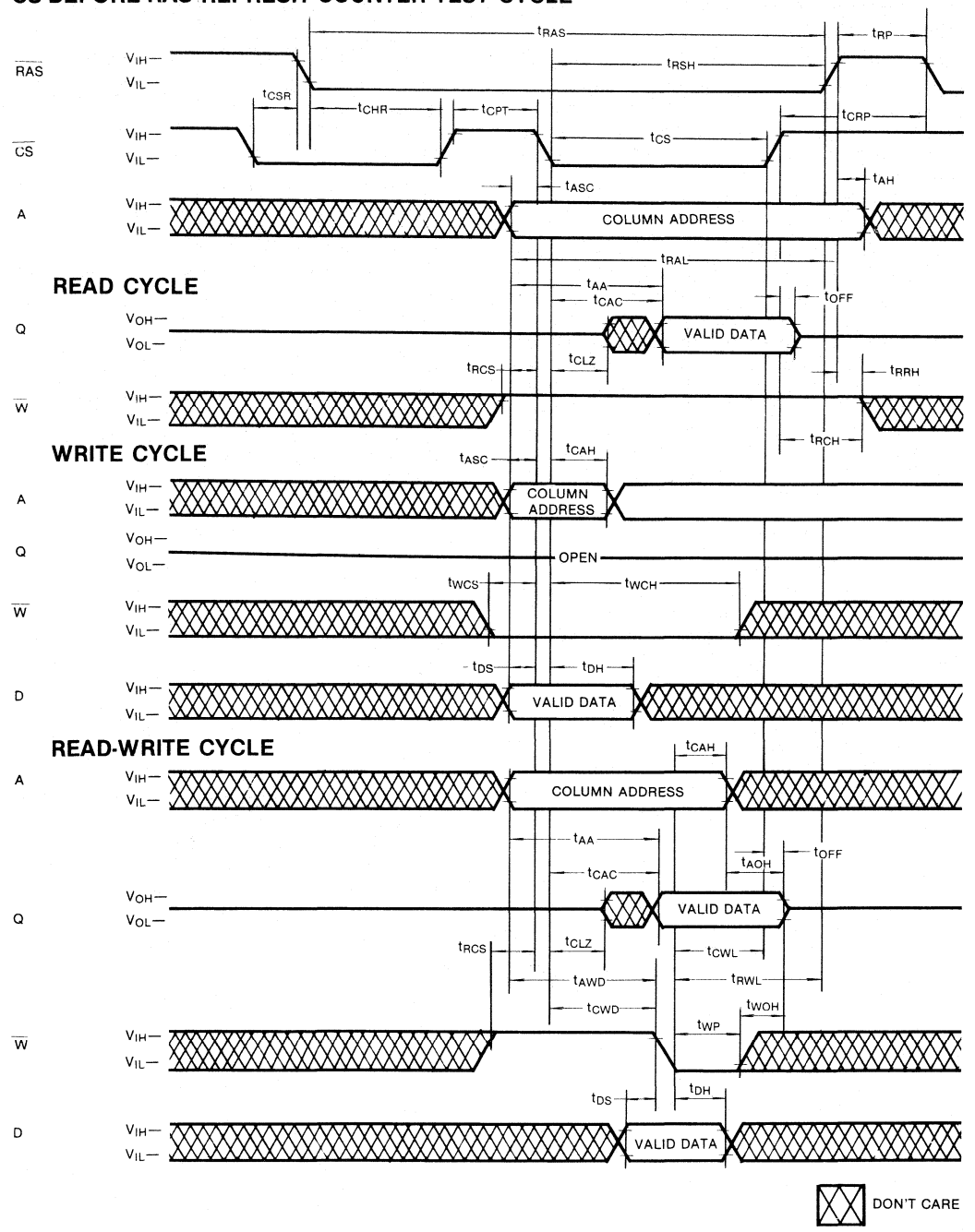
HIDDEN REFRESH CYCLE (WRITE)



DON'T CARE

TIMING DIAGRAMS (Continued)

$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM41C258 contains 262,114 memory locations. Eighteen address bits are required to address a particular 4-bit word in the memory array. Since the KM41C258 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the chip select input ($\overline{CS}$) and the valid address inputs.

Operation of the KM41C258 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CS}$. This is the beginning of any KM41C258 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths are specified by t_{RAS}(min) and t_{CS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C258 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CS}$ cycle. The access time is normally specified by t_{RAC}. If $\overline{CS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CS}$ low before t_{RCD}(max).

Write

The KM41C258 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CS}$, whichever is later.

Early Write: An early write cycle is performed by bringing W low before $\overline{CS}$. The data at the data input pin(D) is written into the addressed memory cells. Throughout the early write cycle the outputs remain in the Hi-Z state. The cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cells appears at the outputs before and during the time that data is being written into the same cell locations. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters t_{CWD} and t_{AWD}, are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C258 has a three-state output buffers which are controlled by $\overline{CS}$. When either $\overline{CS}$ is high (V_{IH}) the output are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C258 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Static Column Mode Read, Static Column Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Static Column Mode Write, $\overline{CS}$-before-$\overline{RAS}$ Refresh, $\overline{CS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C258 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integri-

DEVICE OPERATION (Continued)

ty it is necessary to refresh each of the rows every 4 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CS}$-before-RAS Refresh: The KM41C258 has $\overline{CS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CS}$ active time and cycling $\overline{RAS}$. The KM41C258 hidden refresh cycle is actually a $\overline{CS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C258 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CS}$-before-$\overline{RAS}$ refresh is the preferred method.

Static Column Mode

Static Column mode allows high speed read, write or read-modify-write access to all the memory cells within a selected row. Operation within a selected row is similar to a static RAM. The read, write or read-modify-write cycles may be mixed in any order.

A Static Column mode read cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{W} = V_{IH}$ and $\overline{RAS} = V_{IL}$.

A Static Column mode write cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{RAS} = V_{IL}$ and toggling either $\overline{W}$ or $\overline{CS}$. The data is written into the cell triggered by the latter falling edge to $\overline{W}$ or $\overline{CS}$.

$\overline{CS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 8 row address bits and 9 column address bits defined as follows:

Row Address—Bits A_0 through A_7 are supplied by the on-chip refresh counter. The A_8 bit is set High internally.

Column Address—Bits A_0 through A_8 are strobed-in by the falling edge of $\overline{CS}$ as in a normal memory cycle.

Suggested $\overline{CS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 cycles.

2. Write a test pattern of "lows" int the memory cells at a single column address and 256 row addresses. (The row addresses are supplied by the on-chip refresh counter.)

3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 256 times so that

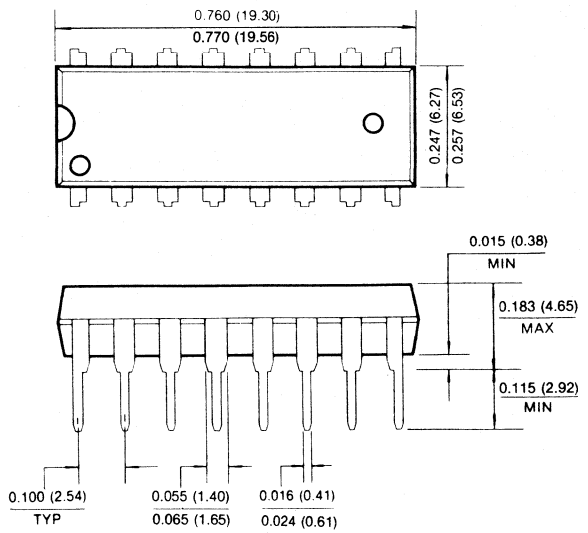
4. Read the "highs" written during step 3.

5. Complement the test pattern and repeat steps 2, 3 and 4.

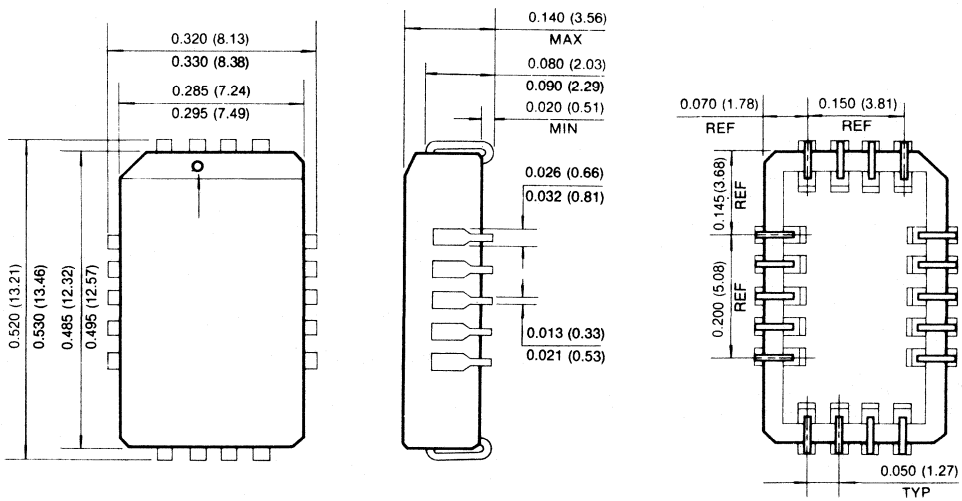
PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (millimeters)



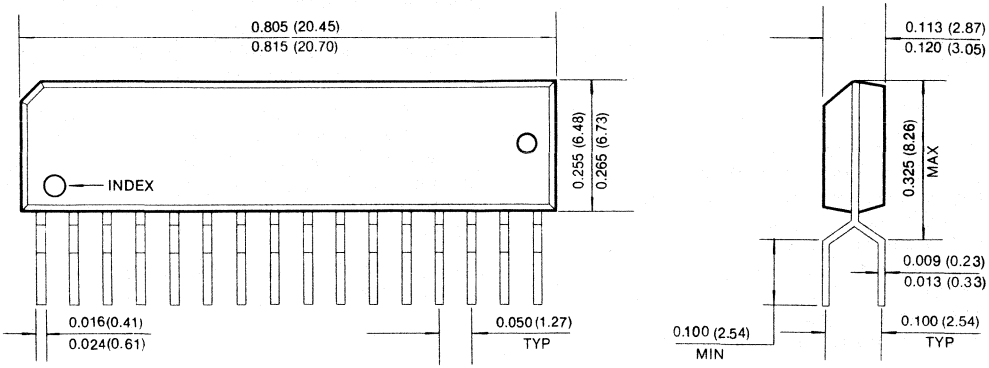
18- LEAD PLASTIC CHIP CARRIER



PACKAGE DIMENSIONS (Continued)

16-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE

Units: Inches (millimeters)



2

64K x 4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C464-7	70ns	20ns	130ns
KM41C464-8	80ns	20ns	150ns
KM41C464-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and output**
- **Early Write or output enable controlled write**
- **Single +5V ± 10% power supply**
- **256 cycles/4ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic DIP, PLCC or ZIP**

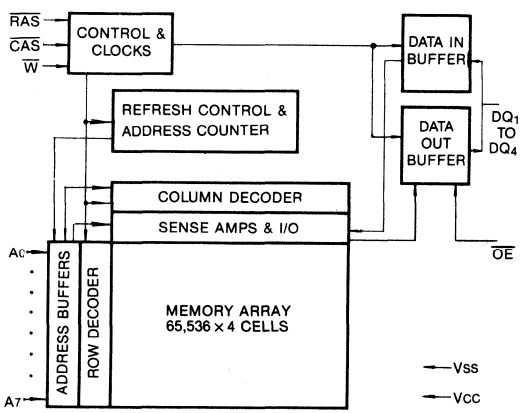
GENERAL DESCRIPTION

The Samsung KM41C464 is a CMOS high speed 65,536 bit x 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C464 features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs and fully TTL compatible.

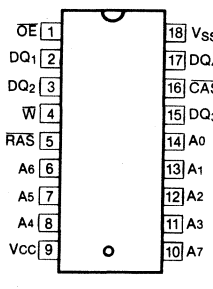
The KM41C464 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

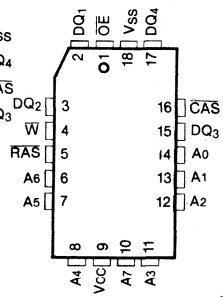


PIN CONFIGURATION (Top Views)

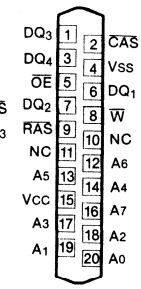
- **KM41C464P**



- **KM41C464J**



- **KM41C464Z**



Pin Name	Pin Function
A_0-A_7	Address Inputs
DQ_1-DQ_4	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

*Note: Permanent device damage may occur of "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC}=min.)	KM41C464-7	I_{CC1}	—	65	mA
	KM41C464-8		—	55	mA
	KM41C464-10		—	45	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling @t_{RC} = min.)	KM41C464-7	I_{CC3}	—	65	mA
	KM41C464-8		—	55	mA
	KM41C464-10		—	45	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC}=min.)	KM41C464-7	I_{CC4}	—	40	mA
	KM41C464-8		—	35	mA
	KM41C464-10		—	30	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min.)	KM41C464-7	I_{CC6}	—	65	mA
	KM41C464-8		—	55	mA
	KM41C464-10		—	45	mA
Input Leakage Current (Any input 0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0 ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

CAPACITANCE ($T_A = 25°C$)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_7)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{DQ}	—	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1, 2)

Parameter	Symbol	KM41C464-7		KM41C464-8		KM41C464-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	185		205		245		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	25	0	25	0	30	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	20	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		65		75		ns	6

STANDARD OPERATION (Continued)

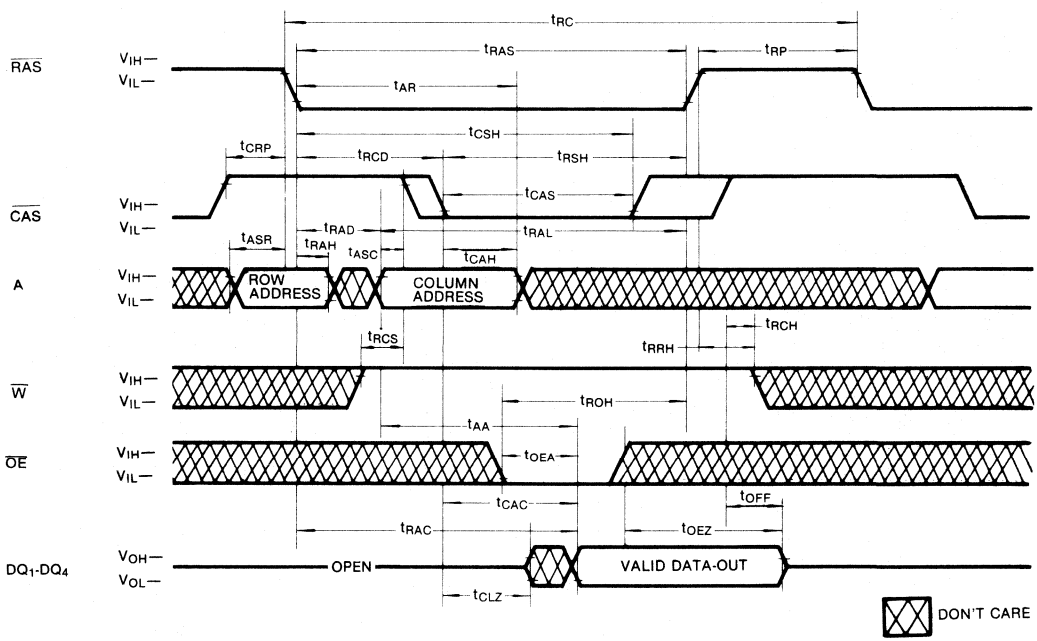
Parameter	Symbol	KM41C464-7		KM41C464-8		KM41C464-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	15		15		20		ns	10
Data hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (256 cycles)	t_{REF}		4		4		4	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	50		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	100		110		135		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	65		70		85		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$ Before $\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ Before $\overline{RAS}$ refresh)	t_{CHR}	20		25		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
Refresh counter test $\overline{CAS}$ precharge time	t_{CPT}	35		40		50		ns	
Fast Page mode cycle time	t_{PC}	45		50		60		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
Fast page mode read-modify-write	t_{PRWC}	100		105		125		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	15		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		20		25		ns	
Output buffer turn off delay $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures the t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} < t_{RWD}$(min) and $_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

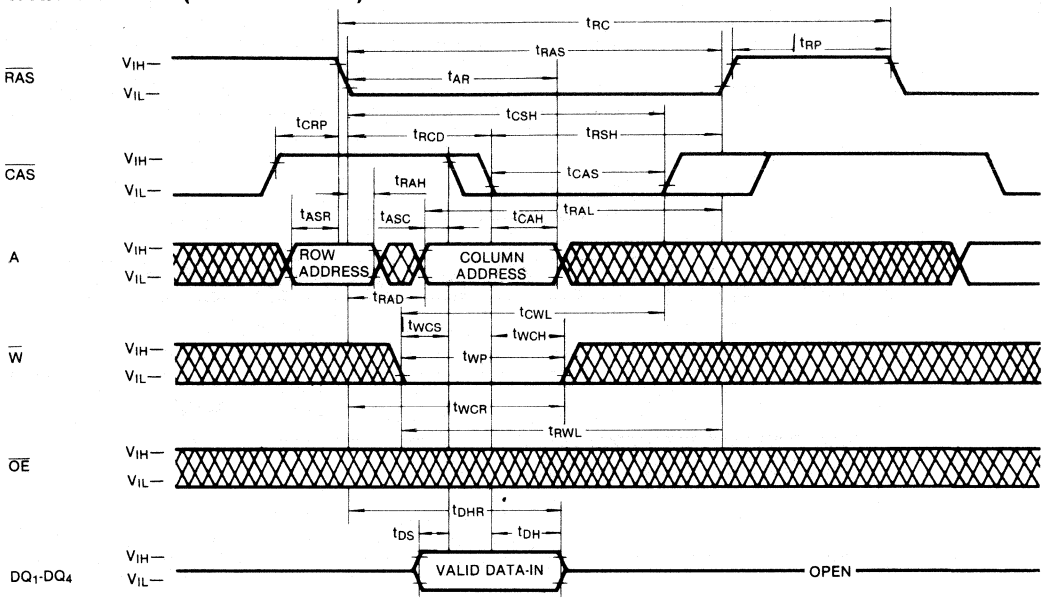
TIMING DIAGRAMS

READ CYCLE

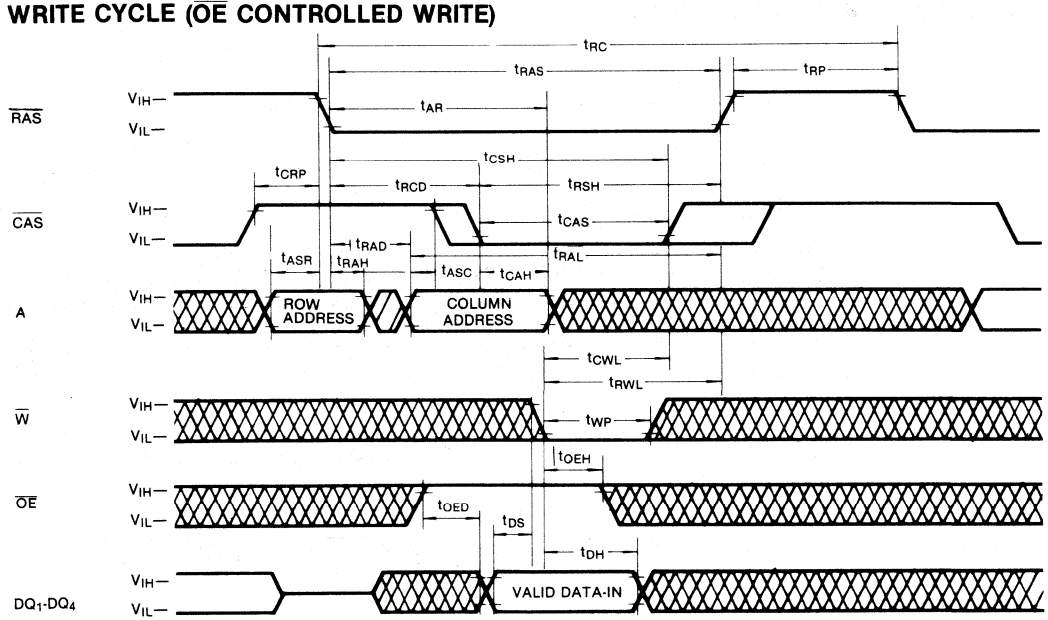


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

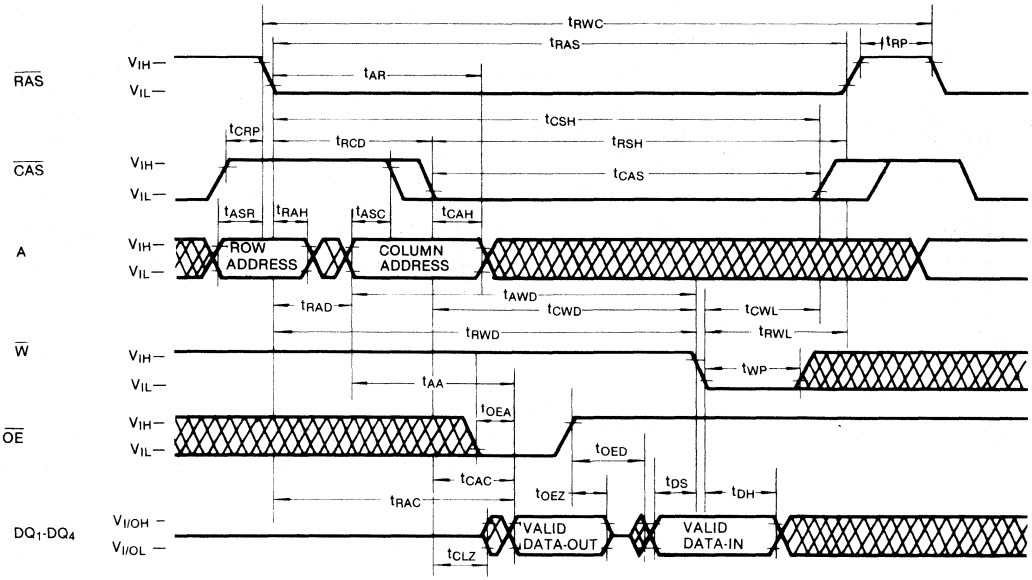


WRITE CYCLE (OE CONTROLLED WRITE)

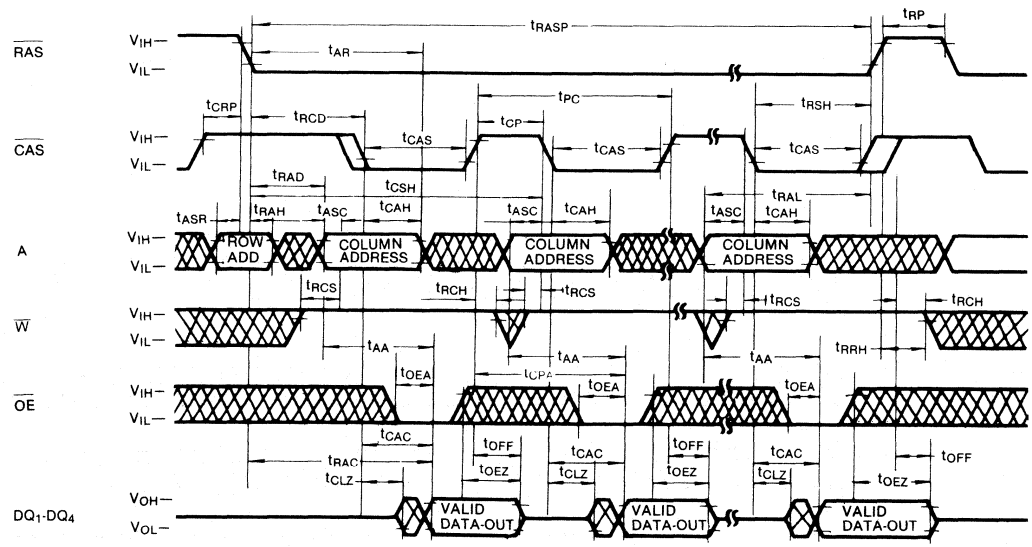


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



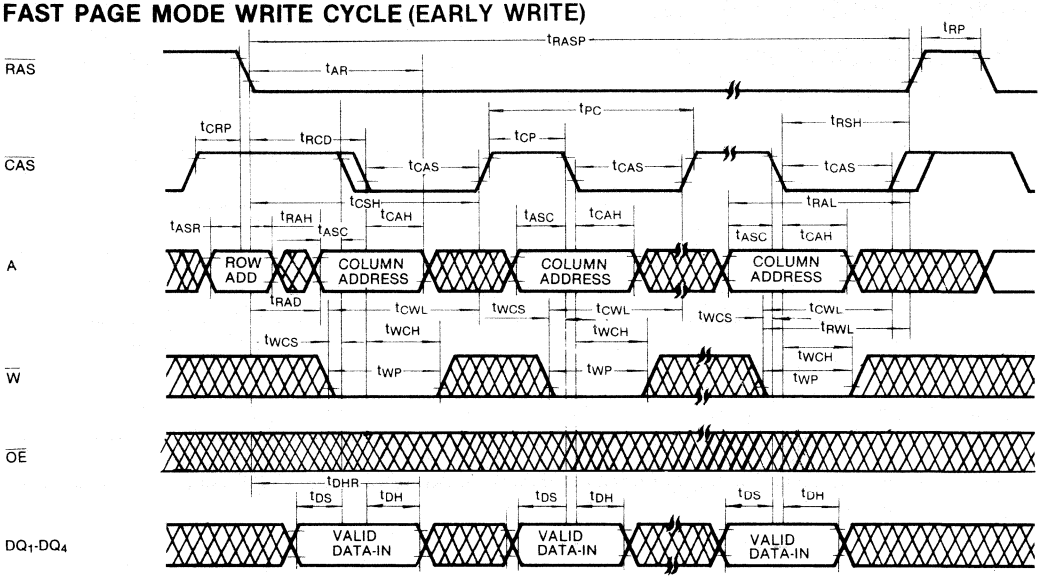
FAST PAGE MODE READ CYCLE



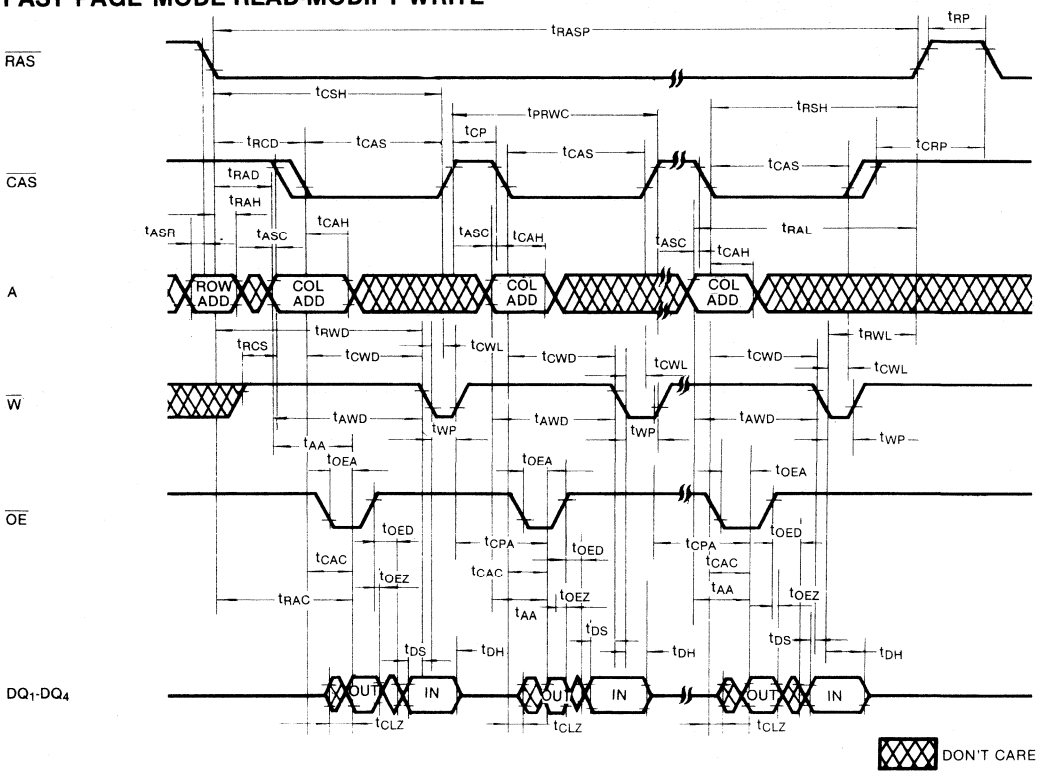
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



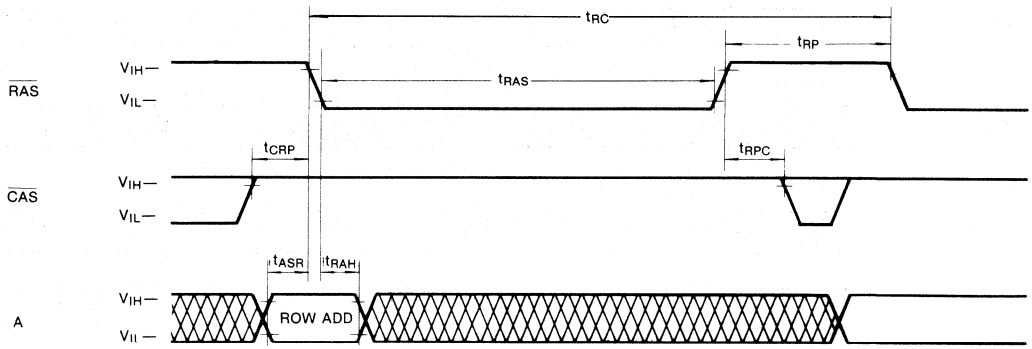
FAST PAGE MODE READ-MODIFY-WRITE



TIMING DIAGRAMS (Continued)

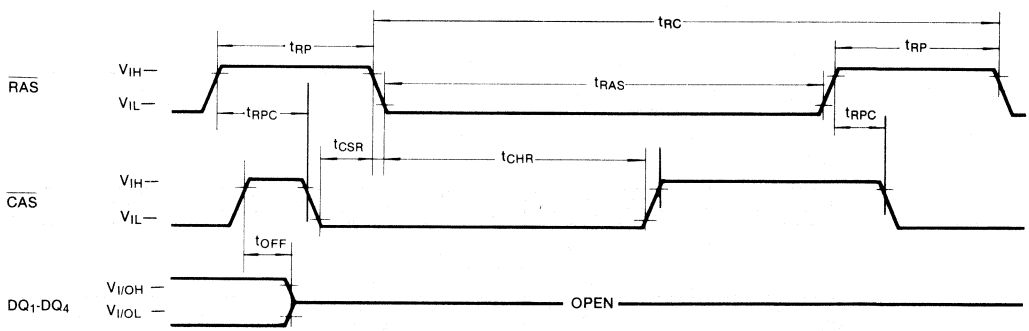
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

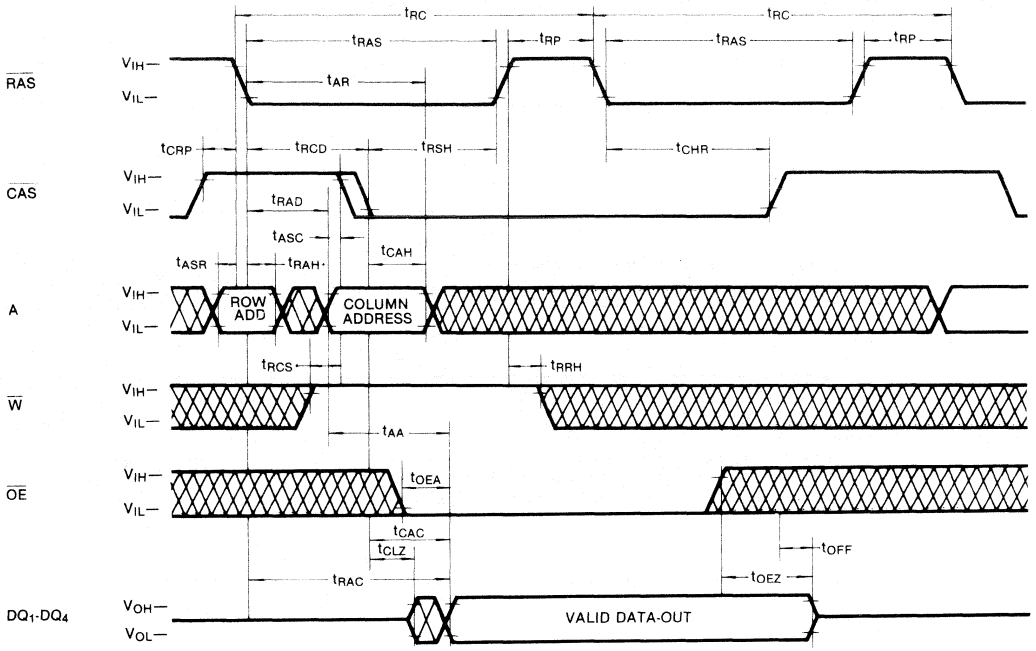
Note: $\overline{W}$, $\overline{OE}$, A = Don't care



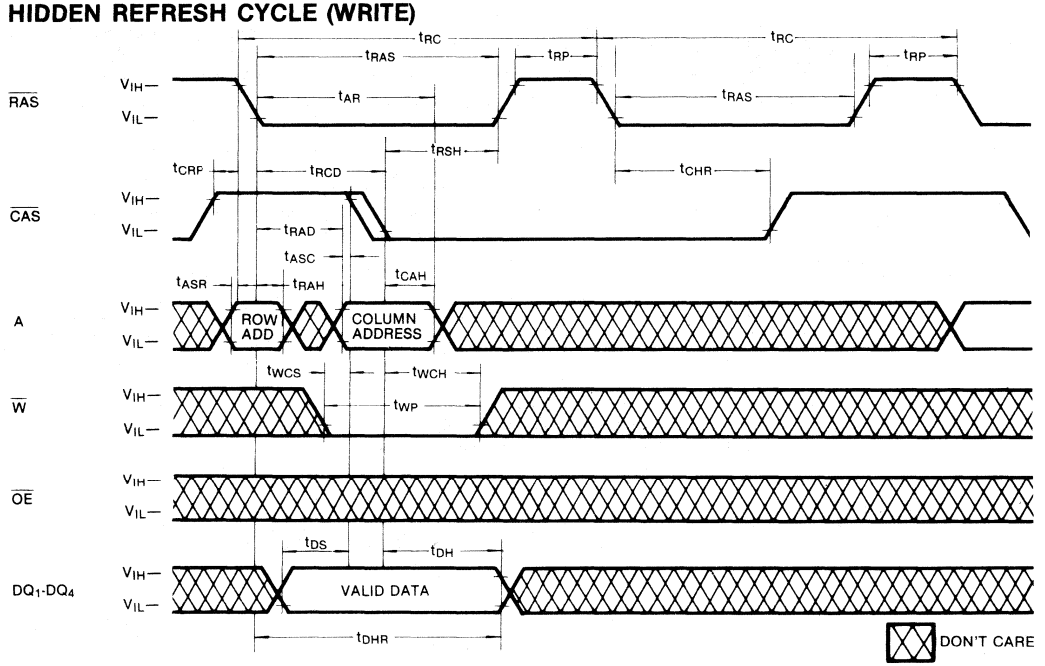
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

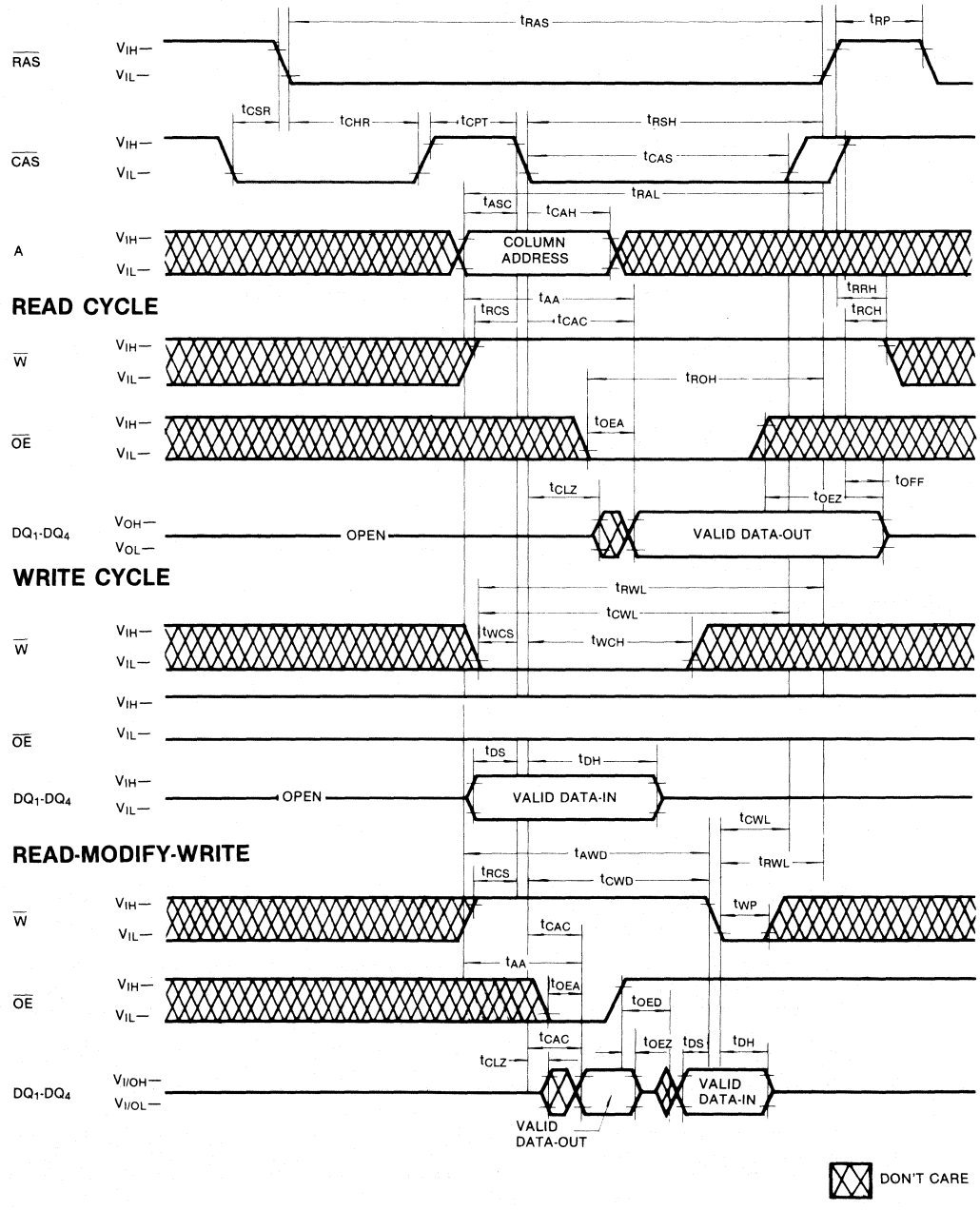


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM41C464 contains 262,144 memory locations organized as 65,536 four-bit words. Sixteen address bits are required to address a particular 4-bit word in the memory array. Since the KM41C464 has only 8 address input pins, time multiplexed addressing is used to input 8 row and 8 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the KM41C464 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 8 address input pins is changed from a row address to a column address and is strobed in by CAS. This is the beginning of any KM41C464 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C464 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

The KM41C464 has common data I/O pins. For this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to apppear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OFZ}.

Write

The KM41C464 can perform early write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CAS}$. In any type of write cycle Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the outputs remain in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cells appears at the outputs before and during the time that data is being written into the same cell locations. This cycle is achieved by bringing W low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The output enable input ($\overline{OE}$) must be low during the time defined by t_{OEA} and t_{OEZ} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met the output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM41C464's DQ pins.

Data Output

The KM41C464 has a three-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. When either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}) the output are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C464 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} are not met)

Refresh

The data in the KM41C464 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 4 ms. Either a burst refresh or distributed refresh may be

DEVICE OPERATION (Continued)

used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 256 row addresses, (A_0-A_7).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C464 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C464 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C464 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

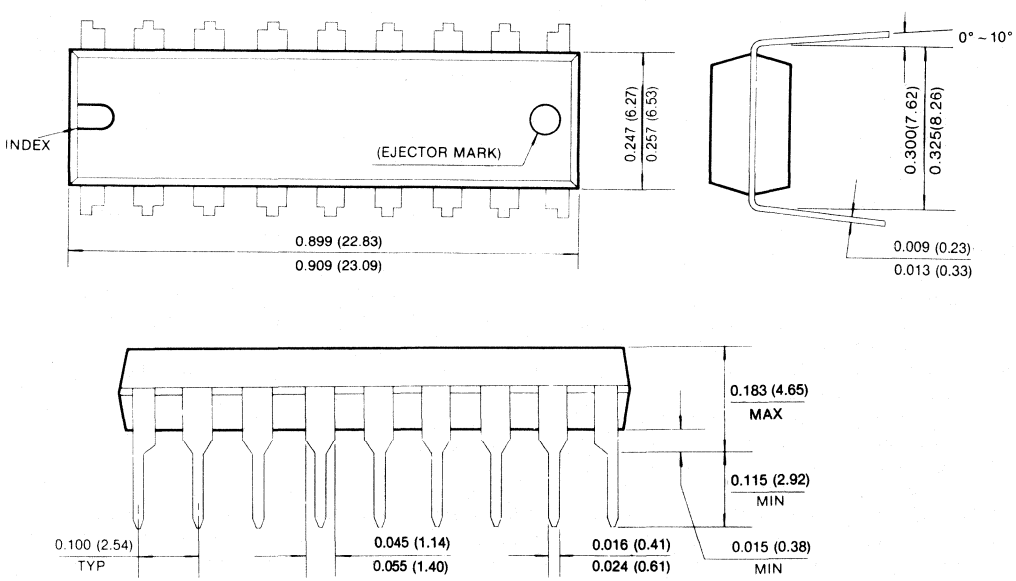
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A_0 through A_7 are supplied by the on-chip refresh counter.

PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

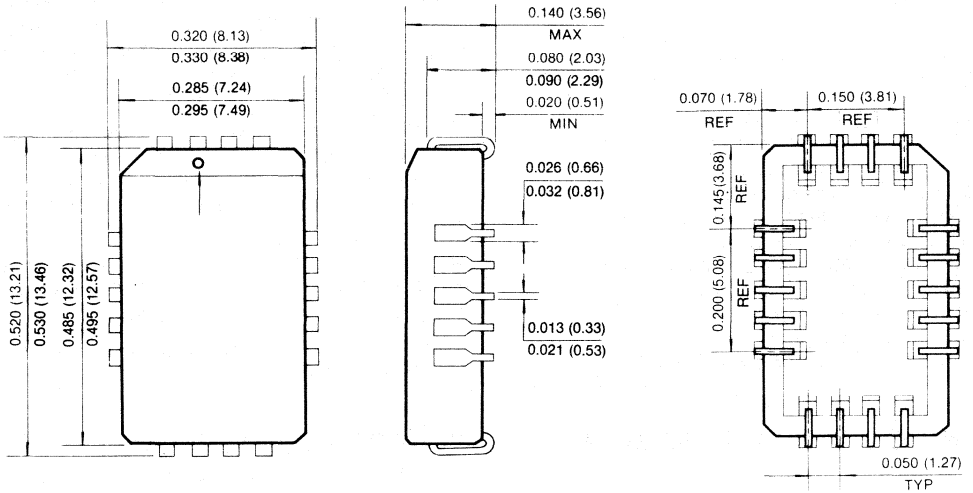
Units: Inches (millimeters)



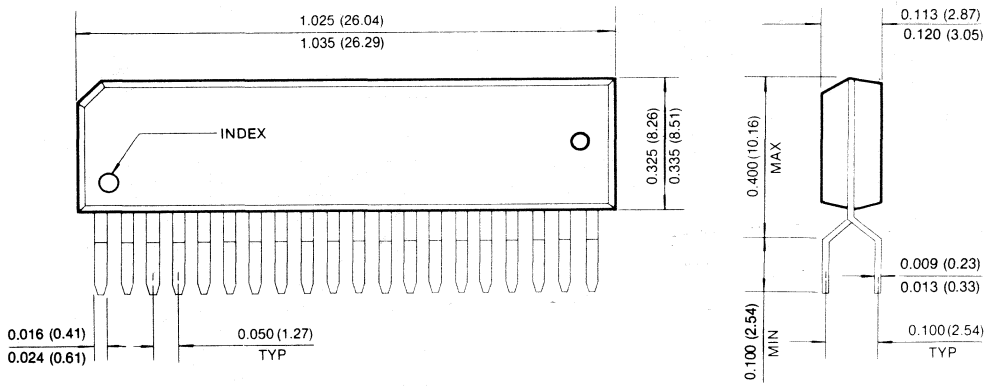
PACKAGE DIMENSIONS (Continued)

18-PIN PLASTIC LEADED CHIP CARRIER

Units: Inches (Millimeters)



20-PIN PLASTIC ZIGZAG-IN-LINE PACKAGE



64K x 4 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C466-7	70ns	20ns	130ns
KM41C466-8	80ns	20ns	150ns
KM41C466-10	100ns	25ns	180ns

- **Static Column Mode operation**
- **$\overline{CS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and output**
- **Early write or Output Enable Controlled Write**
- **Single +5V ± 10% power supply**
- **256 cycles/4ms refresh**
- **JEDEC standard pinout**
- **A vailable in Plastic DIP, PLCC or ZIP**

GENERAL DESCRIPTION

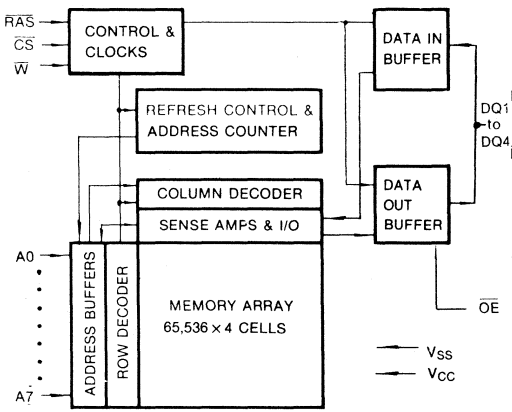
The Samsung KM41C466 is a CMOS high speed 65,536 bit x 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C466 features Static Column Mode operation which allows high speed random or sequential access within a row. Static Column Mode operation offers high performance while relaxing many critical system timing requirements for fast usable speed.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

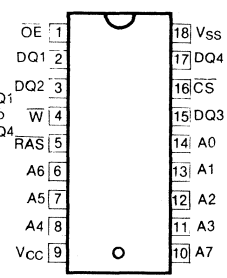
The KM41C466 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

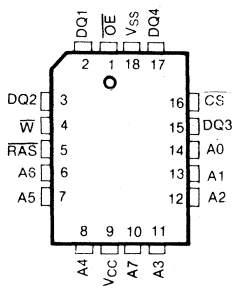


PIN CONFIGURATION (Top Views)

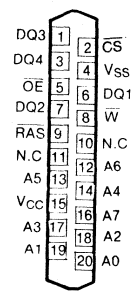
- **KM41C466P**



- **KM41C466J**



- **KM41C466Z**



Pin Name	Pin Function
A_0-A_7	Address Inputs
DQ_1-DQ_4	Data In/Data Output
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

*Note: Permanent device damage may occur of "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CS}$, Address Cycling @t_{PC} = min.)	KM41C466-7	I_{CC1}	—	65	mA
	KM41C466-8		—	55	mA
	KM41C466-10		—	45	mA
Standby Current ($\overline{RAS}$ = $\overline{CS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CS}$=V_{IH}, $\overline{RAS}$, Cycling @t_{RC}=min.)	KM41C466-7	I_{CC3}	—	65	mA
	KM41C466-8		—	55	mA
	KM41C466-10		—	45	mA
Static Column Mode Current* ($\overline{RAS}$ = $\overline{CS}$ = V_{IL}, Address Cycling: t_{SC}=min.)	KM41C466-7	I_{CC4}	—	40	mA
	KM41C466-8		—	35	mA
	KM41C466-10		—	30	mA
Standby Current ($\overline{RAS}$ = $\overline{CS}$ = V_{CC} − 0.2V)		I_{CC5}	—	1	mA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{RC} = min.)	KM41C466-7	I_{CC6}	—	65	mA
	KM41C466-8		—	55	mA
	KM41C466-10		—	45	mA
Input Leakage Current (Any input 0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0 ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

CAPACITANCE ($T_A = 25°C$)

Item	Symbol	Min	Max	Unit
Input capacitance (A_0-A_7)	C_{IN1}	—	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{OUT}	—	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1, 2)

Standard Operation	Symbol	KM41C466-7		KM41C466-8		KM41C466-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	185		205		245		ns	
Static column Mode Cycle Time	t_{SC}	40		45		55		ns	
Static column Mode Read-Write Cycle Time	t_{SRWC}	100		110		135		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
Access time from last write	t_{ALW}		65		75		95	ns	3,12
$\overline{CS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay time	t_{OFF}	0	25	0	25	0	30	ns	7
Output data hold time from column address	t_{AOH}	5		5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		45		50		70	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width (static column mode)	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	
$\overline{CS}$ to $\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{RAS}$ to $\overline{CS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CS}$ pulse width	t_{CS}	20	10,000	20	10,000	25	20,000	ns	
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	20	100,000	20	100,000	25	100,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	20	40	20	50	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
$\overline{CS}$ precharge time (static column mode)	t_{CP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		20		ns	
Write address hold time referenced to $\overline{RAS}$	t_{AWR}	55		65		75		ns	6
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	85		95		115		ns	

AC CHARACTERISTICS (Continued)

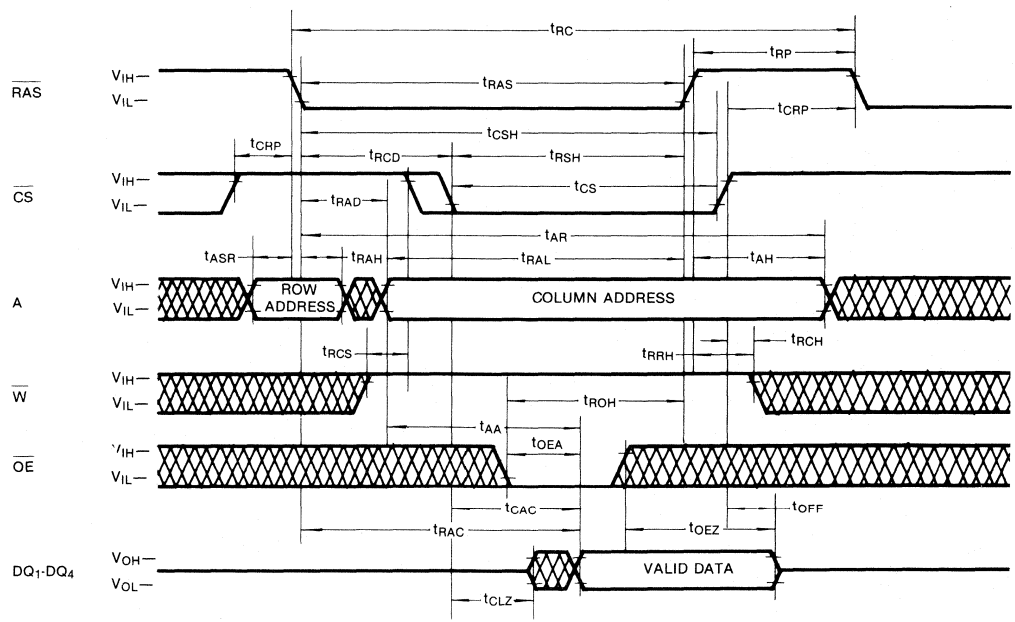
Standard Operation	Symbol	KM41C466-7		KM41C466-8		KM41C466-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Column Address hold time referenced to $\overline{RAS}$ rise	t_{AH}	10		10		10		ns	
Last write to column address delay time	t_{LWAD}	20	30	25	35	25	45	ns	
Last write to column address hold time	t_{AHLW}	65		75		95		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		20		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		65		75		ns	6
Write command pulse width	t_{WP}	15		20		20		ns	
Write command inactive time	t_{WI}	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		20		20		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		65		75		ns	6
Refresh period (256 cycles)	t_{REF}		4		4		4	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CS}$ to $\overline{W}$ delay time (read modify write cycle)	t_{CWD}	50		50		60		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time (read modify write cycle)	t_{RWD}	100		110		135		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	65		70		85		ns	8
$\overline{CS}$ setup time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ to $\overline{CS}$ precharge time	t_{RPC}	10		10		10		ns	
$\overline{CS}$ precharge time	t_{CPT}	35		40		50		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AWR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defineds the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is in-determinate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. Operation within the t_{LWAD}(max) limit insures that t_{ALW}(max) can be met. t_{LWAD}(max) is specified as a reference point only. If t_{LWAD} is greater than the specified t_{LWAD}(max) limit, then access time is controlled by t_{AA}.

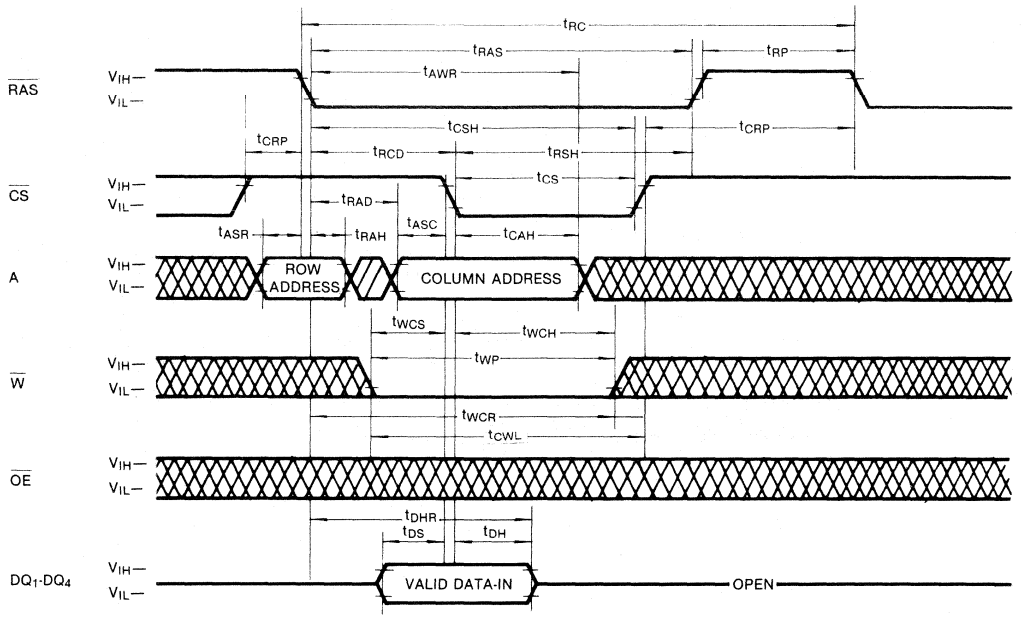
TIMING DIAGRAMS (Continued)

READ CYCLE

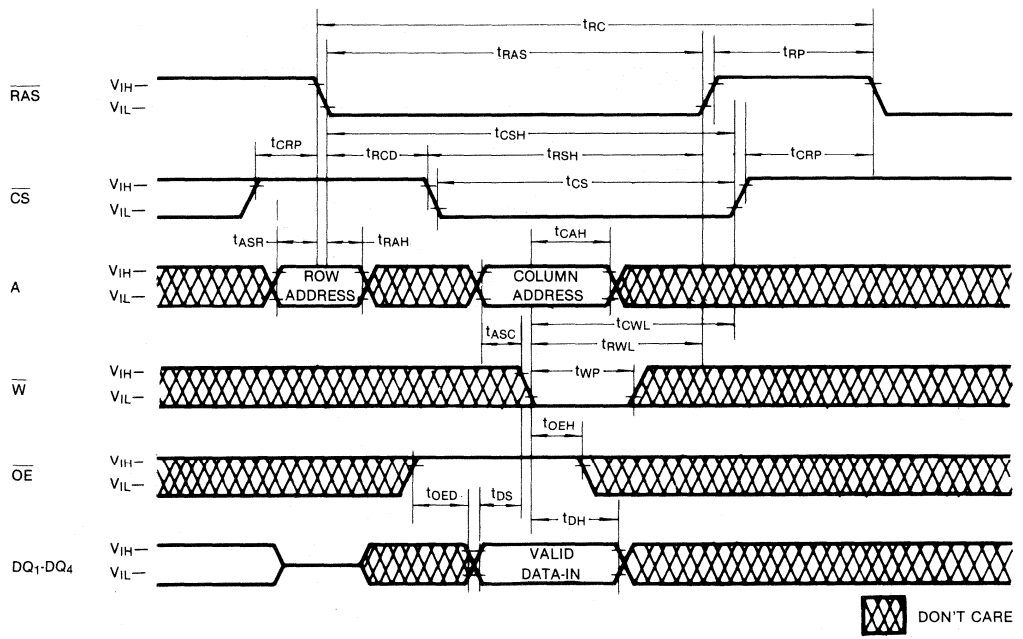


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

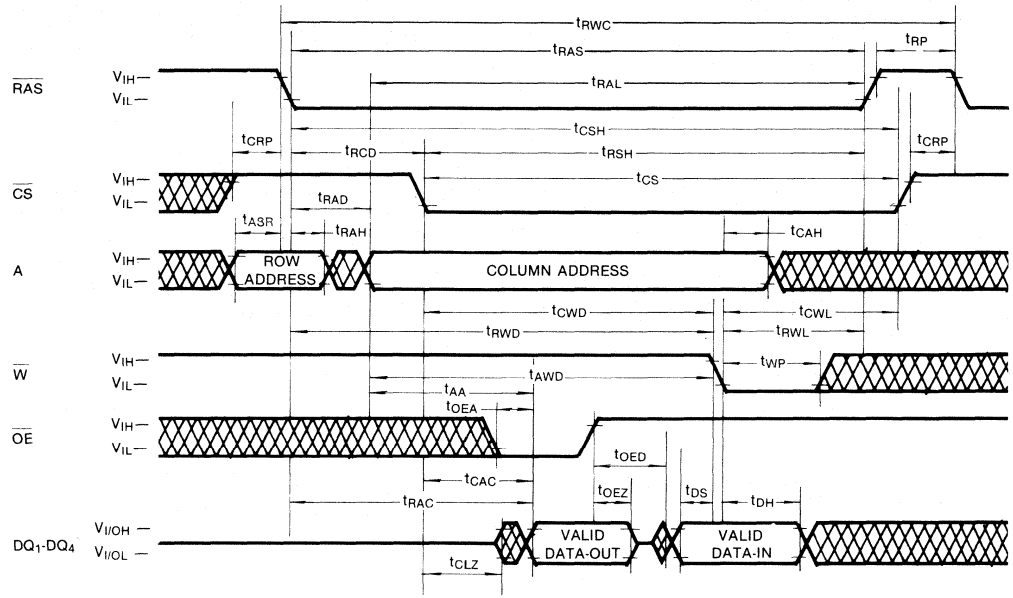


WRITE CYCLE (OE CONTROLLED WRITE)

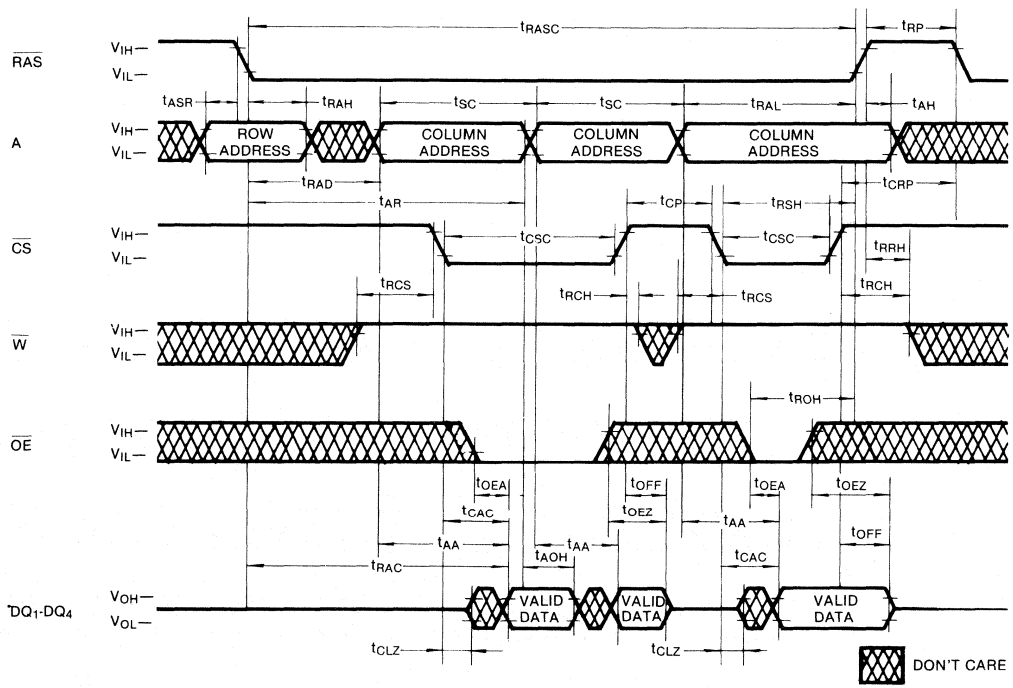


TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

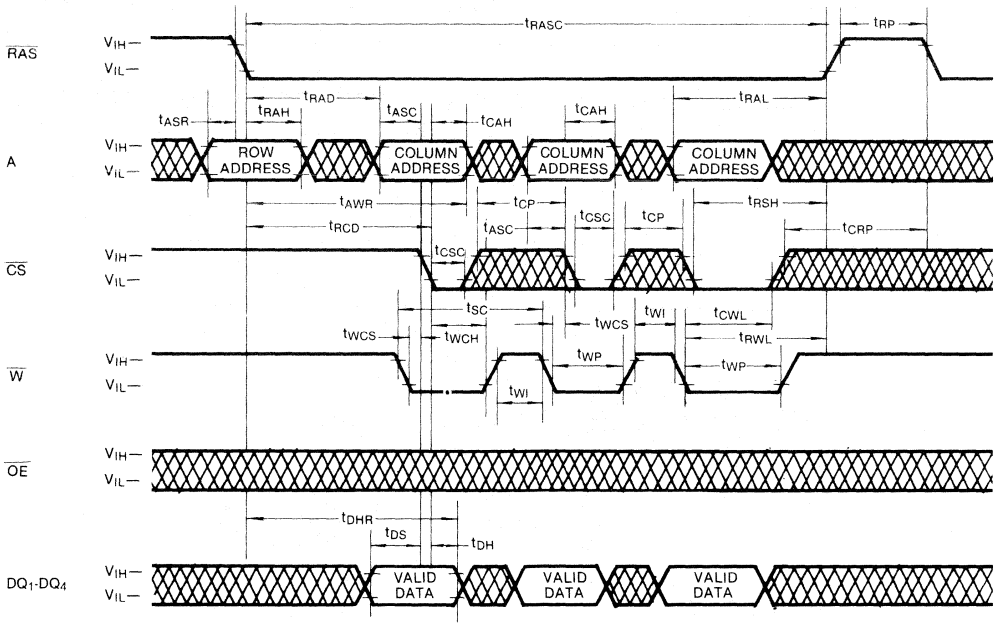


STATIC COLUMN MODE READ CYCLE

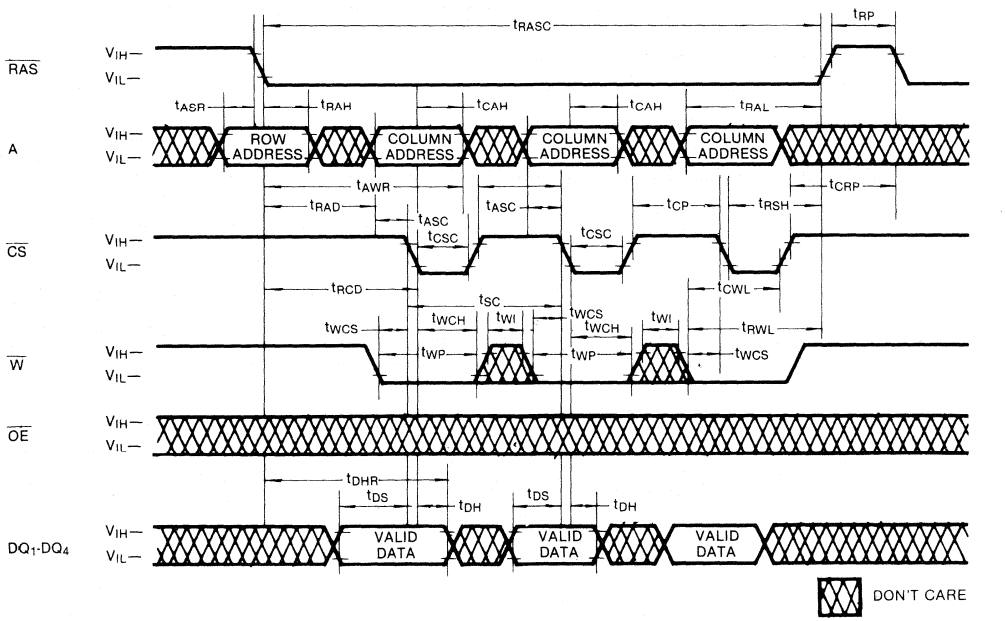


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ controlled early write)

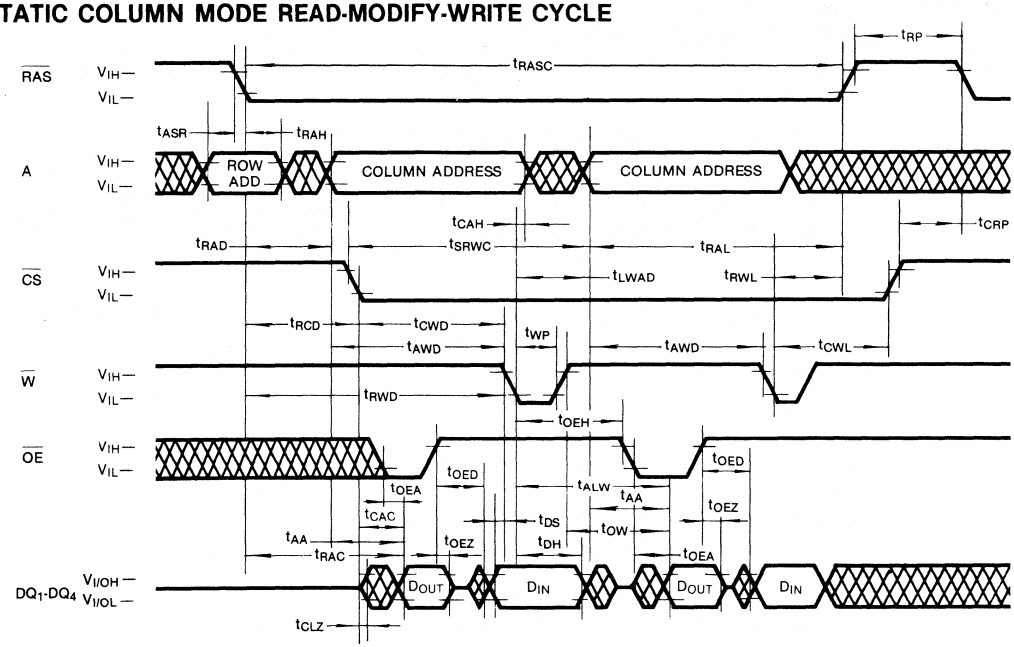


STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ controlled early write)

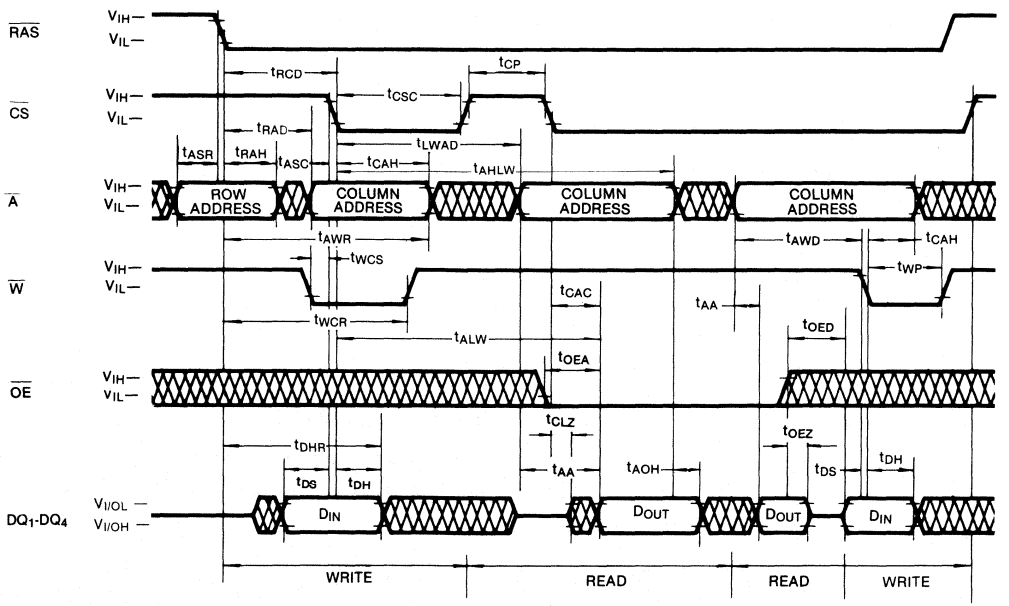


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



STATIC COLUMN MODE MIXED CYCLE

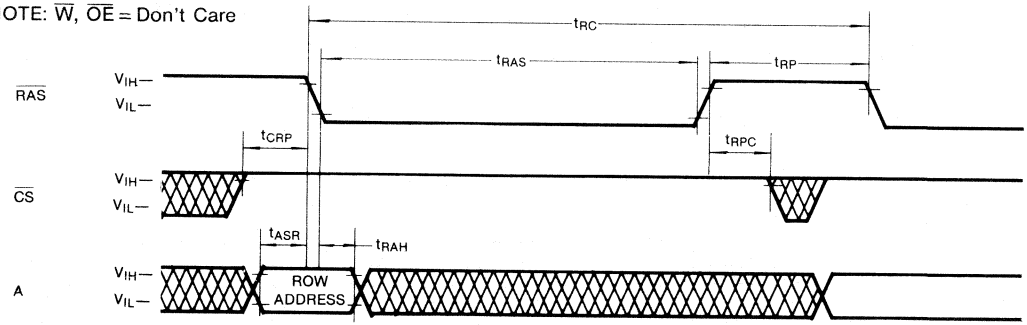


DON'T CARE

TIMING DIAGRAMS (Continued)

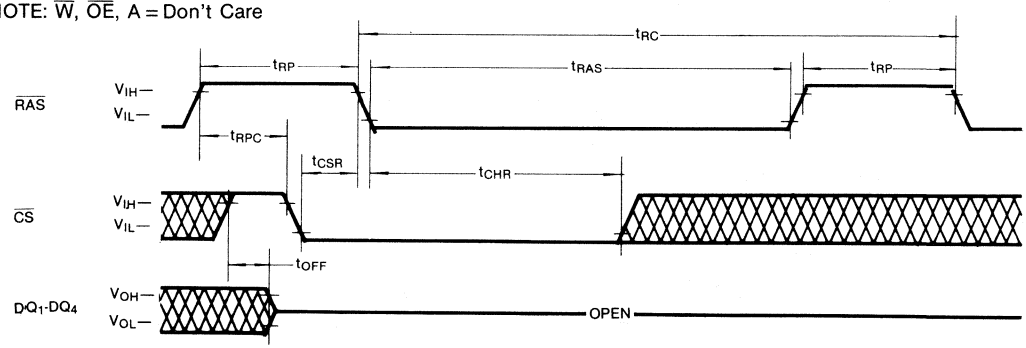
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$ = Don't Care



$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

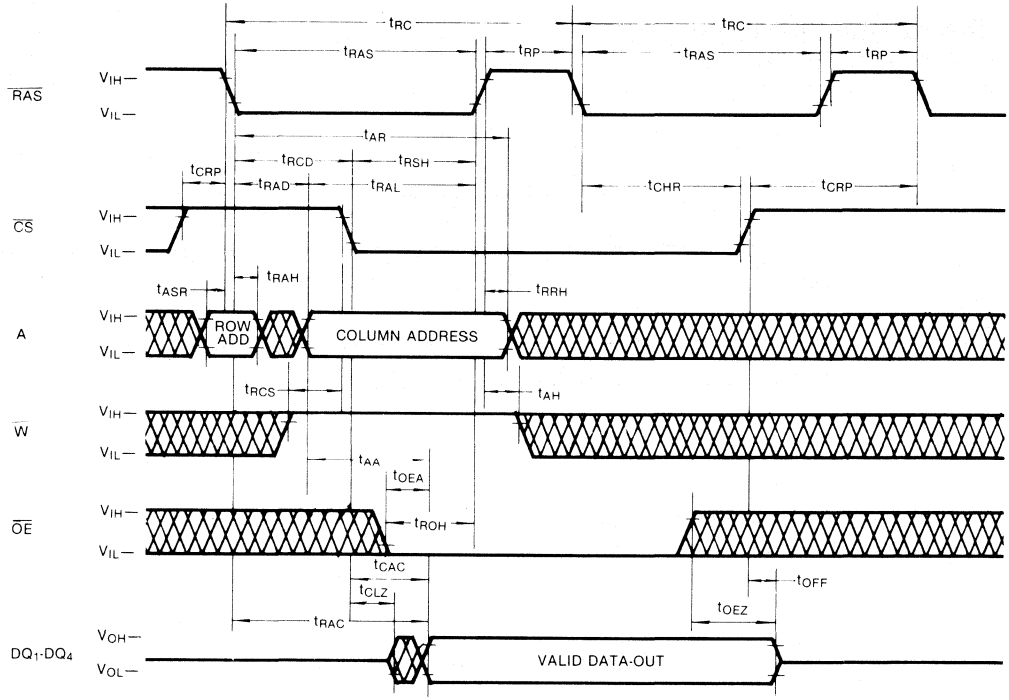
NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care



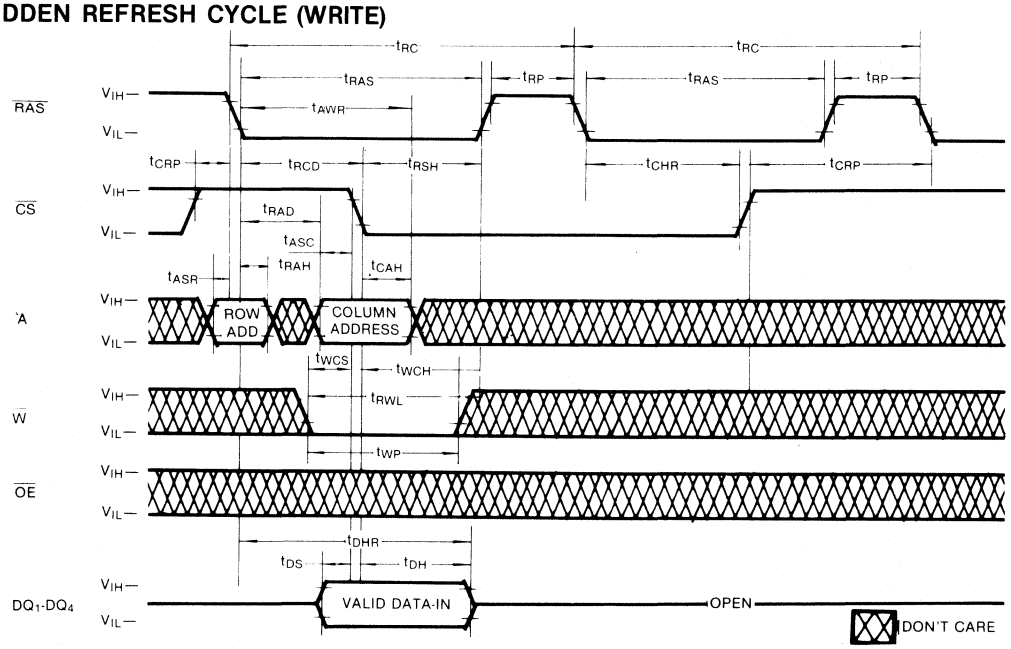
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

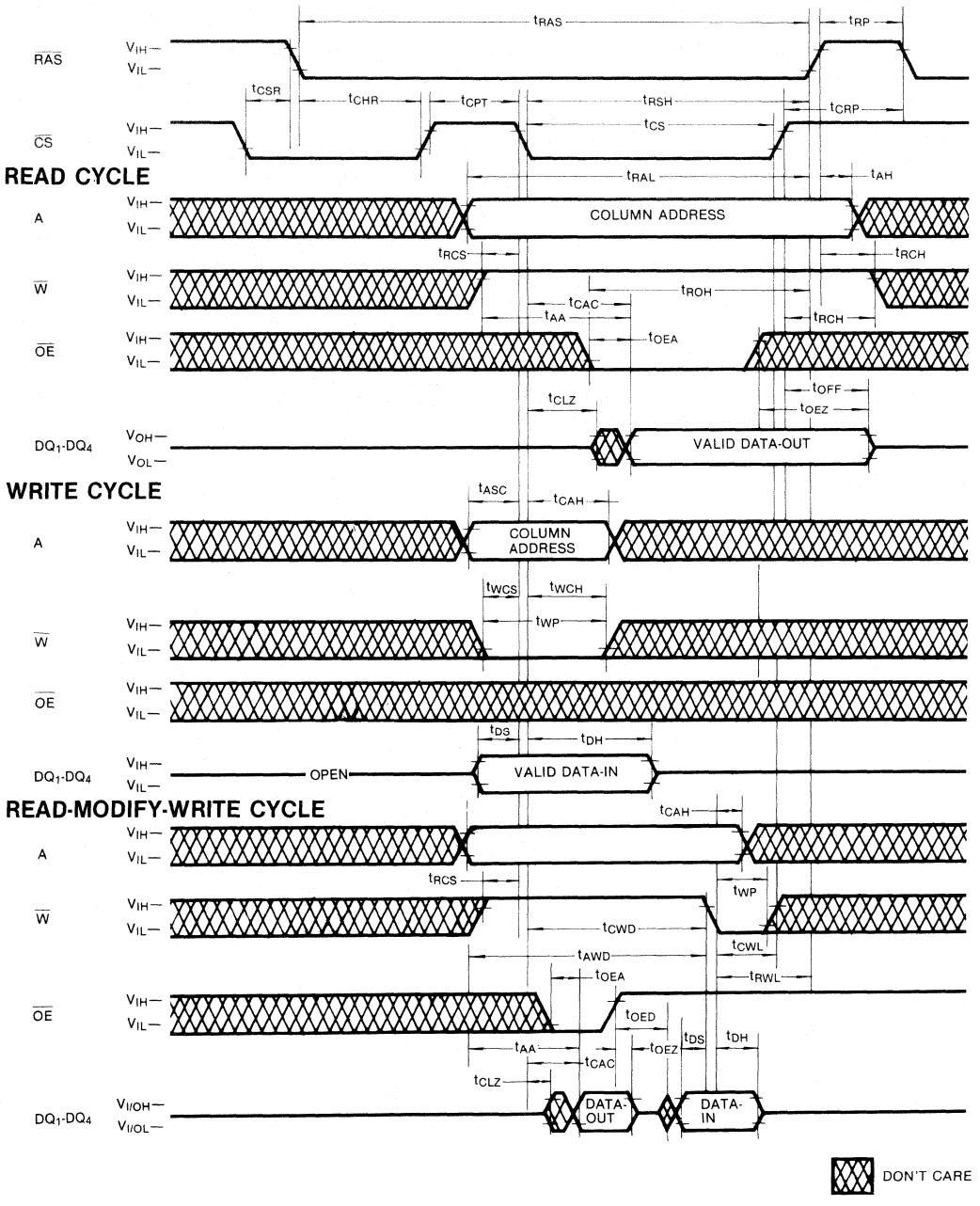


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM41C466 contains 262,114 memory locations. Sixteen address bits are required to address a particular memory location. Since the KM41C466 has only 8 address input pins, time multiplexed addressing is used to input 8 row and 8 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the chip select input ($\overline{CS}$) and the valid row and column address inputs.

Operation of the KM41C466 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CS}$ remains high. Then the address on the 8 address input pins is changed from a row address to a column address and is strobed in by $\overline{CS}$. This is the beginning of any KM41C466 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths are specified by t_{RAS}(min) and t_{CS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C466 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CS}$ cycle. The access time is nomally specified with respect to the falling edge $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CS}$ and on the vallid column address transition.

If $\overline{CS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM41C466 can perform early write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CS}$. In any type of write cycle Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the outputs remain in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cells appears at the outputs before and during the time that data is being written into the same cell locations. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CS}$ and meeting the data sheet read-modify-write cycle timing requirements. The output enable input $\overline{OE}$ must be low during the time defined by t_{OEA} and t_{OEZ} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met the output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM41C466's DQ pins.

Data Output

The KM41C466 has a three-state output buffers which are controlled by $\overline{CS}$ and $\overline{OE}$. When either $\overline{CS}$ or $\overline{OE}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C466 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Static Column Mode Read, Static Column Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Static Column Mode Write, $\overline{CS}$-before-$\overline{RAS}$ Refresh, $\overline{CS}$-only cycle.

Indeterminate Output State: Delayed Write

DEVICE OPERATION (Continued)

Refresh

The data in the KM41C466 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 4 ms. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CS}$ remains high. This cycle must be repeated for each of the 256 row addresses, (A_0-A_7).

$\overline{CS}$-before-RAS Refresh: The KM41C466 has $\overline{CS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CS}$ active time and cycling $\overline{RAS}$. The KM41C466 hidden refresh cycle is actually a $\overline{CS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C466 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CS}$-before-$\overline{RAS}$ refresh is the preferred method.

Static Column Mode

Static Column mode allows high speed read, write or read-modify-write access to all the memory cells within a selected row. Operation within a selected row is similar to a static RAM. The read, write or read-modify-write cycles may be mixed in any order.

A Static Column mode read cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{W} = V_{IH}$ and $\overline{RAS} = V_{IL}$.

A Static Column mode write cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{RAS} = V_{IL}$ and toggling either $\overline{W}$ or $\overline{CS}$. The data is written into the cell triggered by the latter falling edge to $\overline{W}$ or $\overline{CS}$.

$\overline{CS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 8 row address bits and 8 column address bits defined as follows:

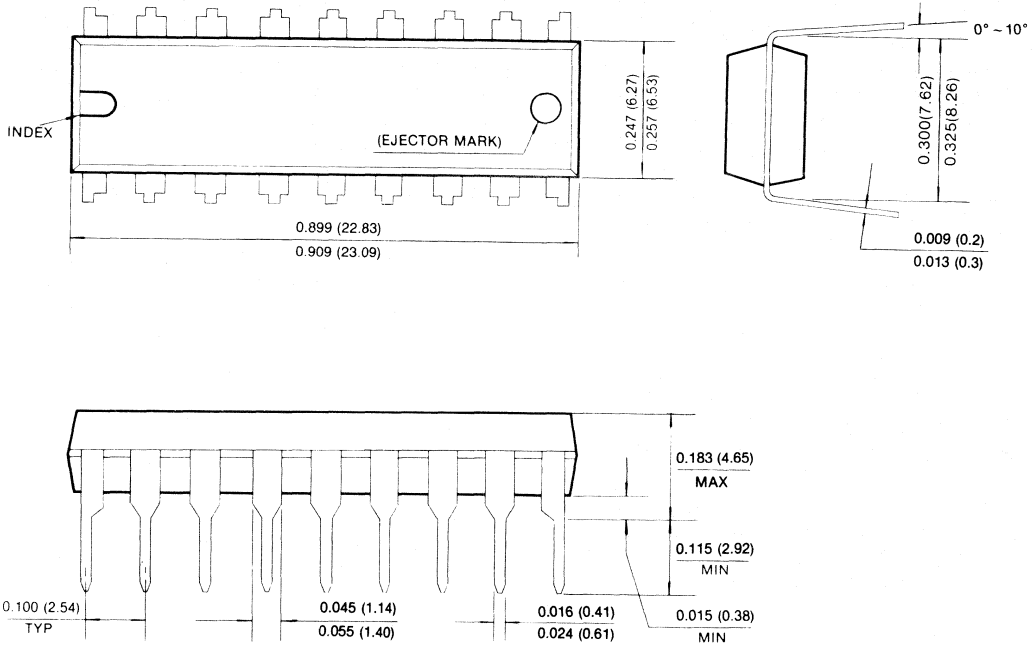
Row Address—Bits A_0 through A_7 are supplied by the on-chip refresh counter.

Column Address—Bits A_0 through A_7 are strobed-in by the falling edge of $\overline{CS}$ as in a normal memory cycle.

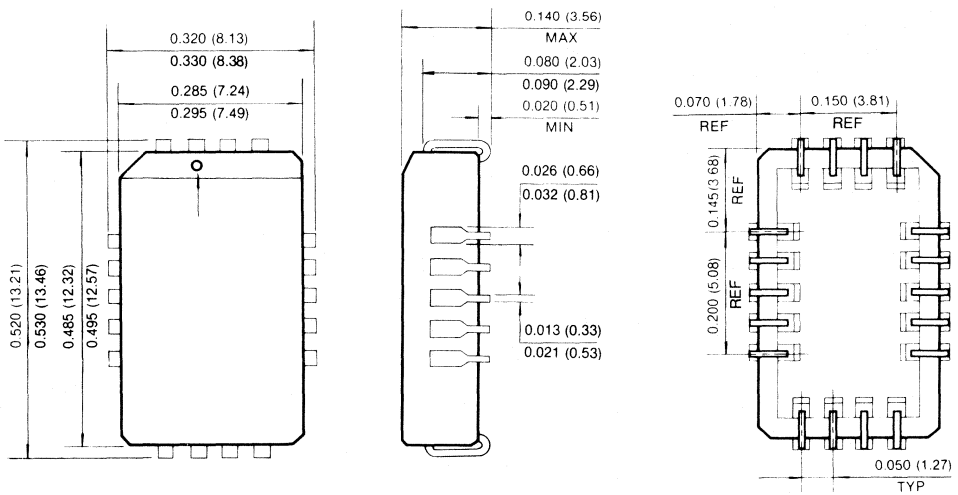
PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (millimeters)



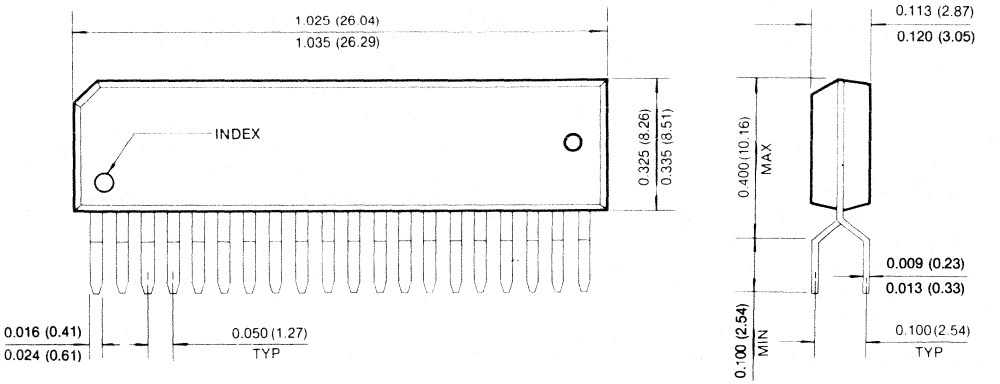
18- LEAD PLASTIC CHIP CARRIER



PACKAGE DIMENSIONS (Continued)

20-PIN PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)



1M×1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C1000C-6	60ns	15ns	110ns
KM41C1000C-7	70ns	20ns	130ns
KM41C1000C-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible input and output**
- **Single +5V ± 10% power supply**
- **512 cycles/8ms refresh**
- **256K×4 fast test mode**
- **JEDEC Standard pinout available in Plastic DIP, SOJ, ZIP, TSOP (I), TSOP (II) packages.**

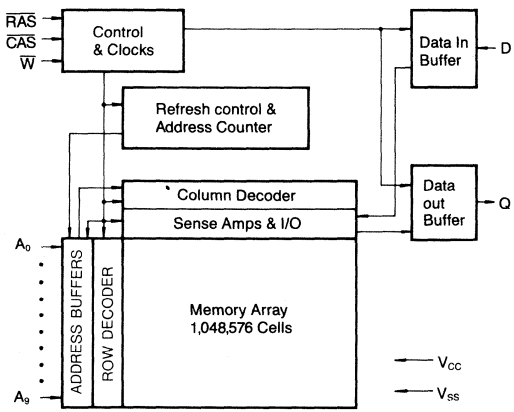
GENERAL DESCRIPTION

The Samsung KM41C1000C is a CMOS high speed 1,048,576×1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance microprocessor computers.

The KM41C1000C features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM41C1000C is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

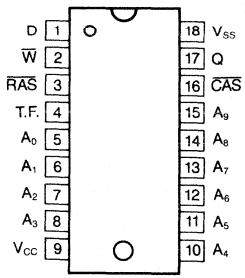


ORDERING INFORMATION

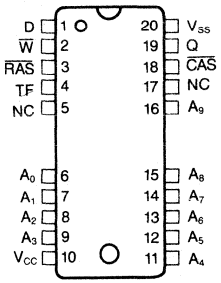
Part No.	Access Time	Package
KM41C1000CP-6	60ns	300 mil, 18DIP
KM41C1000CP-7	70ns	
KM41C1000CP-8	80ns	
KM41C1000CJ-6	60ns	300 mil, 20SOJ
KM41C1000CJ-7	70ns	
KM41C1000CJ-8	80ns	
KM41C1000CZ-6	60ns	400 mil, 20ZIP
KM41C1000CZ-7	70ns	
KM41C1000CZ-8	80ns	
KM41C1000CV-6	60ns	20 TOSP (I) (Forward)
KM41C1000CV-7	70ns	
KM41C1000CV-8	80ns	
KM41C1000CVR-6	60ns	20 TOSP (I) (Reverse)
KM41C1000CVR-7	70ns	
KM41C1000CVR-8	80ns	
KM41C1000CT-6	60ns	20 TOSP (II) (Forward)
KM41C1000CT-7	70ns	
KM41C1000CT-8	80ns	
KM41C1000CTR-6	60ns	20 TOSP (II) (Reverse)
KM41C1000CTR-7	70ns	
KM41C1000CTR-8	80ns	

PIN CONFIGURATION (Top Views)

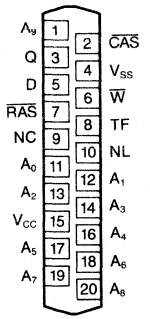
• KM41C1000CP



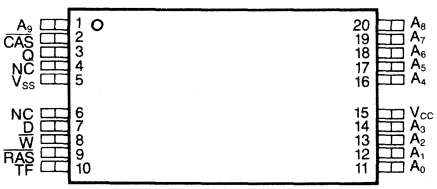
• KM41C1000CJ



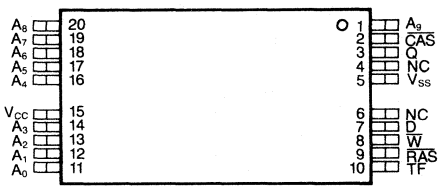
• KM41C1000CZ



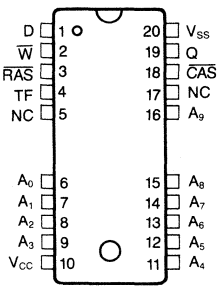
• KM41C1000CV



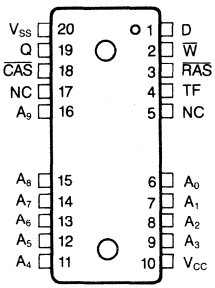
• KM41C1000CVR



• KM41C1000CT



• KM41C1000CTR



Pin Names	Pin Function
A_0-A_9	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
TF	Test Function
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection
NL	No Lead

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, and $\overline{CAS}$, Address Cycling @ t_{RC}=min.)	KM41C1000C-6	I_{CC1}	—	70	mA
	KM41C1000C-7		—	65	mA
	KM41C1000C-8		—	60	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @ t_{RC}=min.)	KM41C1000C-6	I_{CC3}	—	70	mA
	KM41C1000C-7		—	65	mA
	KM41C1000C-8		—	60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @ t_{PC}=min.)	KM41C1000C-6	I_{CC4}	—	55	mA
	KM41C1000C-7		—	50	mA
	KM41C1000C-8		—	45	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC}-0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ cycling @ t_{RC}=min.)	KM41C1000C-6	I_{CC6}	—	70	mA
	KM41C1000C-7		—	65	mA
	KM41C1000C-8		—	60	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3} Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A =25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance [D]	C_{IN1}	—	5	pF
Input Capacitance [A_0-A_9]	C_{IN1}	—	6	pF
Input Capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$]	C_{IN3}	—	7	pF
Output Capacitance [Q]	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC} =5.0V ± 10%, See notes 1, 2)

Parameter	Symbol	KM41C1000C-6		KM41C1000C-7		KM41C1000C-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	130		150		170		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3, 4, 11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3, 4, 5
Access time from column address	t_{AA}		30		35		40	ns	3, 10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	

AC CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$, See notes 1, 2)

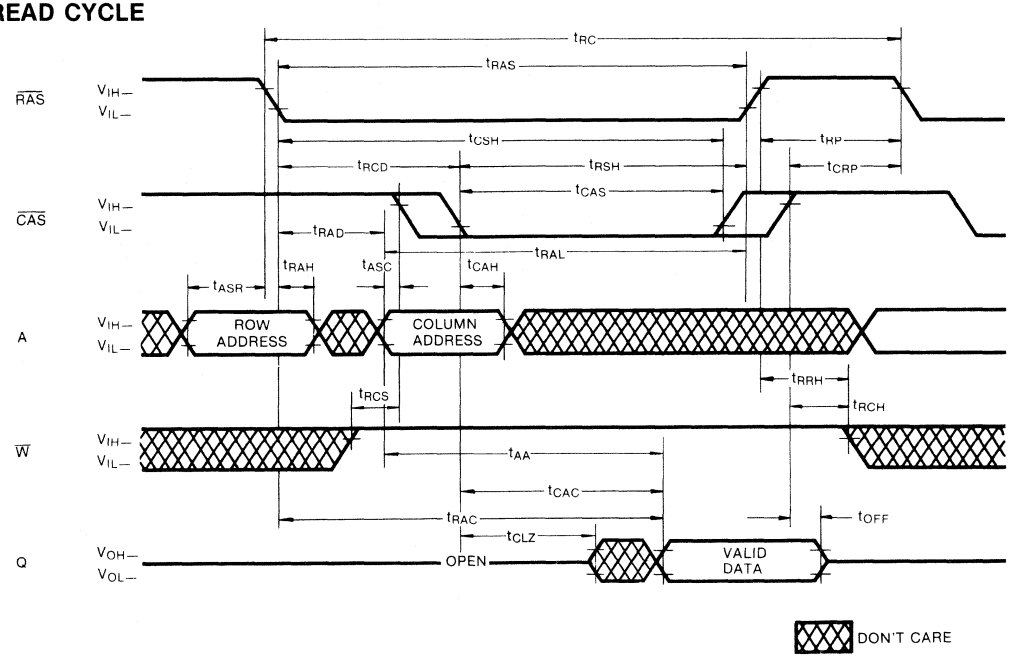
Parameter	Symbol	KM41C1000C-6		KM41C1000C-7		KM41C1000C-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		50		55		ns	6
Write command pulse width	t_{WP}	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (512 cycles)	t_{REF}		8		8		8	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	15		20		20		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	60		70		80		ns	8
Column address to $\overline{W}$ dealy time	t_{AWD}	30		35		40		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	15		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		35		40	ns	3
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	60		60		65		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
12. Normal operation requires the "T.F" pin to be connected to V_{SS} or TTL logic low level or left unconnected on the printed wiring board.
13. When the "T.F" pin is connected to a defined positive voltage, the internal test function may be activated. Contact Samsung for specific operational details of the "test function."
14. In a test mode read cycle, the value of t_{RAC}, t_{CAC}, t_{AA} is delayed for 3ns.

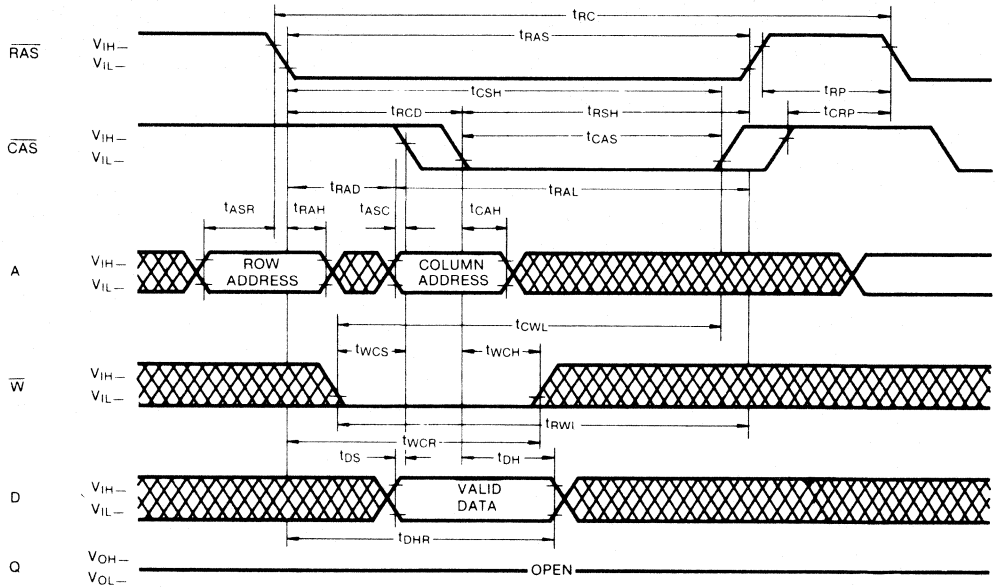
TIMING DIAGRAMS

READ CYCLE

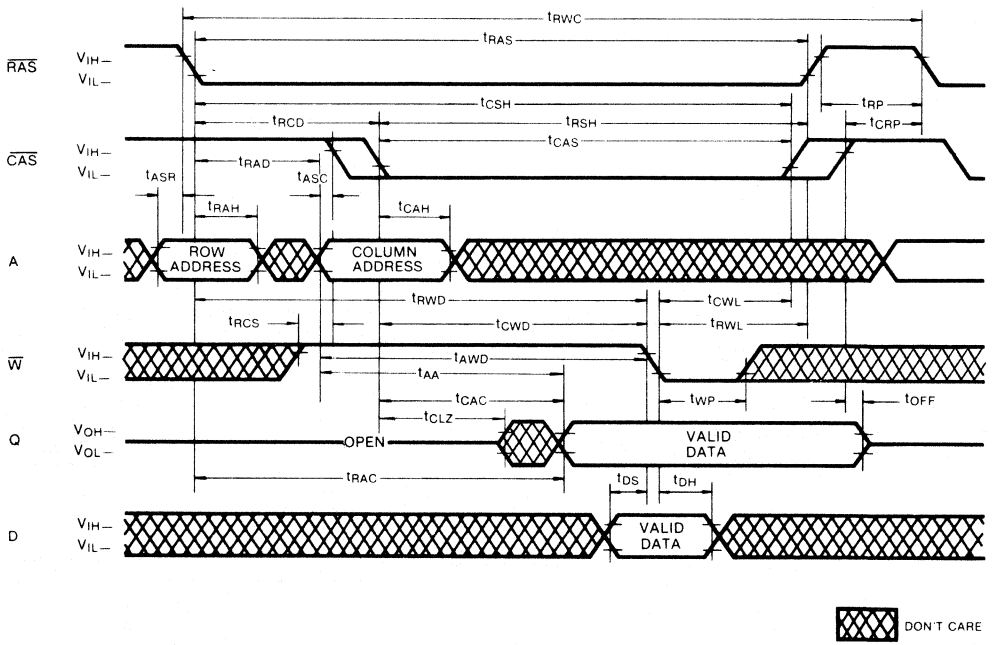


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

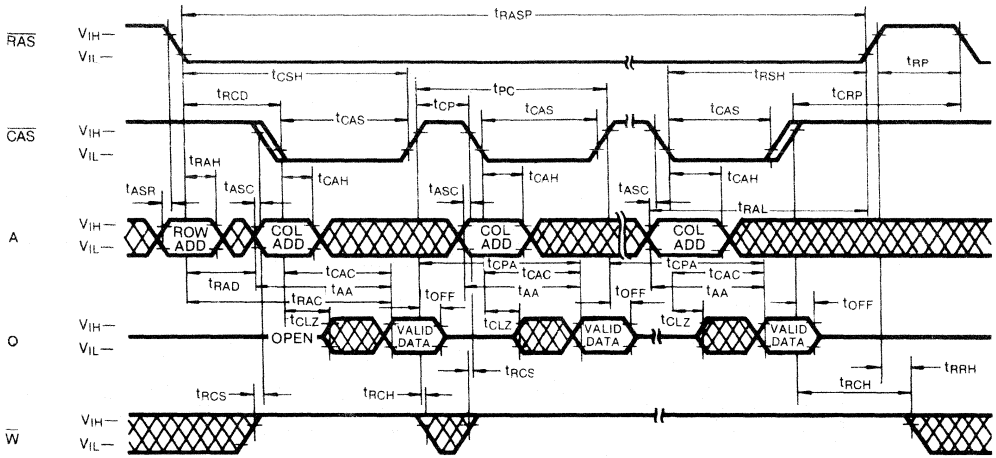


READ-WRITE/READ-MODIFY-WRITE CYCLE

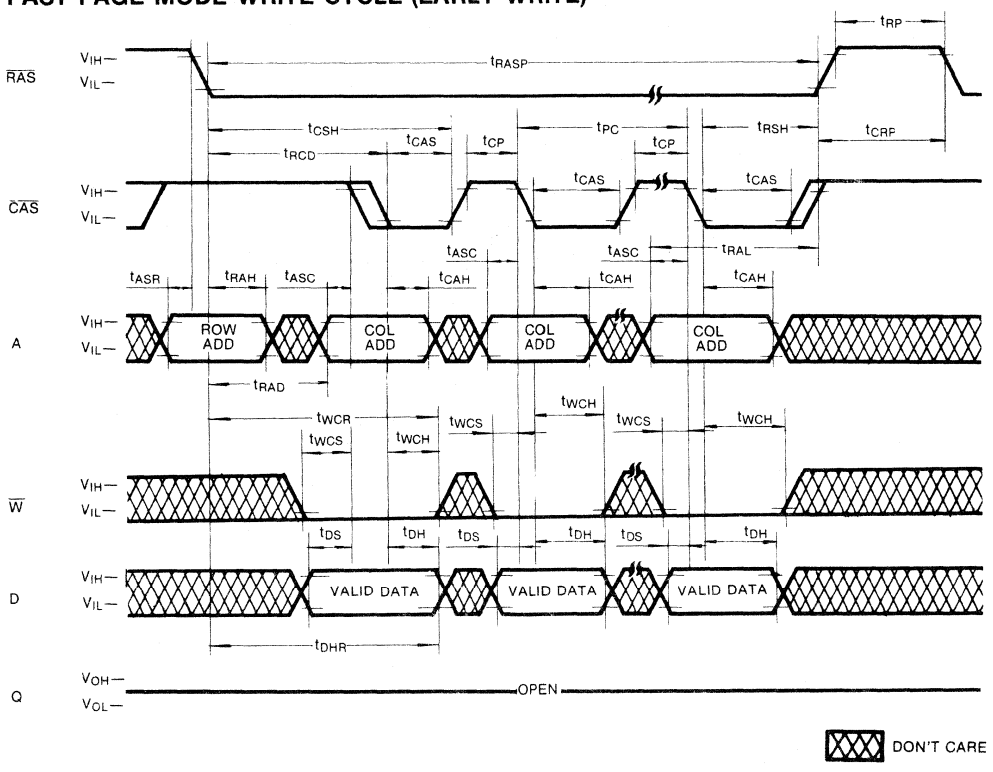


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE

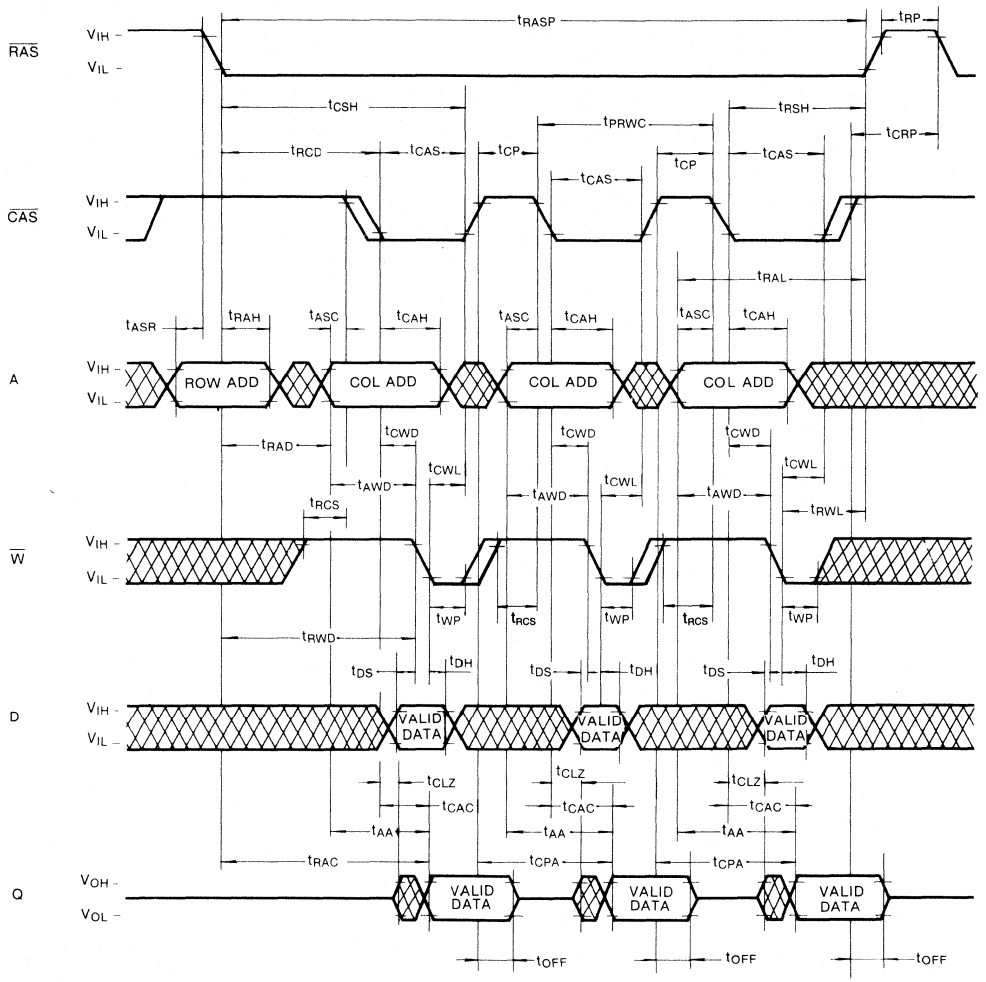


FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

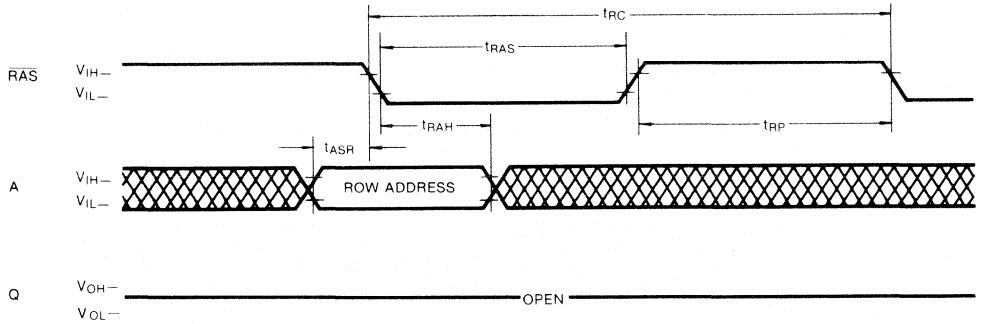
FAST PAGE MODE READ-WRITE CYCLE



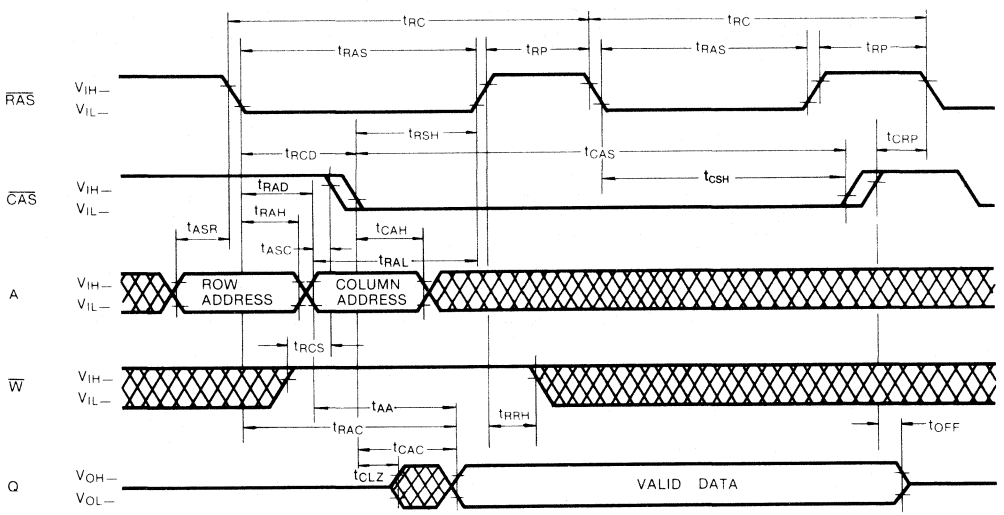
TIMING DIAGRAMS (Continued)

$\overline{RAS}$-ONLY REFRESH CYCLE

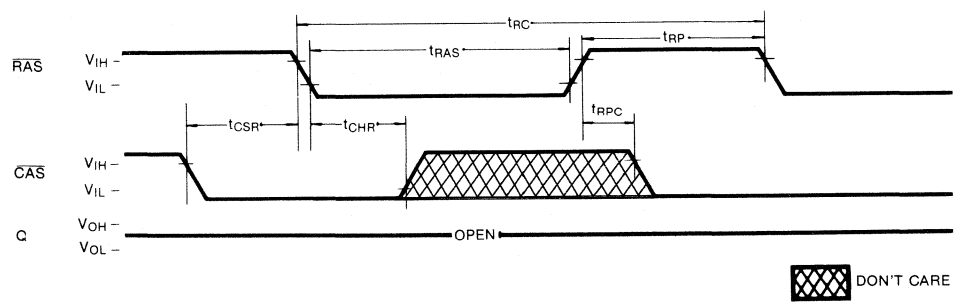
Note: $\overline{CAS}$ = V_{IH}, $\overline{W}$,D, A_9 = Don't Care



HIDDEN REFRESH CYCLE

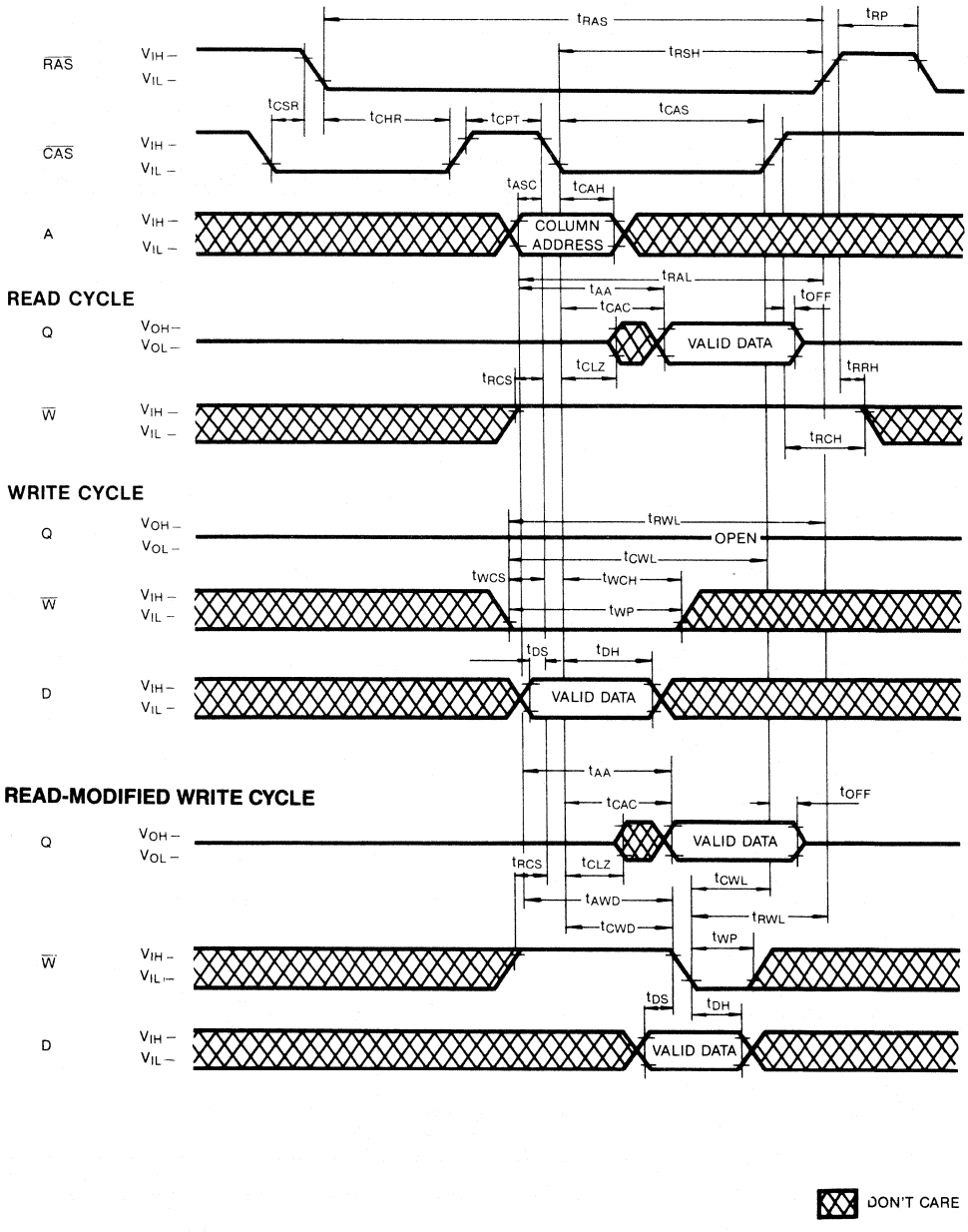


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM41C1000C contains 1,048,576 memory locations. Twenty address bits are required to address a particular memory location. Since the KM41C1000C has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM41C1000C begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C1000C cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (tRP) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by tRAS(min) and tCAS(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, tRP, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C1000C begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before tRCD(max) and if the column address is valid before tRAD(max) then the access time to valid data is specified by tRAC(min). However, if $\overline{CAS}$ goes low after tRCD(max) or if the column address becomes valid after tRAD(max), access is specified by tCAC or tAA. In order to achieve the minimum access time, tRAC(min), it is necessary to meet both tRCD(max) and tRAD(max).

Write

The KM41C1000C can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters tCWD and tAWD are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C1000C has a three-state output buffers which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (VIH) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by tCLZ after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after tCLZ and before the valid data appears at the output. The timing parameters tCAC, tRAC and tAA specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C1000C operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C1000C is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 8 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A0-A8). The state of address A9 is ignored during refresh.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C1000C has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (tCSR) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C1000C hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C1000C by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A0 through A8 are supplied by the on-chip refresh counter. The A9 bit is set low internally.

Fast Page Mode

The KM41C1000C has Fast Page mode capability which provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM41C1000C could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41C1000C inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C1000C input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

DEVICE OPERATION (Continued)

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the VCC to VSS voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each **KM41C1000C** using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the **KM41C1000C** and they supply much of the current used by the **KM41C1000C** during cycling.

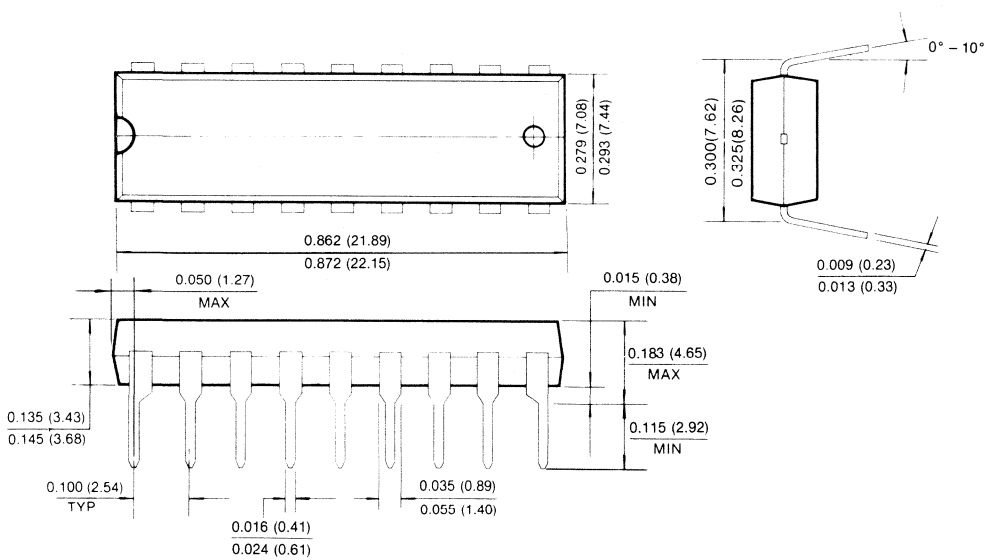
In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

2

PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

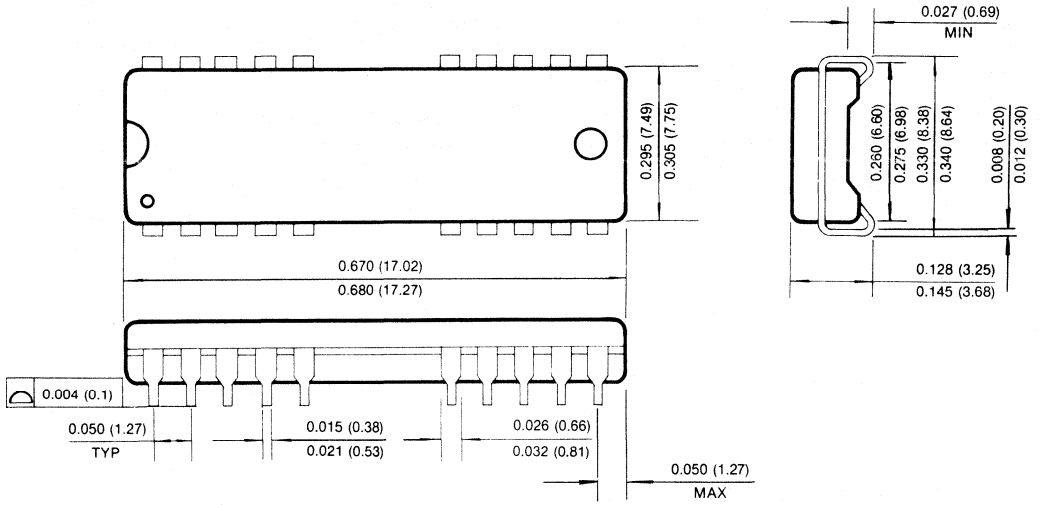
Units: Inches (Millimeters)



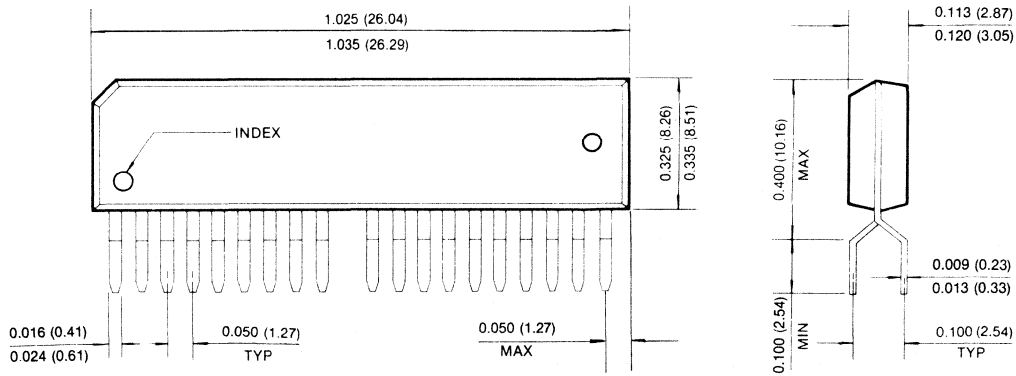
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



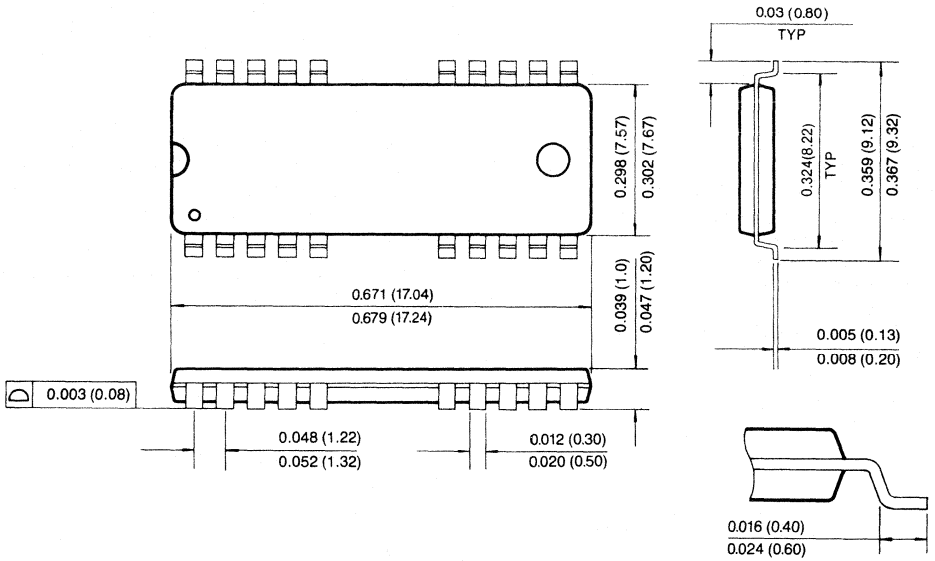
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



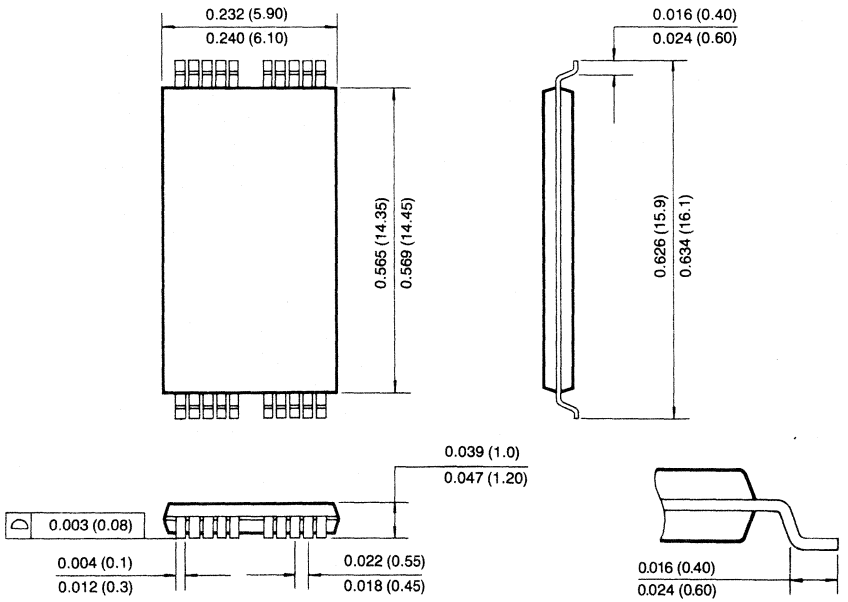
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (I) (Forward and Reverse Type)



1M×1 Bit CMOS Dynamic RAM with Fast Page Mode

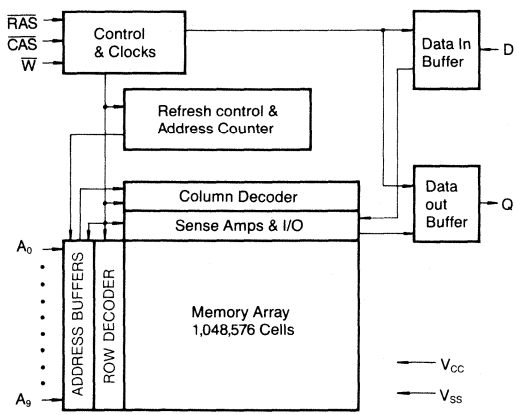
FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C1000CL-6	60ns	15ns	110ns
KM41C1000CL-7	70ns	20ns	130ns
KM41C1000CL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible input and output**
- **Single +5V ± 10% power supply**
- **Low power dissipation**
  - **I_{CC5}: 200μA**
  - **I_{CC7}: 200μA (Battery Backup Mode)**
- **512 cycle/64ms refresh**
- **256K×4 fast test mode**
- **JEDEC Standard pinout**
- Available in Plastic DIP, SOJ, ZIP, TSOP(I), TSOP(II) packages.

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The Samsung KM41C1000CL is a CMOS high speed 1,048,576 × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance microprocessor computers.

The KM41C1000CL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

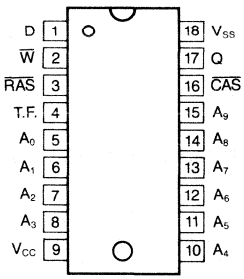
The KM41C1000CL is fabricated using Samsung's advanced CMOS process.

ORDERING INFORMATION

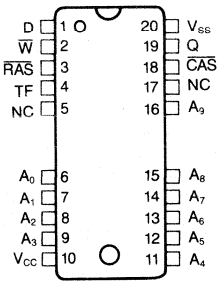
Part No.	Access Time	Package
KM41C1000CLP-6 KM41C1000CLP-7 KM41C1000CLP-8	60ns 70ns 80ns	300 mil. 18DIP
KM41C1000CLJ-6 KM41C1000CLJ-7 KM41C1000CLJ-8	60ns 70ns 80ns	300 mil. 20SOJ
KM41C1000CLZ-6 KM41C1000CLZ-7 KM41C1000CLZ-8	60ns 70ns 80ns	400 mil. 20ZIP
KM41C1000CLV-6 KM41C1000CLV-7 KM41C1000CLV-8	60ns 70ns 80ns	20 TOSP (I) (Forward)
KM41C1000CLVR-6 KM41C1000CLVR-7 KM41C1000CLVR-8	60ns 70ns 80ns	20 TOSP (I) (Reverse)
KM41C1000CLT-6 KM41C1000CLT-7 KM41C1000CLT-8	60ns 70ns 80ns	20 TOSP (II) (Forward)
KM41C1000CLTR-6 KM41C1000CLTR-7 KM41C1000CLTR-8	60ns 70ns 80ns	20 TOSP (II) (Reverse)

PIN CONFIGURATION (Top Views)

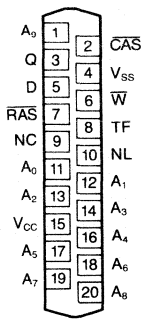
• KM41C1000CLP



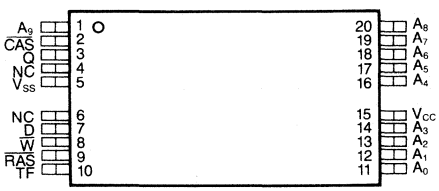
• KM41C1000CLJ



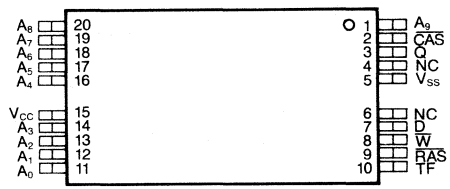
• KM41C1000CLZ



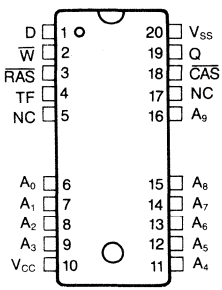
• KM41C1000CLV



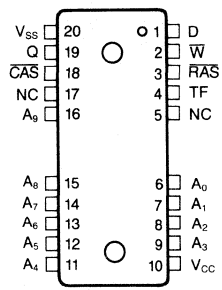
• KM41C1000CLVR



• KM41C1000CLT



• KM41C1000CLTR



Pin Names	Pin Function
A_0-A_9	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
TF	Test Function
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection
NL	No Lead

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, and $\overline{CAS}$, Address Cycling @t_{RC} = min.)	KM41C1000CL-6	I_{CC1}	—	70	mA
	KM41C1000CL-7		—	65	mA
	KM41C1000CL-8		—	60	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM41C1000CL-6	I_{CC3}	—	70	mA
	KM41C1000CL-7		—	65	mA
	KM41C1000CL-8		—	60	mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC} = min.)	KM41C1000CL-6	I_{CC4}	—	55	mA
	KM41C1000CL-7		—	50	mA
	KM41C1000CL-8		—	45	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC}-0.2V)		I_{CC5}	—	200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC} = min.)	KM41C1000CL-6	I_{CC6}	—	70	mA
	KM41C1000CL-7		—	65	mA
	KM41C1000CL-8		—	60	mA
Battery Back Up Current Average Power Supply Current, Battery back up Mode ($\overline{CAS}$ = $\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V, $\overline{W}$ = V_{CC} − 0.2V or 0.2V, A_0 ~ A_9 = V_{CC} − 0.2V or 0.2V, D_{IN} = V_{CC} − 0.2V, 0.2V or OPEN: t_{RC} = 125μS, t_{RAS} = t_{RAS} min. ~ 1μS)	KM41C1000CL-6 KM41C1000CL-7 KM41C1000CL-8	I_{CC7}	—	200	μA
Input Leakage Current (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0 ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3} Address can be changed maximum two times while $\overline{RAS}$ = V_{IL}, I_{CC4}, Address can be changed maximum once while $\overline{CAS}$ = V_{IH}.

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance [D]	C_{IN1}	—	5	pF
Input Capacitance [A_0-A_9]	C_{IN2}	—	6	pF
Input Capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$]	C_{IN3}	—	7	pF
Output Capacitance [Q]	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ± 10%, See notes 1, 2)

Parameter	Symbol	KM41C1000CL-6		KM41C1000CL-7		KM41C1000CL-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	130		150		170		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3, 4, 11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3, 4, 5
Access time from column address	t_{AA}		30		35		40	ns	3, 10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	

AC CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$, See notes 1, 2)

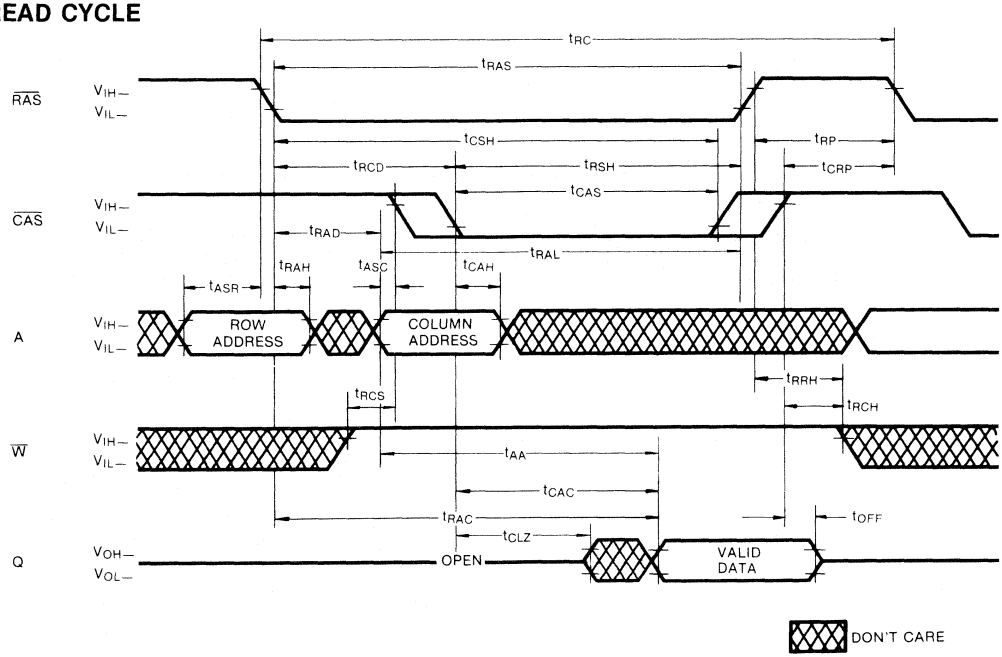
Parameter	Symbol	KM41C1000CL-6		KM41C1000CL-7		KM41C1000CL-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		50		55		ns	6
Write command pulse width	t_{WP}	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (512 cycles)	t_{REF}		64		64		64	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	15		20		20		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	60		70		80		ns	8
Column address to $\overline{W}$ dealy time	t_{AWD}	30		35		40		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	15		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		35		40	ns	3
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	60		60		65		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
12. Normal operation requires the "T.F" pin to be connected to V_{SS} or TTL logic low level or left unconnected on the printed wiring board.
13. When the "T.F" pin is connected to a defined positive voltage, the internal test function may be activated. Contact Samsung for specific operational details of the "test function."
14. In a test mode read cycle, the value of t_{RAC}, t_{CAC}, t_{AA} is delayed for 3ns.

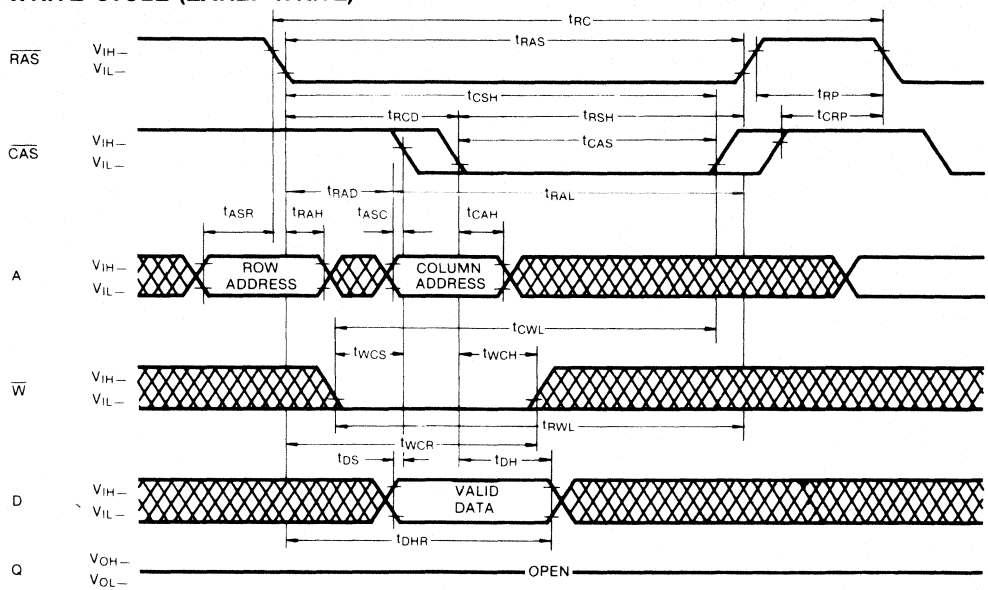
TIMING DIAGRAMS

READ CYCLE

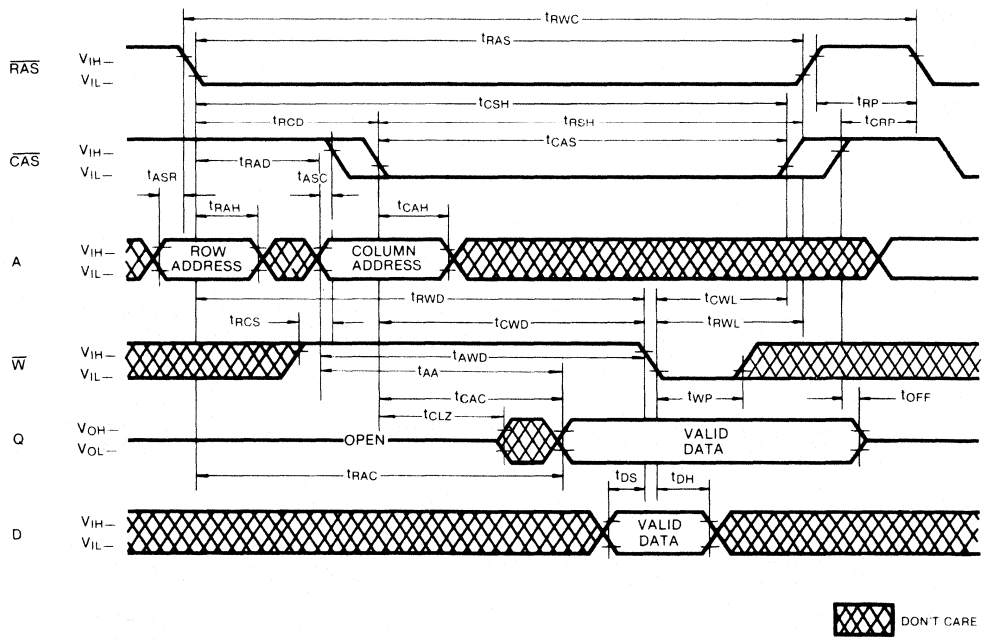


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

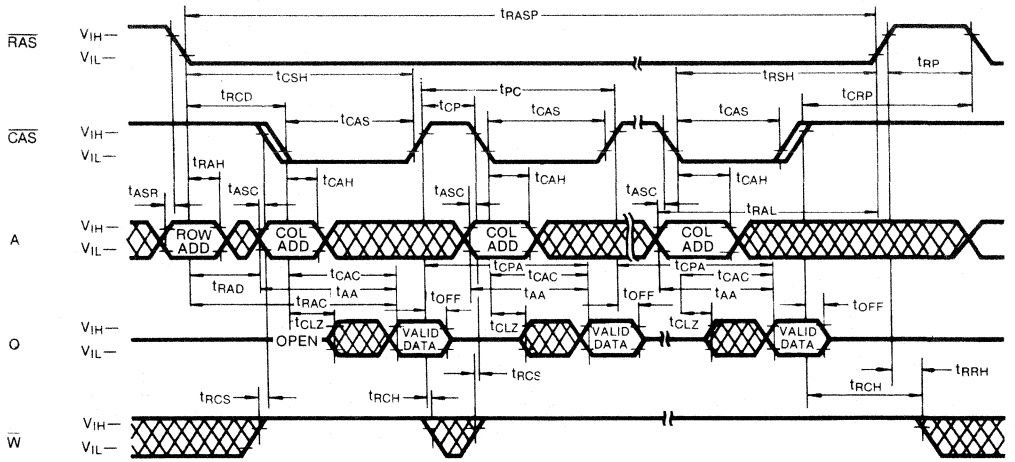


READ-WRITE/READ-MODIFY-WRITE CYCLE

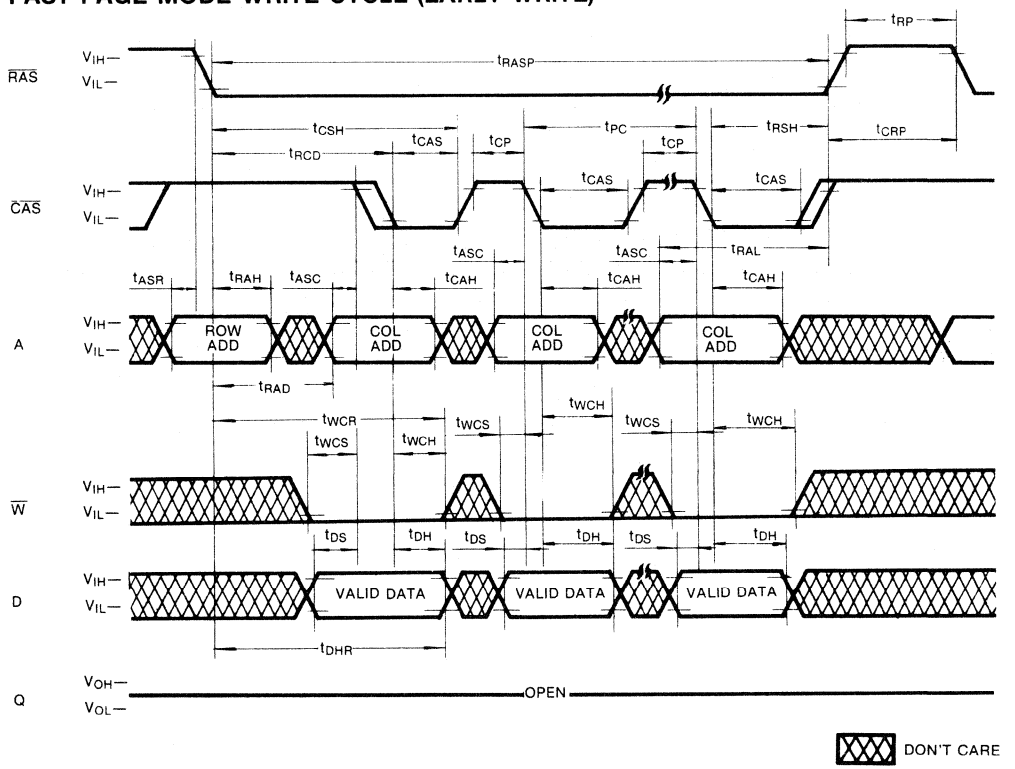


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE

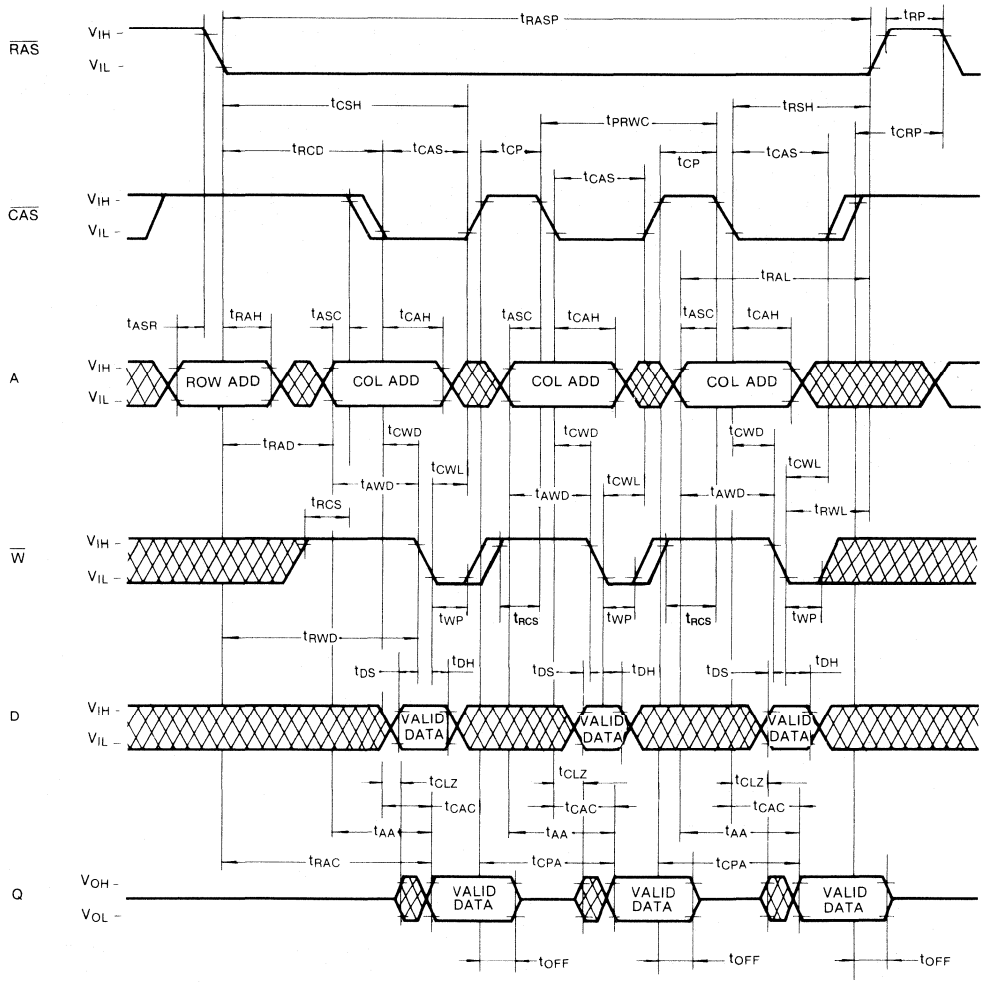


FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

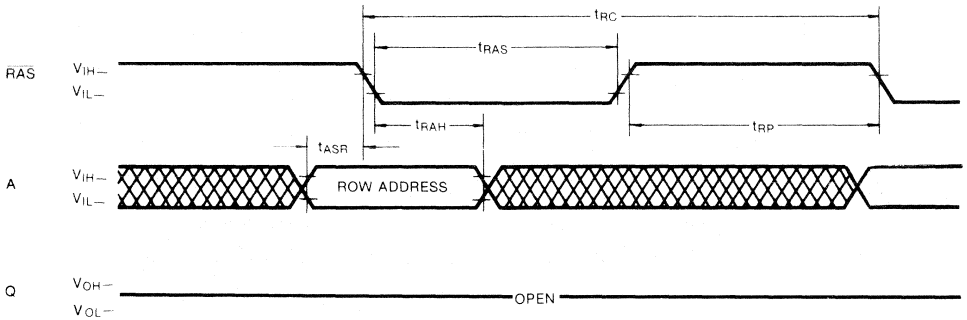
FAST PAGE MODE READ-WRITE CYCLE



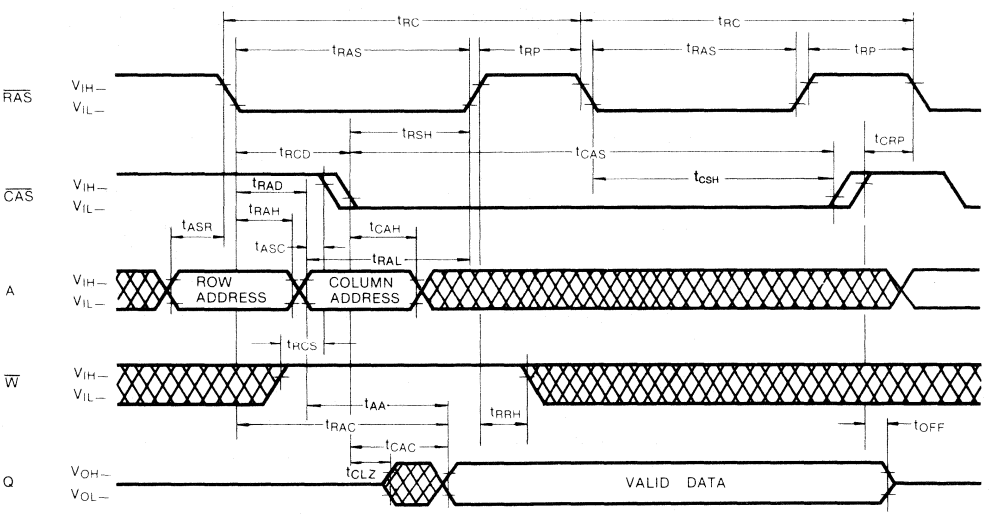
TIMING DIAGRAMS (Continued)

$\overline{RAS}$-ONLY REFRESH CYCLE

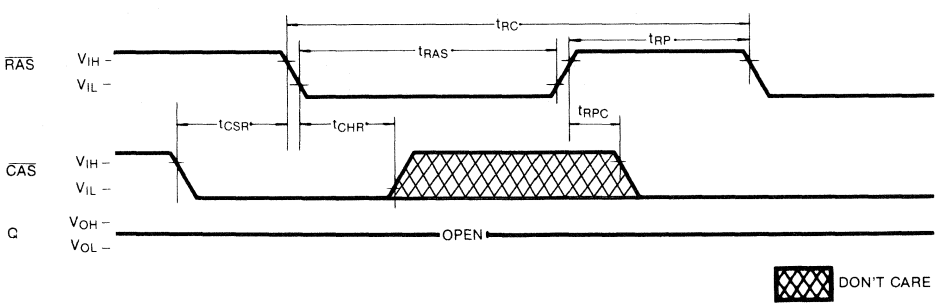
Note: $\overline{CAS}$ = V_{IH}, $\overline{W}$,D, A_9 = Don't Care



HIDDEN REFRESH CYCLE

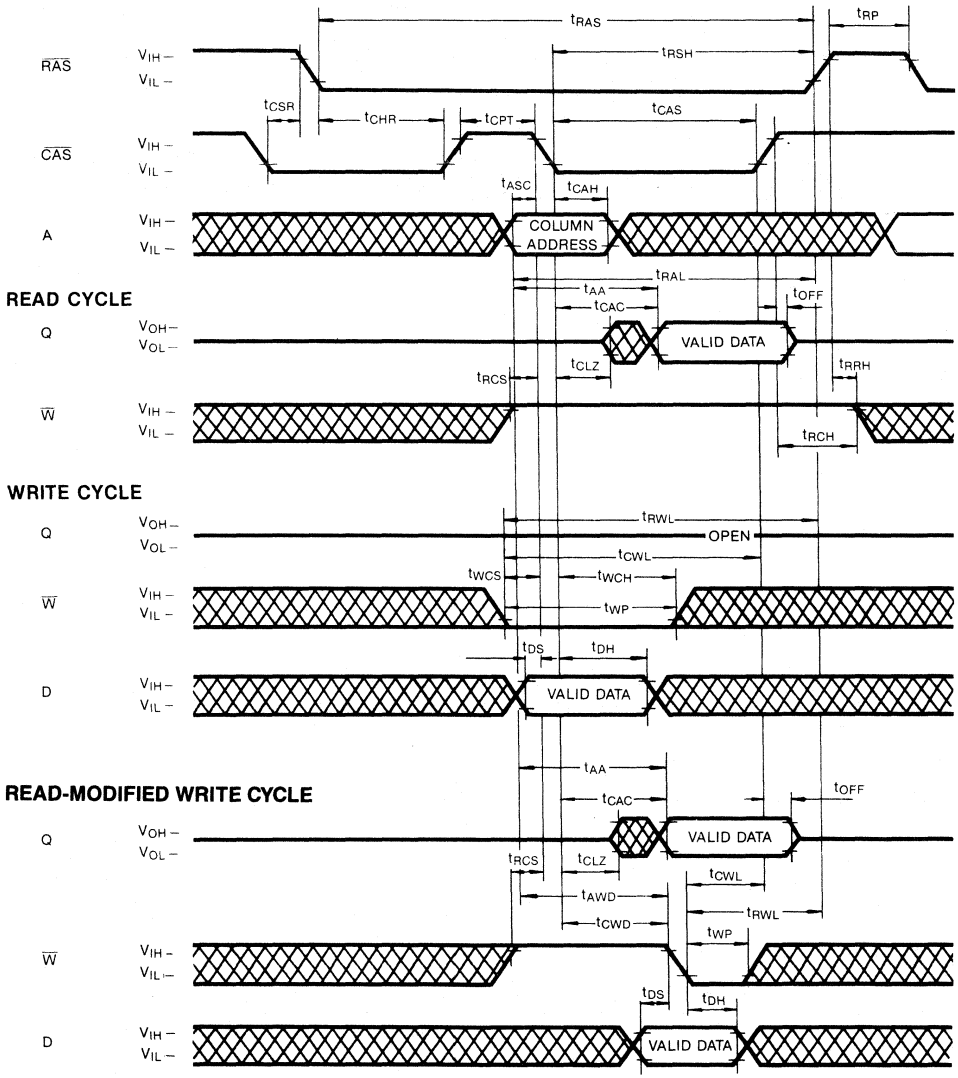


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DON'T CARE

DEVICE OPERATION

Device Operation

The KM41C1000CL contains 1,048,576 memory locations. Twenty address bits are required to address a particular memory location. Since the KM41C1000CL has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM41C1000CL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C1000CL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both RAS and CAS have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (tRP) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by tRAS(min) and tCAS(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, tRP, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C1000CL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before tRCD(max) and if the column address is valid before tRAD(max) then the access time to valid data is specified by tRAC(min). However, if $\overline{CAS}$ goes low after tRCD(max) or if the column address becomes valid after tRAD(max), access is specified by tCAC or tAA. In order to achieve the minimum access time, tRAC(min), it is necessary to meet both tRCD(max) and tRAD(max).

Write

The KM41C1000CL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters tCWD and tAWD are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C1000CL has a three-state output buffers which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by tCLZ after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after tCLZ and before the valid data appears at the output. The timing parameters tCAC, tRAC and tAA specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C1000CL operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C1000CL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 64 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A0-A8). The state of address A9 is ignored during refresh.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C1000CL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (tCSR) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C1000CL hidden refresh cycle is actually a CAS-before-RAS refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C1000CL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A0 through A8 are supplied by the on-chip refresh counter. The A9 bit is set low internally.

Fast Page Mode

The KM41C1000CL has Fast Page mode capability which provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM41C1000CL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41C1000CL inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C1000CL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

DEVICE OPERATION (Continued)

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground **pins of each KM41C1000CL using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C1000CL and they supply much of the current used by the KM41C1000CL during cycling.**

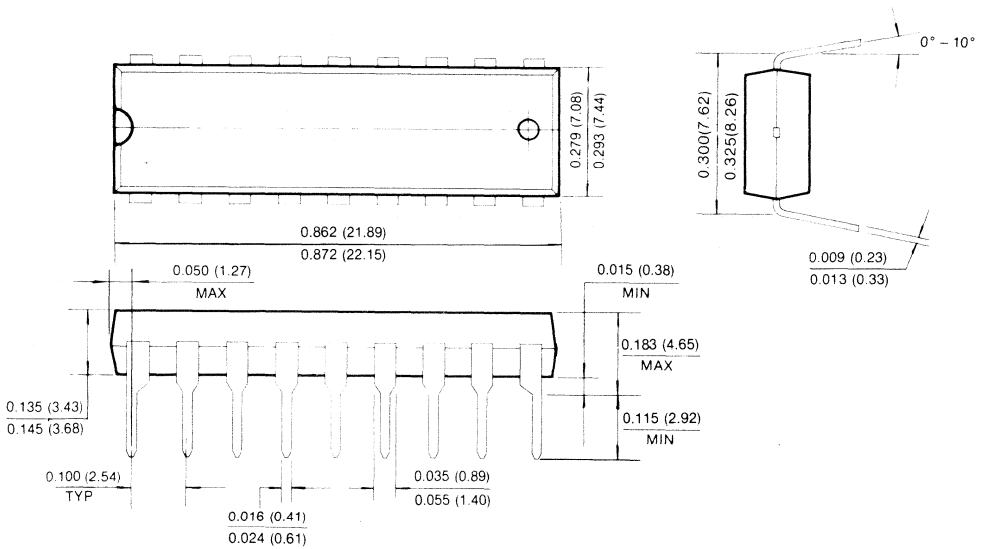
In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

2

PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

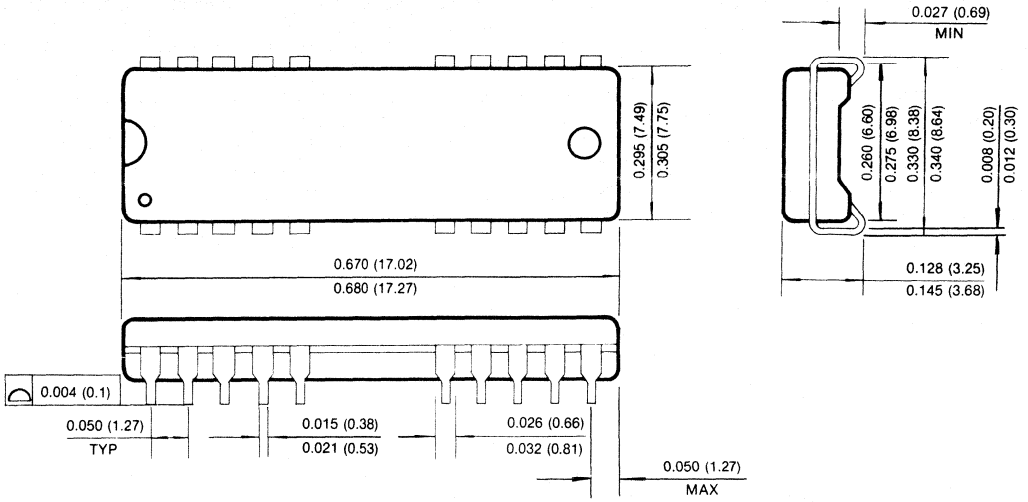
Units: Inches (Millimeters)



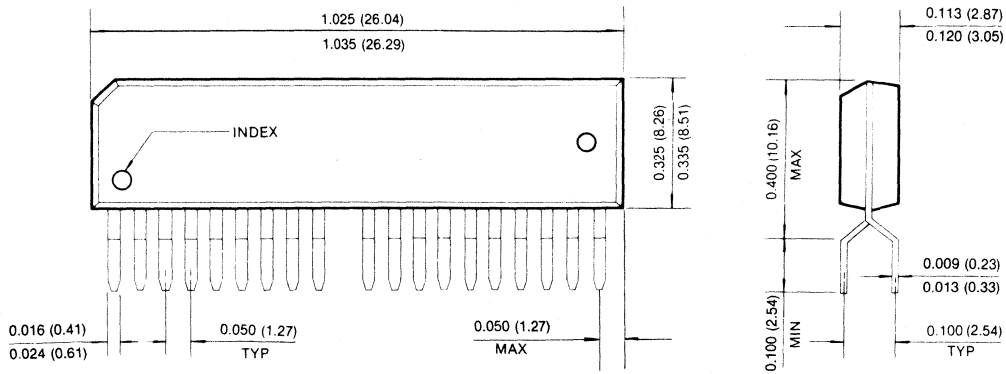
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



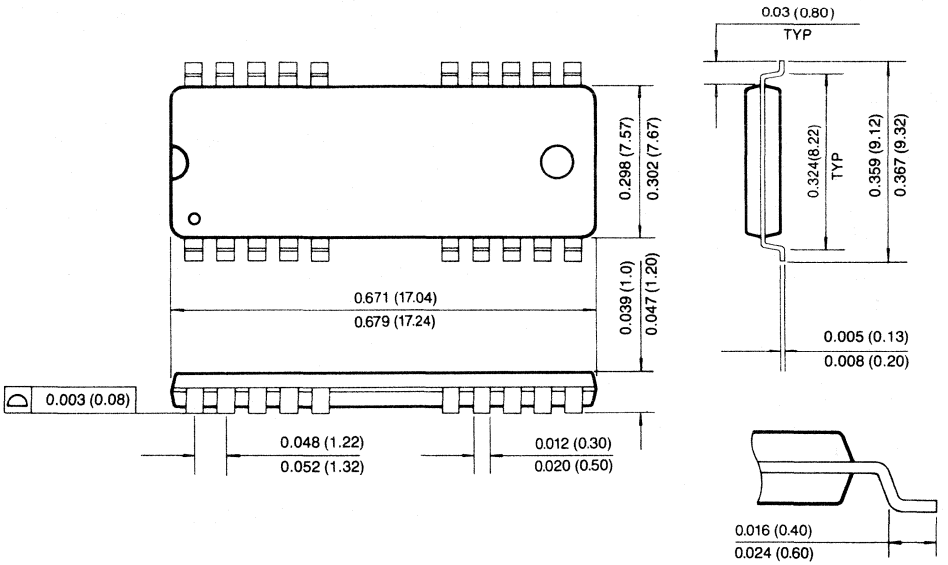
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



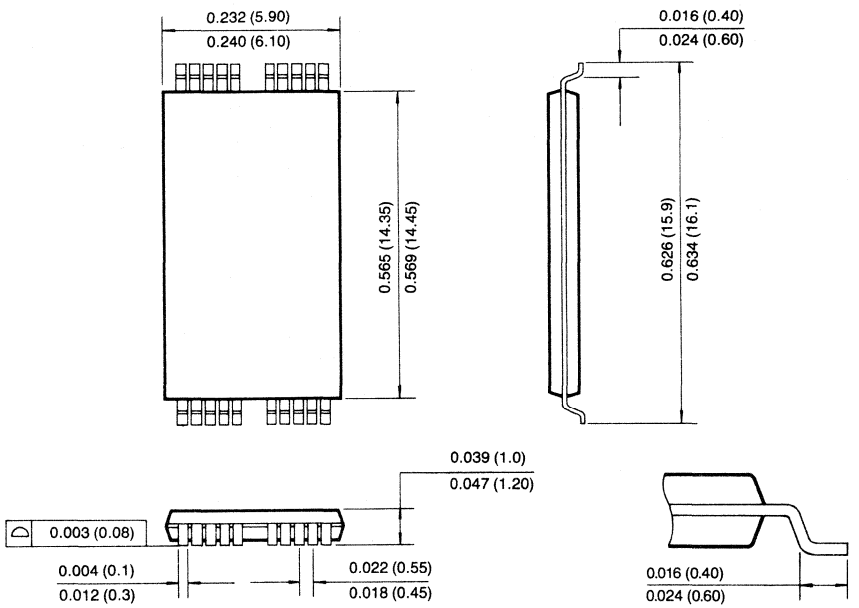
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (I) (Forward and Reverse Type)



1M×1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C1000CSL-6	60ns	15ns	110ns
KM41C1000CSL-7	70ns	20ns	130ns
KM41C1000CSL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible input and output**
- **Single +5V ± 10% power supply**
- **Low power dissipation**
  - **I_{CC5}: 100μA**
  - **I_{CC7}: 100μA**
- **512 cycle/128ms refresh**
- **256K×4 fast test mode**
- **JEDEC Standard pinout**
- Available in Plastic DIP, SOJ, ZIP, TSOP(I), TSOP(II) packages.

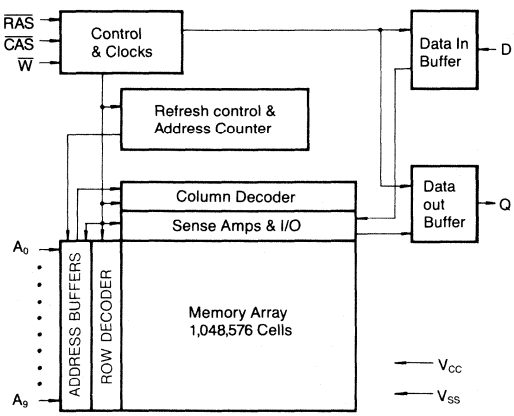
GENERAL DESCRIPTION

The Samsung KM41C1000CSL is a CMOS high speed 1,048,576 × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance microprocessor computers.

The KM41C1000CSL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM41C1000CSL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

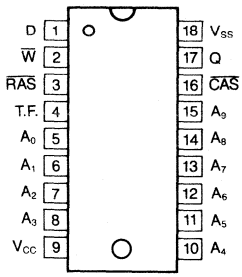


ORDERING INFORMATION

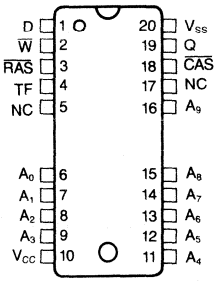
Part No.	Access Time	Package
KM41C1000CSLP-6	60ns	300 mil. 18DIP
KM41C1000CSLP-7	70ns	
KM41C1000CSLP-8	80ns	
KM41C1000CSLJ-6	60ns	300 mil. 20SOJ
KM41C1000CSLJ-7	70ns	
KM41C1000CSLJ-8	80ns	
KM41C1000CSLZ-6	60ns	400 mil. 20ZIP
KM41C1000CSLZ-7	70ns	
KM41C1000CSLZ-8	80ns	
KM41C1000CSLV-6	60ns	20 TOSP (I) (Forward)
KM41C1000CSLV-7	70ns	
KM41C1000CSLV-8	80ns	
KM41C1000CSLVR-6	60ns	20 TOSP (I) (Reverse)
KM41C1000CSLVR-7	70ns	
KM41C1000CSLVR-8	80ns	
KM41C1000CSLT-6	60ns	20 TOSP (II) (Forward)
KM41C1000CSLT-7	70ns	
KM41C1000CSLT-8	80ns	
KM41C1000CSLTR-6	60ns	20 TOSP (II) (Reverse)
KM41C1000CSLTR-7	70ns	
KM41C1000CSLTR-8	80ns	

PIN CONFIGURATION (Top Views)

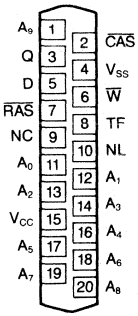
• KM41C1000CSLP



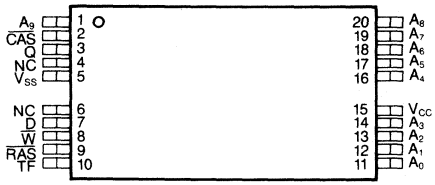
• KM41C1000CSLJ



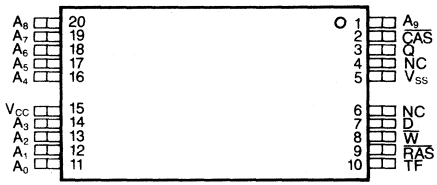
• KM41C1000CSLZ



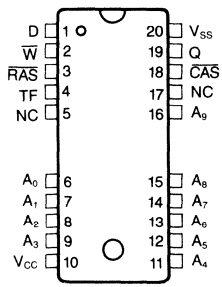
• KM41C1000CSLV



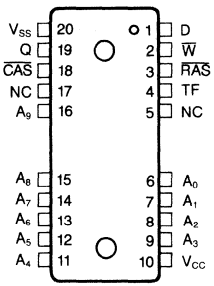
• KM41C1000CSLVR



• KM41C1000CSLT •



• KM41C1000CSLTR



Pin Names	Pin Function
A_0-A_9	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
TF	Test Function
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection
NL	No Lead

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, and $\overline{CAS}$, Address Cycling @t_{RC} = min.)	KM41C1000CSL-6	I_{CC1}	—	70	mA
	KM41C1000CSL-7		—	65	mA
	KM41C1000CSL-8		—	60	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM41C1000CSL-6	I_{CC3}	—	70	mA
	KM41C1000CSL-7		—	65	mA
	KM41C1000CSL-8		—	60	mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC} = min.)	KM41C1000CSL-6	I_{CC4}	—	55	mA
	KM41C1000CSL-7		—	50	mA
	KM41C1000CSL-8		—	45	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC}-0.2V)		I_{CC5}	—	100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC} = min.)	KM41C1000CSL-6	I_{CC6}	—	70	mA
	KM41C1000CSL-7		—	65	mA
	KM41C1000CSL-8		—	60	mA
Battery Back Up Current Average Power Supply Current, Battery back up Mode ($\overline{CAS}$ = $\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V, $\overline{W}$ = V_{CC} − 0.2V or 0.2V, A_0 ~ A_9 = V_{CC} − 0.2V or 0.2V, D_{IN} = V_{CC} − 0.2V, 0.2V or OPEN: t_{RC} = 250μS, t_{RAS} = t_{RAS} min. ~ 1μS)	KM41C1000CSL-6 KM41C1000CSL-7 KM41C1000CSL-8	I_{CC7}	—	100	μA
Input Leakage Current (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0 ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3} Address can be changed maximum two times while $\overline{RAS}$ = V_{IL}, I_{CC4}, Address can be changed maximum once while $\overline{CAS}$ = V_{IH}.

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance [D]	C_{IN1}	—	5	pF
Input Capacitance [A_0-A_9]	C_{IN2}	—	6	pF
Input Capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$]	C_{IN3}	—	7	pF
Output Capacitance [Q]	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ± 10%, See notes 1, 2)

Parameter	Symbol	KM41C1000CSL-6		KM41C1000CSL-7		KM41C1000CSL-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	130		150		170		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3, 4, 11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3, 4, 5
Access time from column address	t_{AA}		30		35		40	ns	3, 10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	

AC CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$, See notes 1, 2)

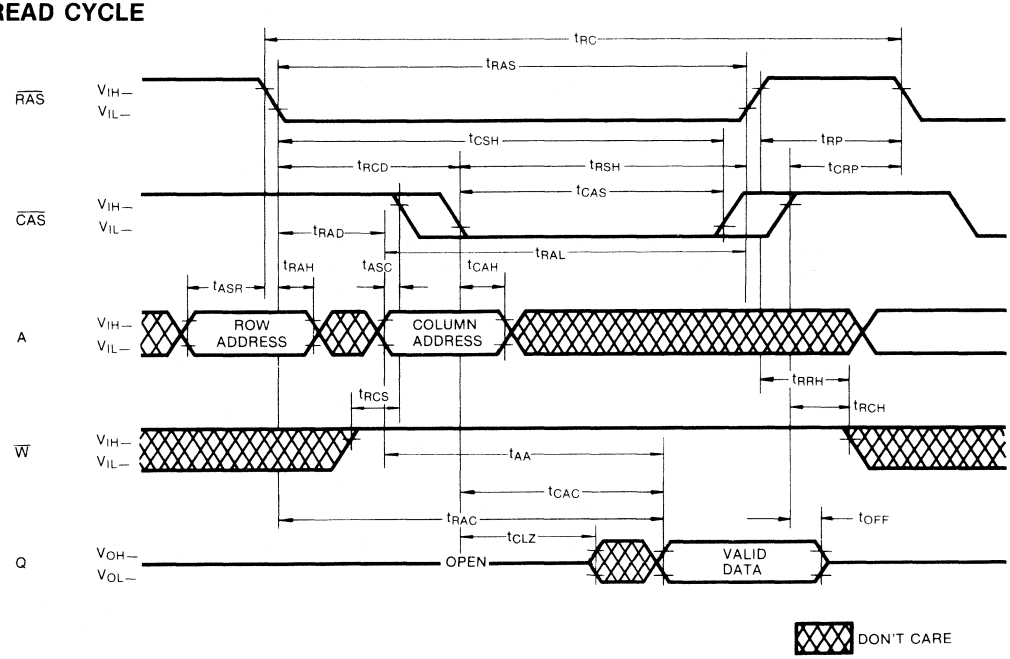
Parameter	Symbol	KM41C1000CSL-6		KM41C1000CSL-7		KM41C1000CSL-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		50		55		ns	6
Write command pulse width	t_{WP}	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (512 cycles)	t_{REF}		128		128		128	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	15		20		20		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	60		70		80		ns	8
Column address to $\overline{W}$ dealy time	t_{AWD}	30		35		40		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	15		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		35		40	ns	3
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	60		60		65		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
12. Normal operation requires the "T.F" pin to be connected to V_{SS} or TTL logic low level or left unconnected on the printed wiring board.
13. When the "T.F" pin is connected to a defined positive voltage, the internal test function may be activated. Contact Samsung for specific operational details of the "test function."
14. In a test mode read cycle, the value of t_{RAC}, t_{CAC}, t_{AA} is delayed for 3ns.

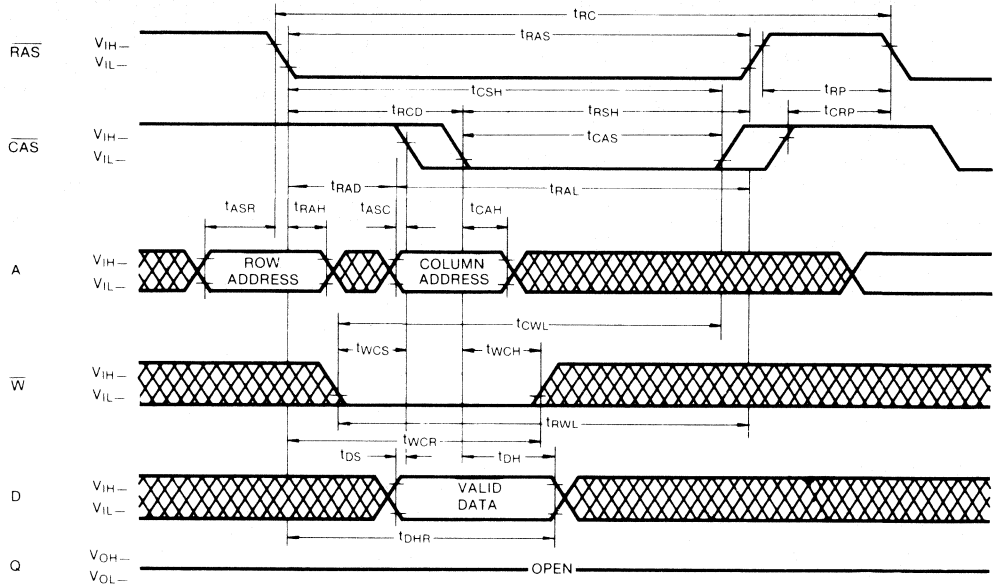
TIMING DIAGRAMS

READ CYCLE

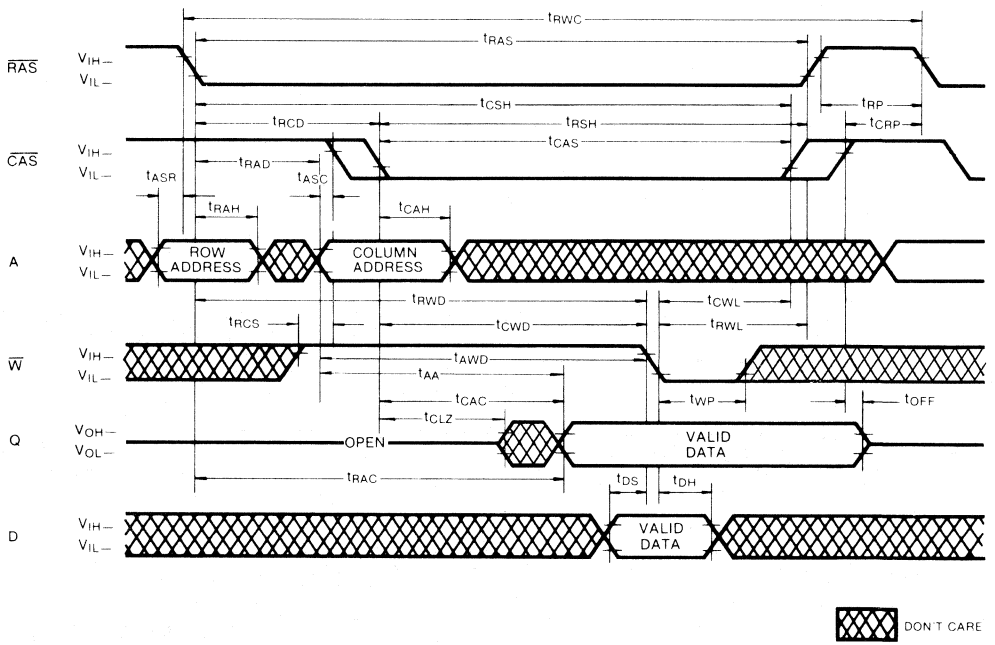


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

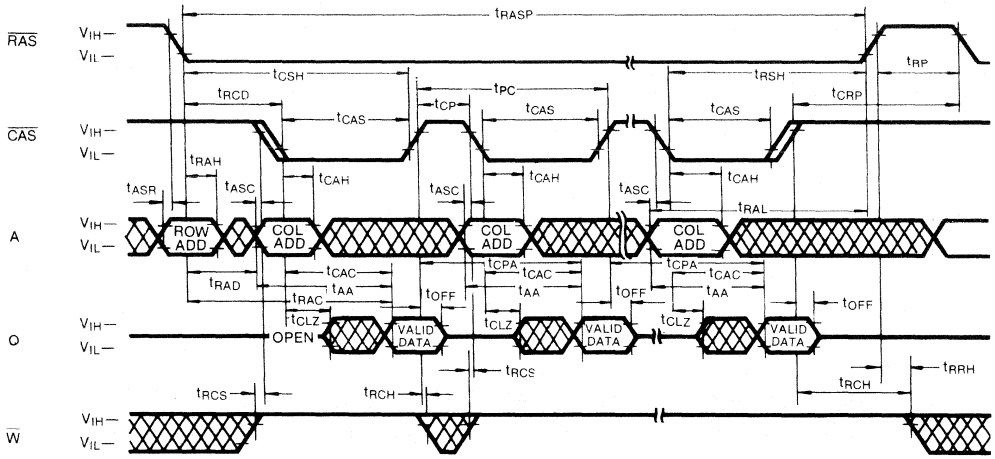


READ-WRITE/READ-MODIFY-WRITE CYCLE

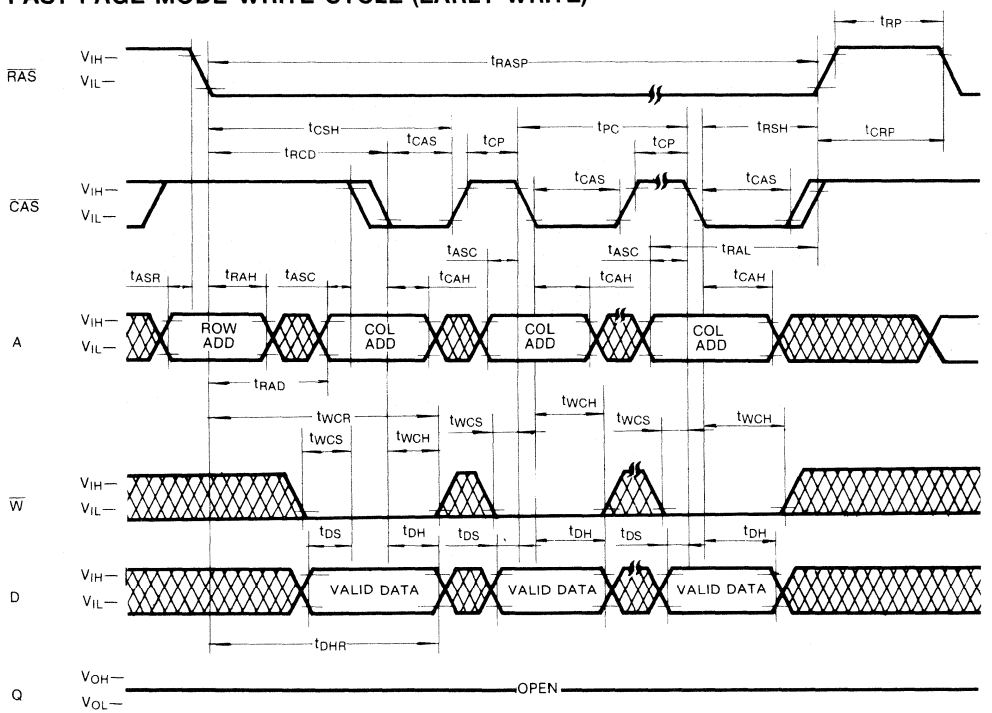


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE

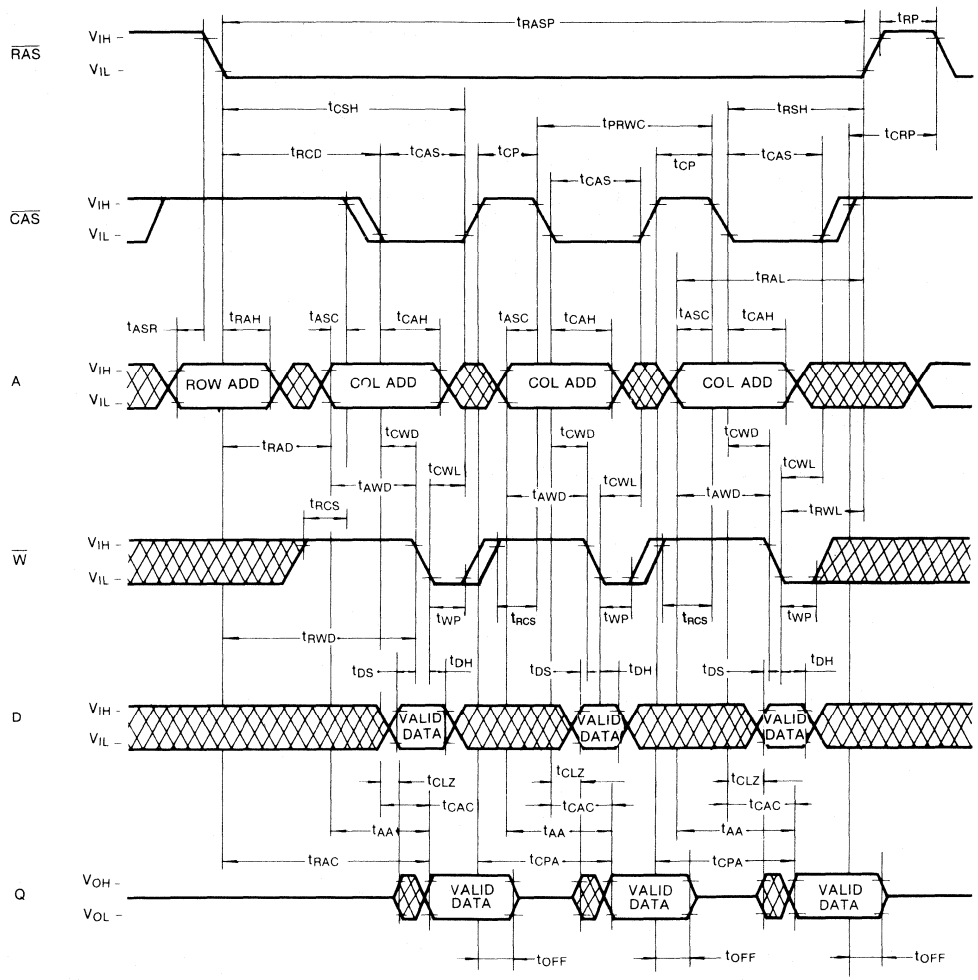


FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

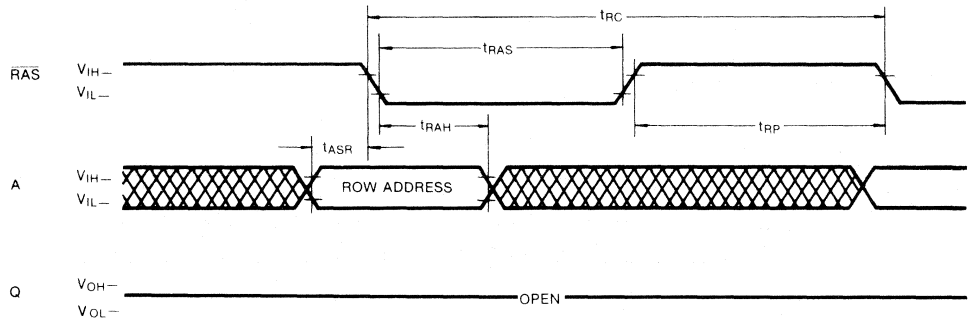
FAST PAGE MODE READ-WRITE CYCLE



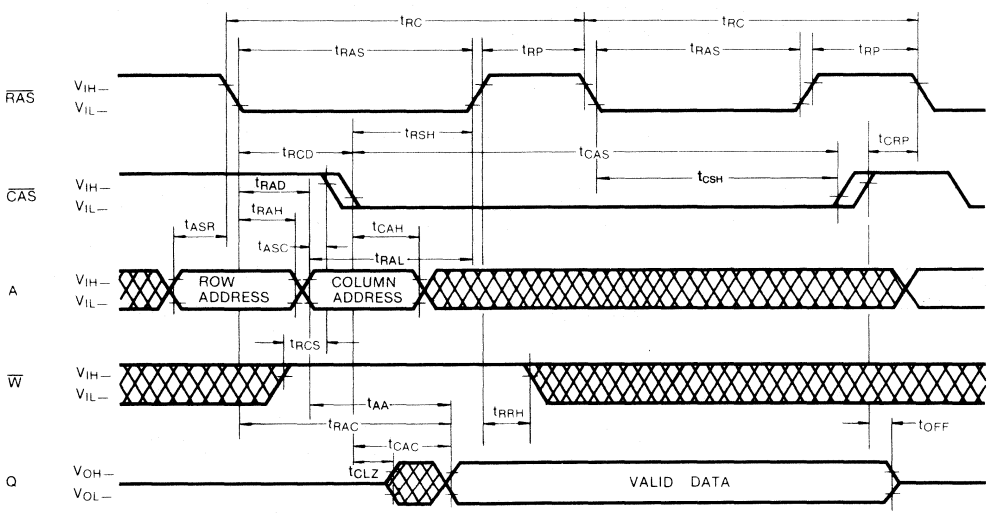
TIMING DIAGRAMS (Continued)

$\overline{RAS}$-ONLY REFRESH CYCLE

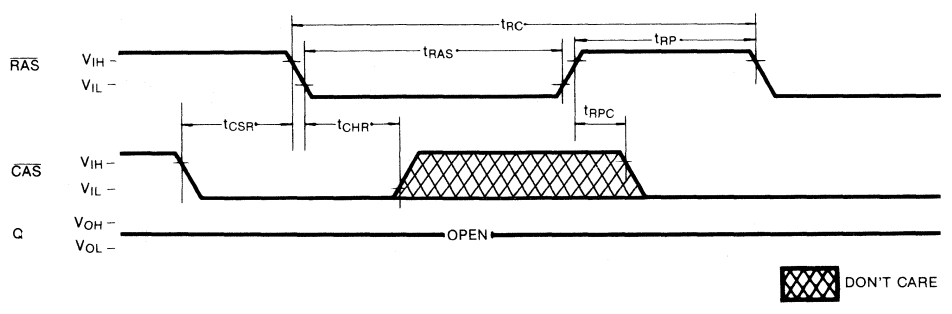
Note: $\overline{CAS}$ = V_{IH}, $\overline{W}$,D, A_9 = Don't Care



HIDDEN REFRESH CYCLE

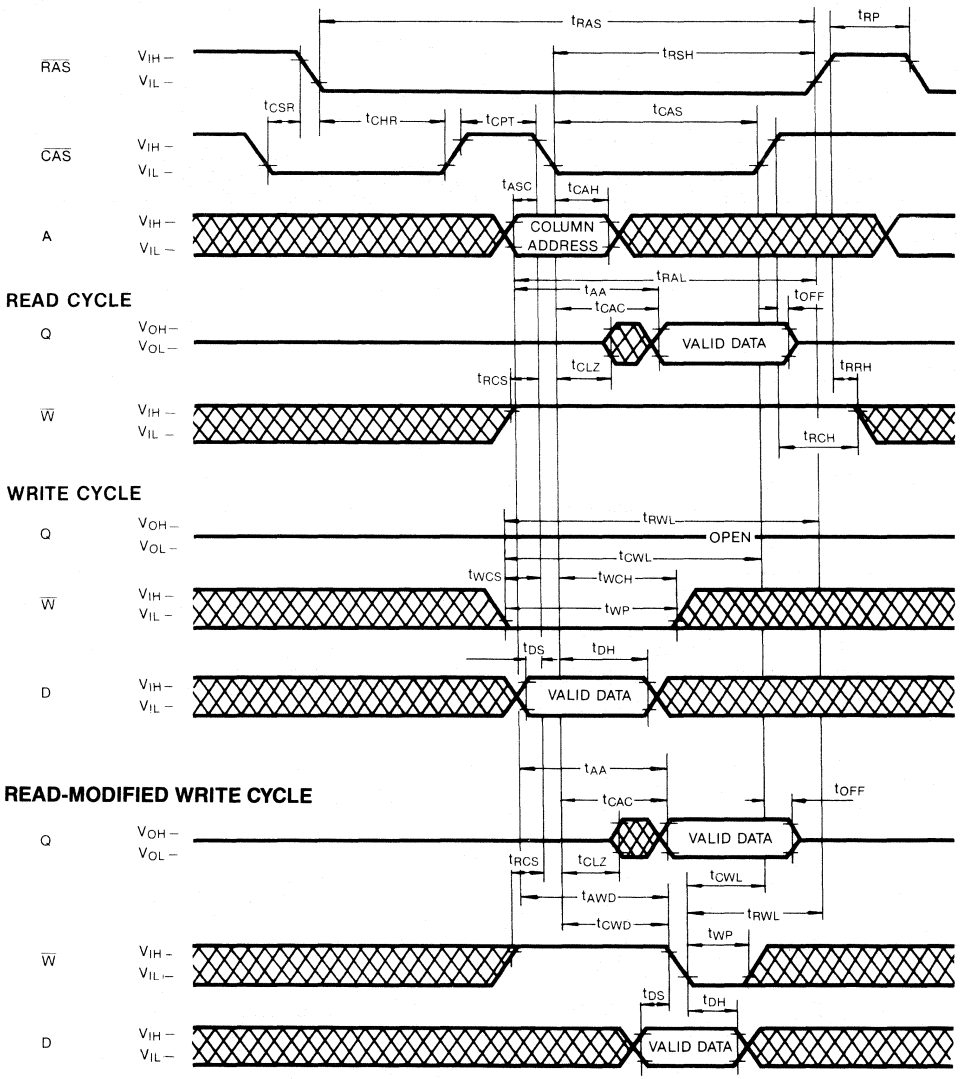


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM41C1000CSL contains 1,048,576 memory locations. Twenty address bits are required to address a particular memory location. Since the KM41C1000CSL has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM41C1000CSL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C1000CSL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (tRP) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by tRAS(min) and tCAS(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, tRP, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C1000CSL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before tRCD(max) and if the column address is valid before tRAD(max) then the access time to valid data is specified by tRAC(min). However, if $\overline{CAS}$ goes low after tRCD(max) or if the column address becomes valid after tRAD(max), access is specified by tCAC or tAA. In order to achieve the minimum access time, tRAC(min), it is necessary to meet both tRCD(max) and tRAD(max).

Write

The KM41C1000CSL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters tCWD and tAWD are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C1000CSL has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by tCLZ after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after tCLZ and before the valid data appears at the output. The timing parameters tCAC, tRAC and tAA specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C1000CSL operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C1000CSL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 128 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A0-A8). The state of address A9 is ignored during refresh.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C1000CSL has CAS-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (tCSR) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C1000CSL hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C1000CSL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A0 through A8 are supplied by the on-chip refresh counter. The A9 bit is set low internally.

Fast Page Mode

The KM41C1000CSL has Fast Page mode capability which provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM41C1000CSL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41C1000CSL inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C1000CSL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

DEVICE OPERATION (Continued)

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM41C1000CSL using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C1000CSL and they supply much of the current used by the KM41C1000CSL during cycling.

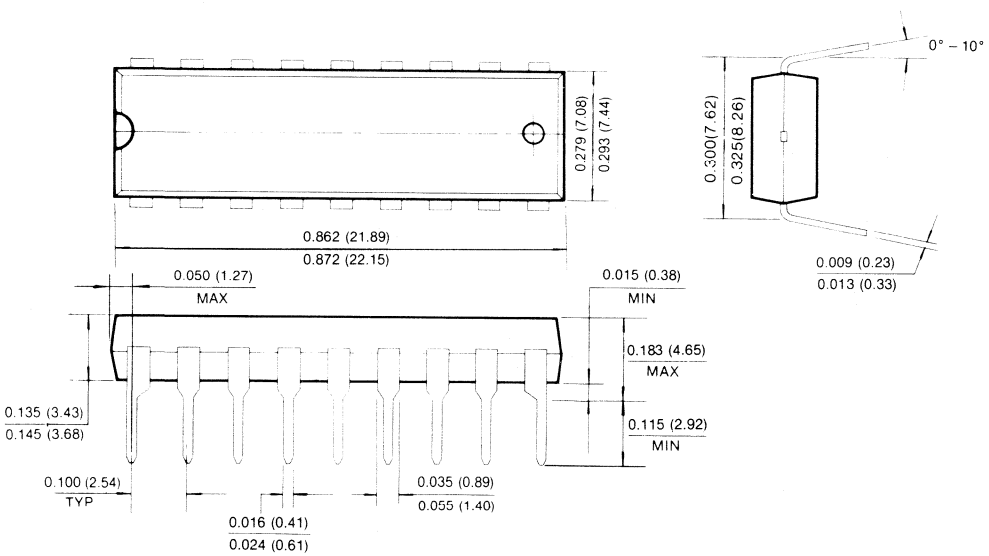
In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

2

PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

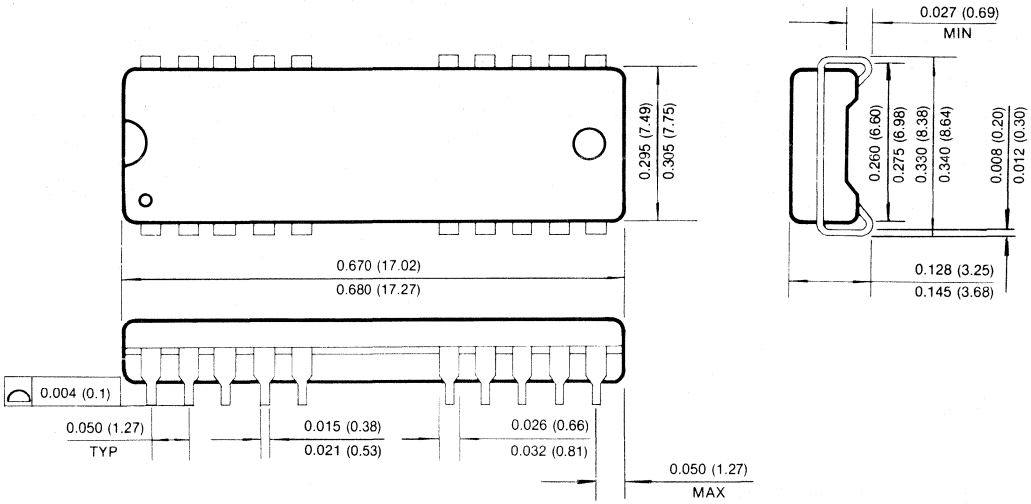
Units: Inches (Millimeters)



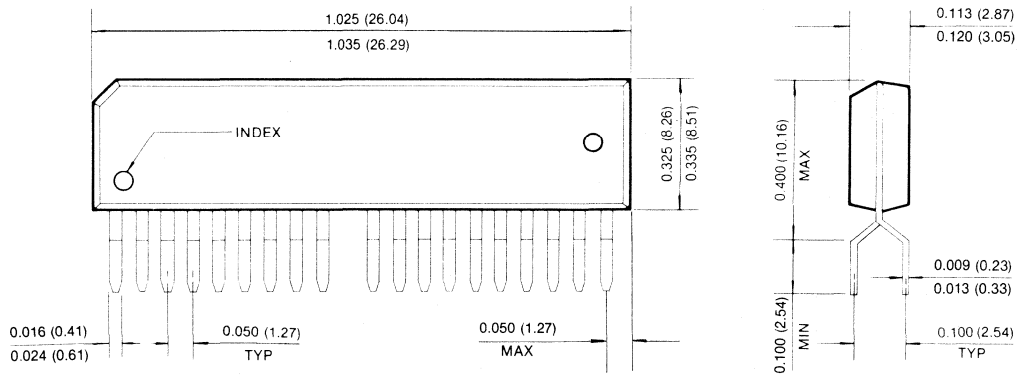
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



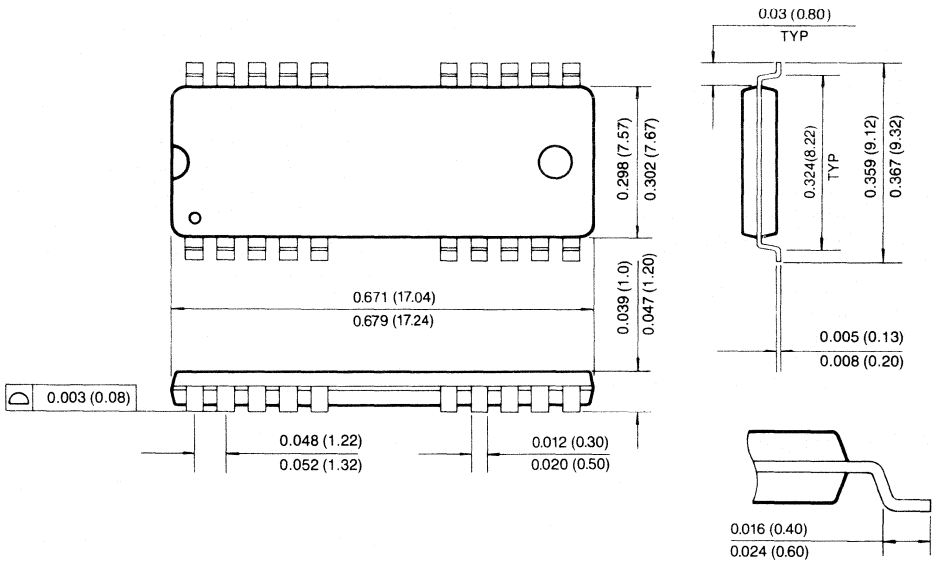
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



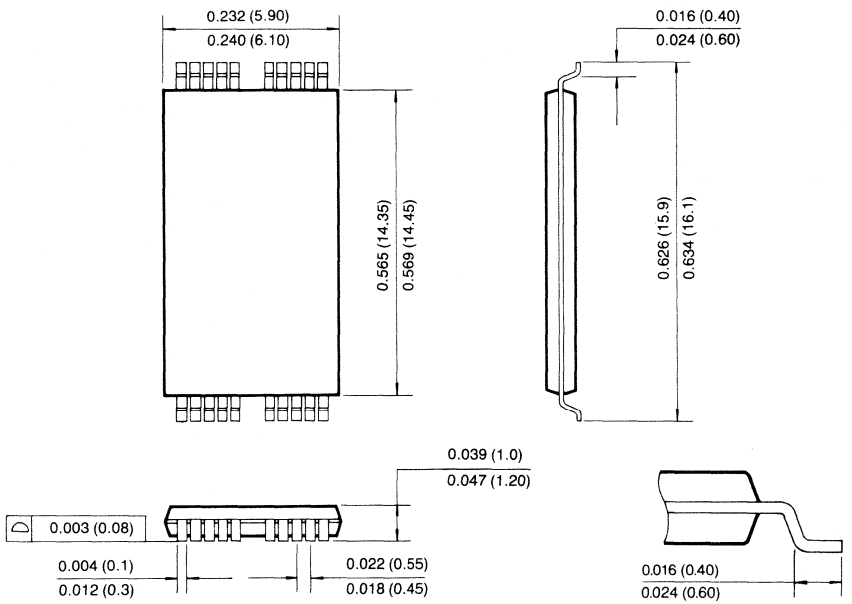
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (I) (Forward and Reverse Type)



1M x 1 Bit CMOS Dynamic RAM with Nibble Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C1001C-6	60ns	15ns	110ns
KM41C1001C-7	70ns	20ns	130ns
KM41C1001C-8	80ns	20ns	150ns

- **Nibble Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and output**
- **Common I/O using early write**
- **Single +5V ± 10% power supply**
- **512 cycle/8ms refresh**
- **256K x 4 fast test mode**
- **JEDEC Standard pinout**
- **Available in Plastic DIP SOJ, ZIP packages**

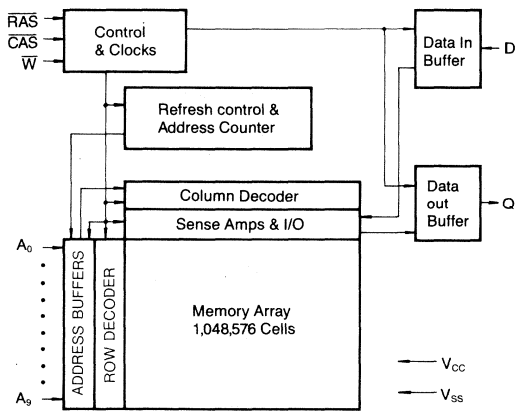
GENERAL DESCRIPTION

The Samsung KM41C1001C is a CMOS high speed 1,048,576 x 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance microprocessor computers.

The KM41C1001C features Nibble Mode operation which allows high speed random access of up to 4 bits of data. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

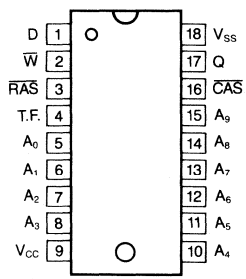
The KM41C1001C is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

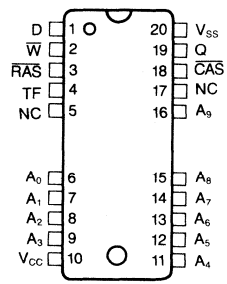


PIN CONFIGURATION (Top Views)

- **KM41C1001CP**

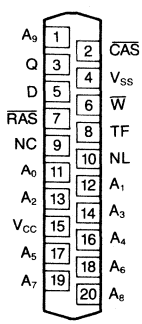


- **KM41C1001CJ**



Pin Names	Pin Function
A_0-A_9	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
TF	Test Function
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection
NL	No Lead

- **KM41C1001CZ**



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, and $\overline{CAS}$, Address Cycling @t_{RC} = min.)	KM41C1001C-6	I_{CC1}	—	70	mA
	KM41C1001C-7		—	65	mA
	KM41C1001C-8		—	60	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM41C1001C-6	I_{CC3}	—	70	mA
	KM41C1001C-7		—	65	mA
	KM41C1001C-8		—	60	mA
Nibble Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC} = min.)	KM41C1001C-6	I_{CC4}	—	55	mA
	KM41C1001C-7		—	50	mA
	KM41C1001C-8		—	45	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min.)	KM41C1001C-6	I_{CC6}	—	70	mA
	KM41C1001C-7		—	65	mA
	KM41C1001C-8		—	60	mA
Input Leakage Current (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3} Address can be changed maximum two times while $\overline{RAS}$ = V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CAS}$ = V_{IH}.

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance [D]	C_{IN1}	—	5	pF
Input Capacitance [A_0-A_9]	C_{IN1}	—	6	pF
Input Capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$]	C_{IN3}	—	7	pF
Output Capacitance [Q]	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ± 10%, See notes 1, 2)

Parameter	Symbol	KM41C1001C-6		KM41C1001C-7		KM41C1001C-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	130		150		170		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3, 4, 11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3, 4, 5
Access time from column address	t_{AA}		30		35		40	ns	3, 10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	

AC CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$, See notes 1, 2)

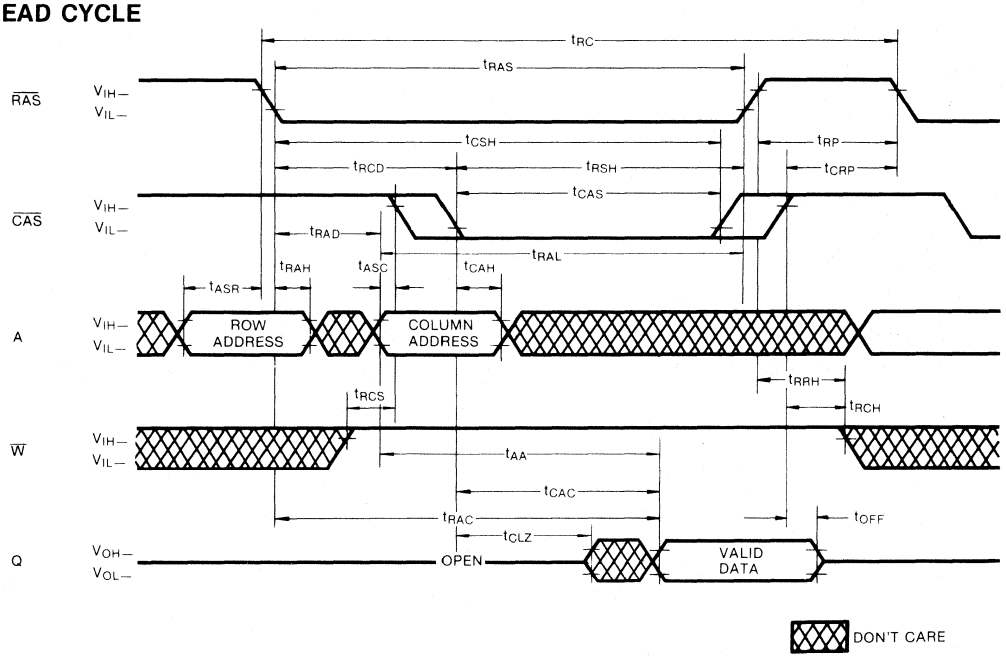
Parameter	Symbol	KM41C1001C-6		KM41C1001C-7		KM41C1001C-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		50		55		ns	6
Write command pulse width	t_{WP}	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (512 cycles)	t_{REF}		8		8		8	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	15		20		20		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	60		70		80		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	30		35		40		ns	8
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	15		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		25		30		ns	
Nibble mode cycle time	t_{NC}	40		40		40		ns	
Nibble mode read-write cycle time	t_{NRWC}	55		60		60		ns	
Nibble mode access time	t_{NCAC}		15		20		20	ns	
Nibble mode $\overline{CAS}$ pulse width	t_{NCAS}	15		20		20		ns	
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	10		10		10		ns	
Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	15		20		20		ns	
Nibble mode $\overline{CAS}$ to $\overline{W}$ delay time	t_{NCWD}	15		20		20		ns	
Nibble mode $\overline{W}$ to $\overline{RAS}$ lead time	t_{NRWL}	15		15		15		ns	
Nibble mode $\overline{W}$ to $\overline{CAS}$ lead time	t_{NCWL}	15		15		15		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
12. Normal operation requires the "T.F" pin to be connected to V_{SS} or TTL logic low level or left unconnected on the printed wiring board.
13. When the "T.F" pin is connected to a defined positive voltage, the internal test function may be activated. Contact Samsung for specific operational details of the "test function."
14. In a test mode read cycle, the value of t_{RAC}, t_{CAC}, t_{AA} is delayed for 3ns.

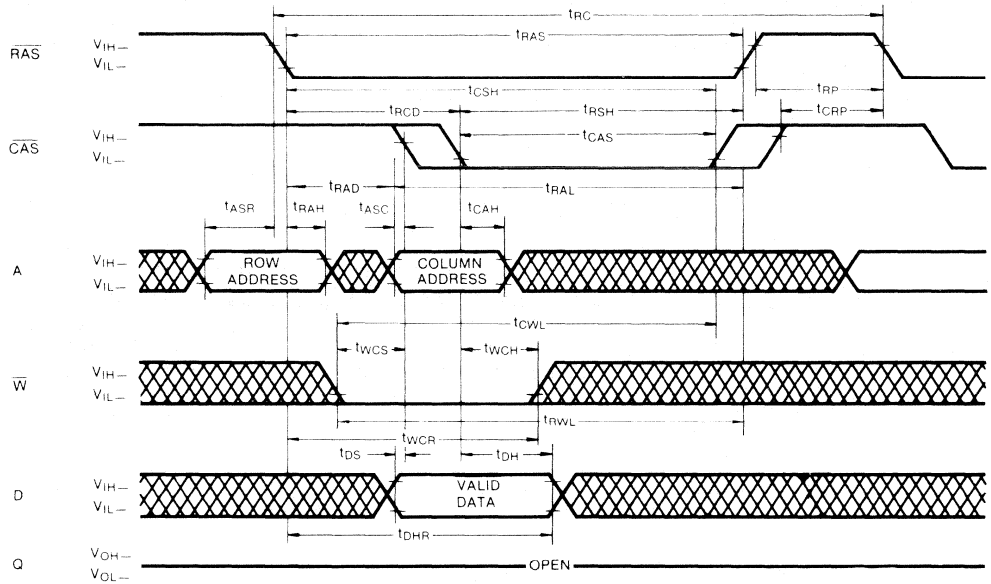
TIMING DIAGRAMS

READ CYCLE

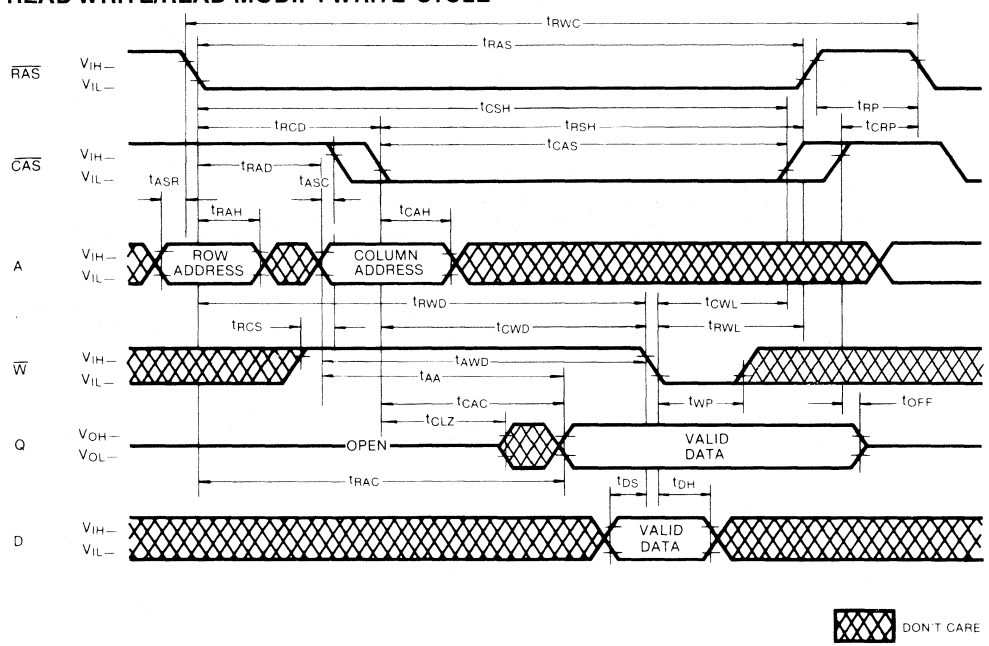


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

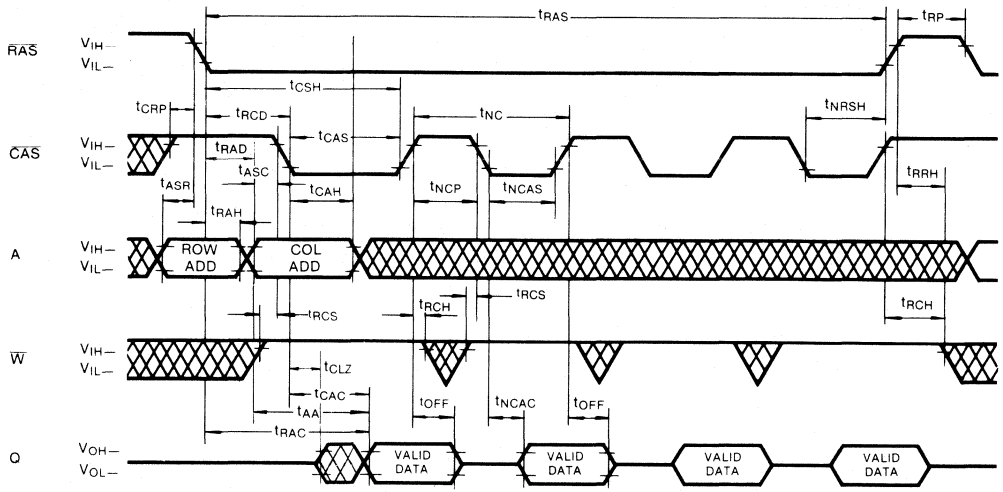


READ-WRITE/READ-MODIFY-WRITE CYCLE

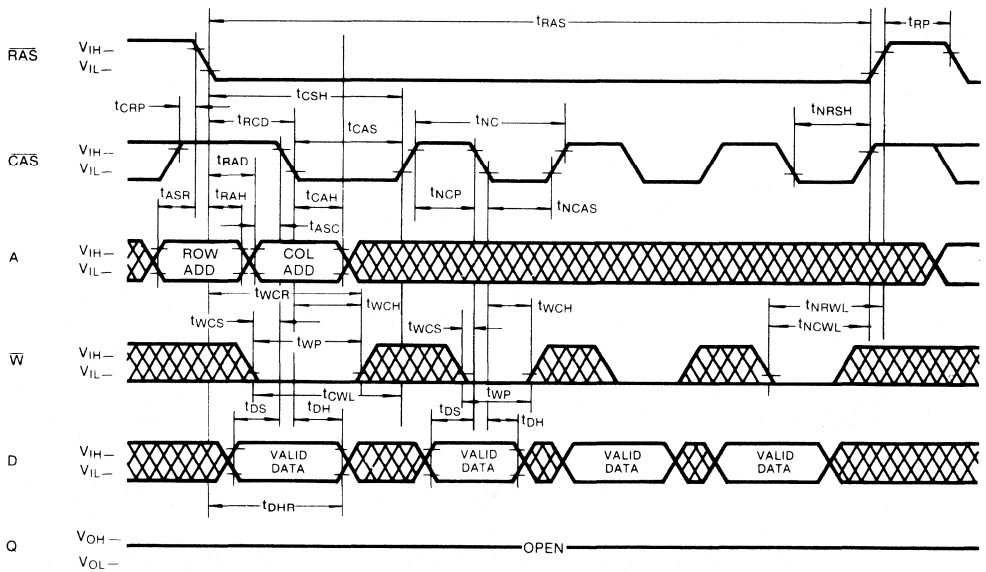


TIMING DIAGRAMS (Continued)

NIBBLE MODE READ CYCLE



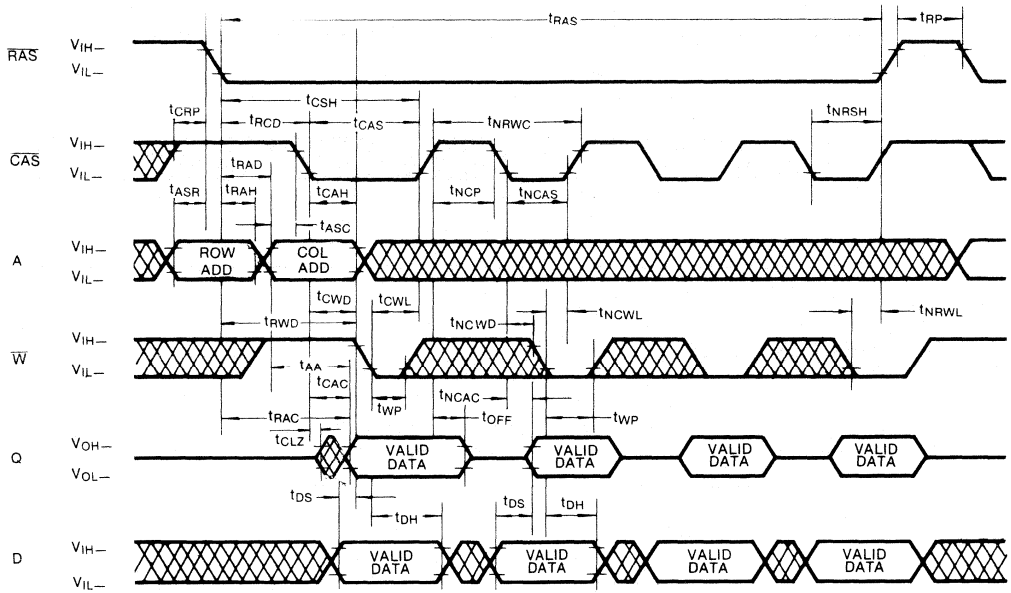
NIBBLE MODE WRITE CYCLE (EARLY WRITE)



DON'T CARE

TIMING DIAGRAMS (Continued)

NIBBLE MODE READ-WRITE CYCLE

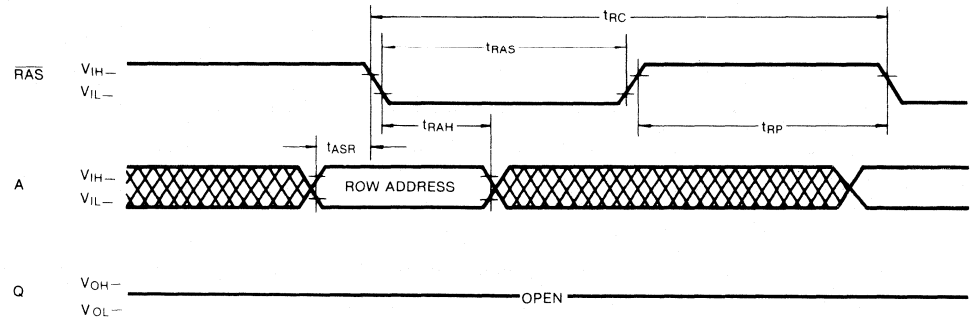


DON'T CARE

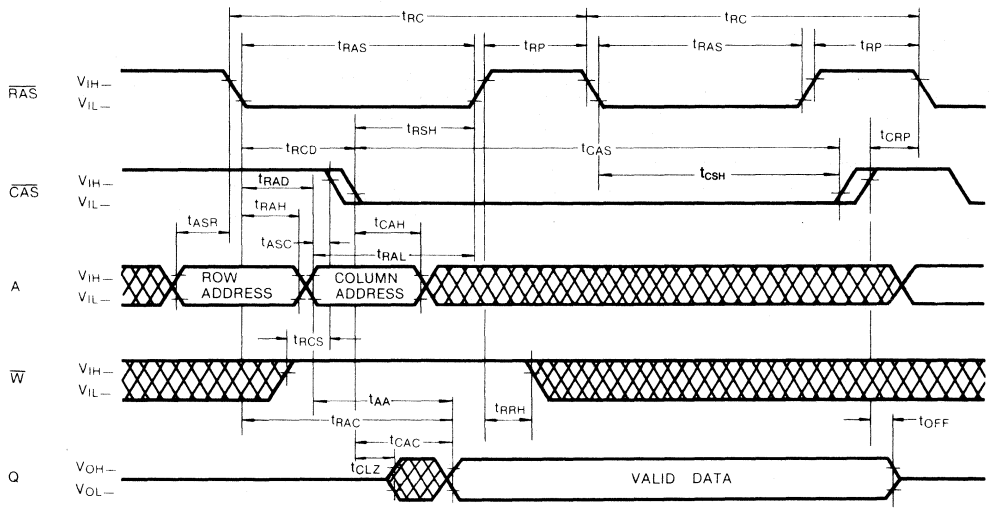
TIMING DIAGRAMS (Continued)

$\overline{RAS}$-ONLY REFRESH CYCLE

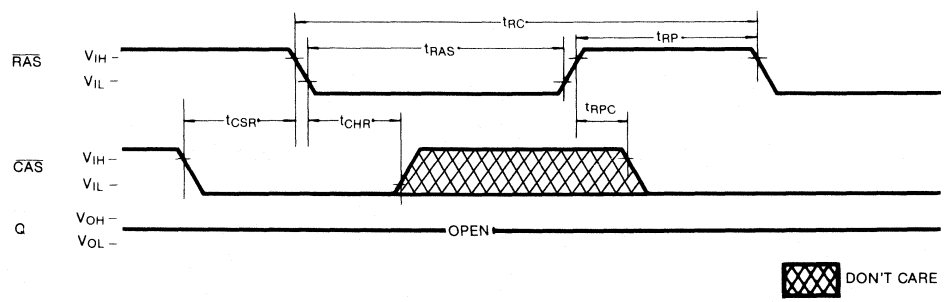
Note: $\overline{CAS}$ = V_{IH}, $\overline{W}$,D, A_9 = Don't Care



HIDDEN REFRESH CYCLE

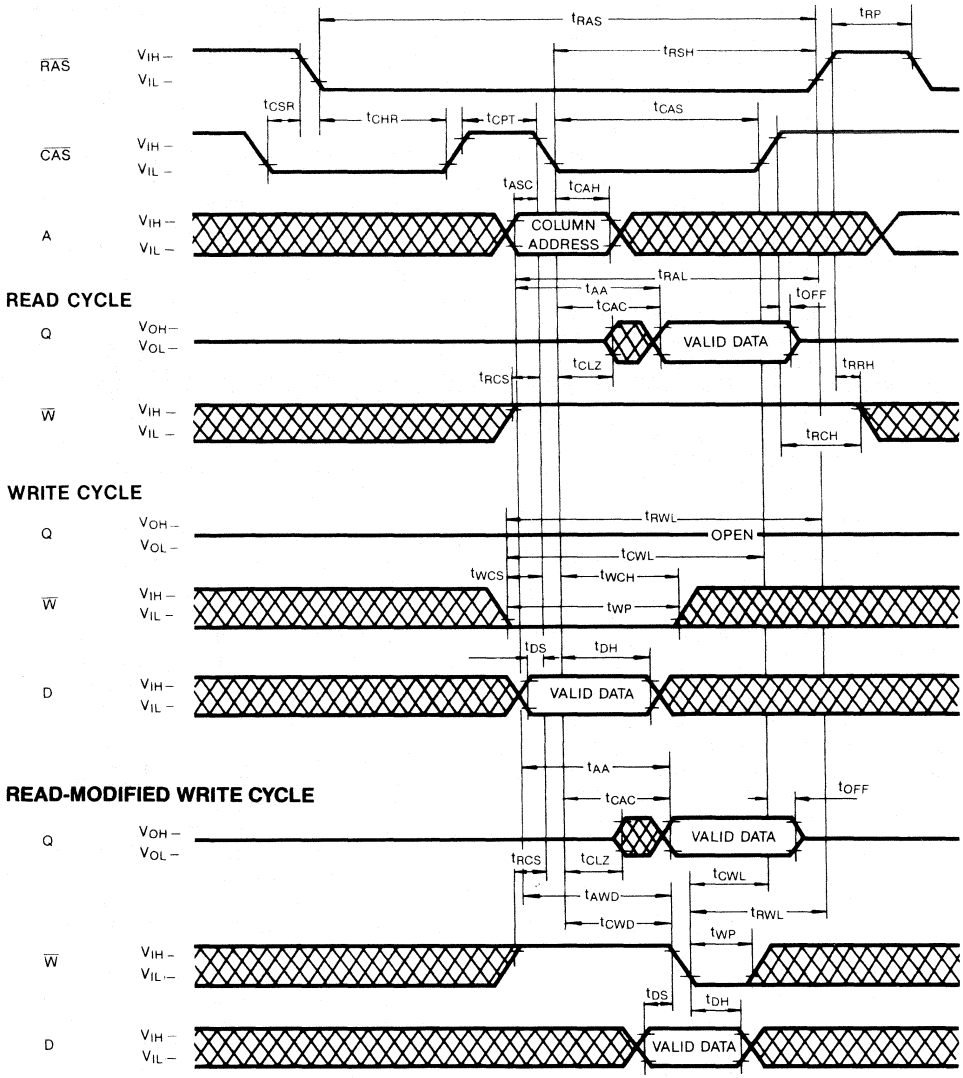


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM41C1001C contains 1,048,576 memory locations. Twenty address bits are required to address a particular memory location. Since the KM41C1001C has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM41C1001C begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C1001C cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C1001C begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input(W) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM41C1001C can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{CWD} and t_{AWD} are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C1001C has a tri-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C1001C operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C1001C is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 8 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A0-A8). The state of address A9 is ignored during refresh.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C1001C has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C1001C hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C1001C by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

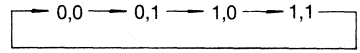
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A0 through A8 are supplied by the on-chip refresh counter. The A9 bit is set low internally.

Nibble Mode

The KM41C1001C has Nibble mode capability. Nibble mode operation allows high speed serial read, write or read-modify-write access of 4 consecutive bits. The first of 4 bits is accessed in the usual manner. The remaining nibble bits are accessed by toggling $\overline{CAS}$ high then low while $\overline{RAS}$ remains low.

The 4 bits of data that may be accessed during Nibble mode are determined by the lower 9 row address bits (RA_0-RA_8) and 9 column address bits (CA_0-CA_8). The two address bits, CA_9 and RA_9 are used to select 1 of the 4 nibble bits for initial access. The remaining nibble bits are accessed by toggling $\overline{CAS}$ with $\overline{RAS}$ held low. Each high-low $\overline{CAS}$ transition will internally increment the nibble address (CA_9, RA_9) as shown in the following diagram with RA_9 being the least significant bit.



If more than 4 bits are accessed during Nibble mode, the address sequence will wrap around and repeat. If any bit is written during Nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on a subsequent access, the new data will be written into the selected cell location.

A Nibble mode cycle can be a read, write, or read-modify-write cycle. Any combinations of reads and writes or read-modify-writes are allowed.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM41C1001C could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

DEVICE OPERATION (Continued)

Termination

The lines from the TTL driver circuits to the KM41C1001C inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C1001C input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

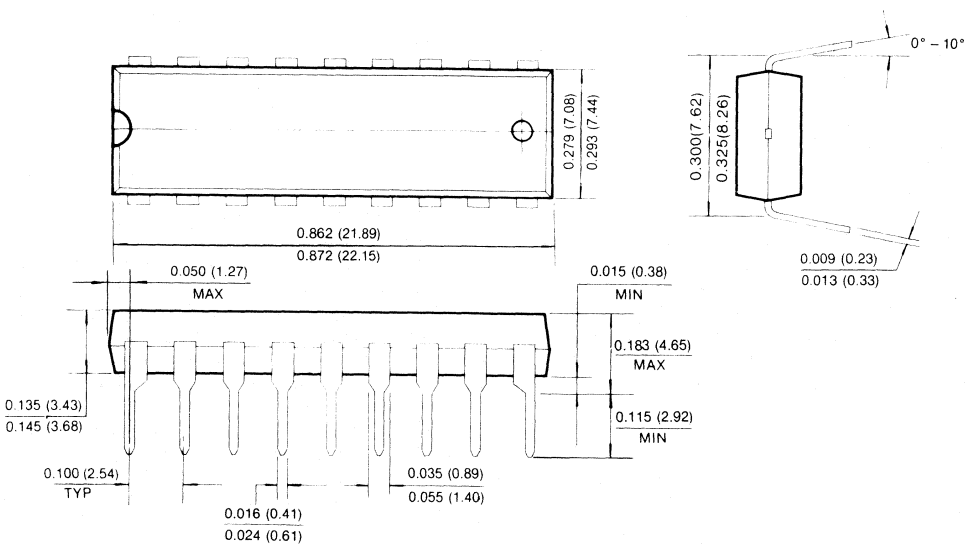
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM41C1001C using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C1001C and they supply much of the current used by the KM41C1001C during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

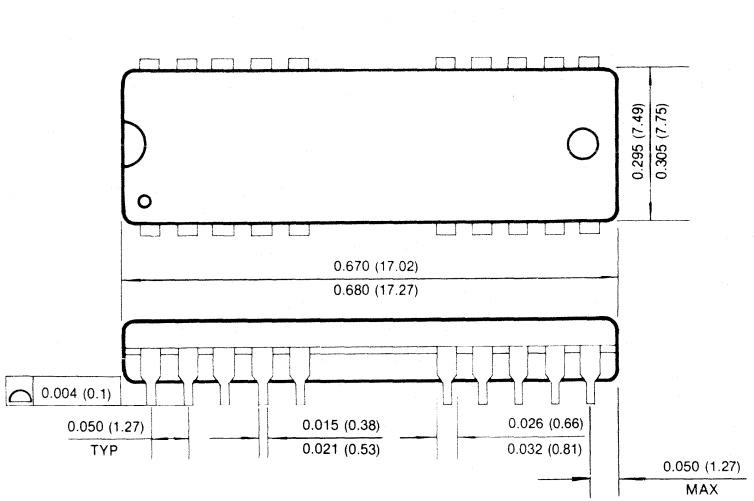
Units: Inches (Millimeters)



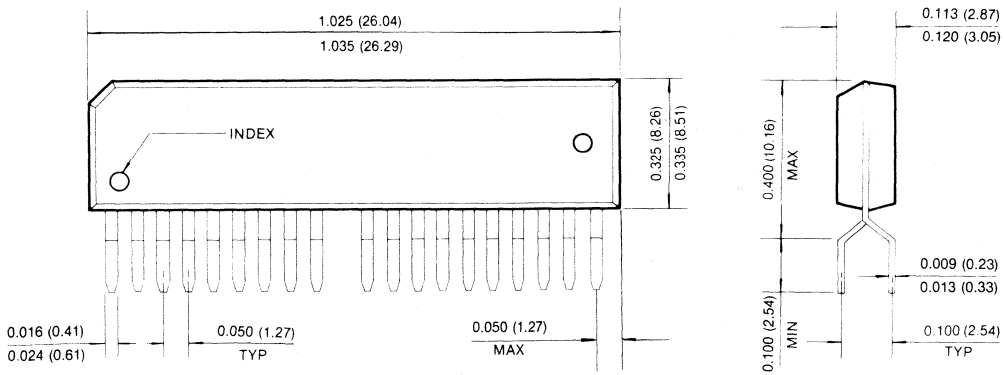
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



1,048,576 x 1 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C1002C-6	60ns	15ns	110ns
KM41C1002C-7	70ns	20ns	130ns
KM41C1002C-8	80ns	20ns	150ns

- **Static Column Mode operation**
- **$\overline{CS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Write**
- **Single +5V ± 10% power supply**
- **512 cycles/8ms refresh**
- **256K x 4 fast test mode**
- **JEDEC standard pinout**
- **Available in Plastic DIP, SOJ and ZIP**

GENERAL DESCRIPTION

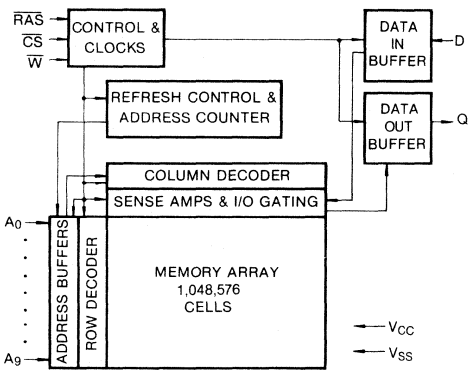
The Samsung KM41C1002C is a CMOS high speed 1,048,576 x 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics, and high performance microprocessor systems.

The KM41C1002C features Static Column Mode operation which allows high speed random or Sequential access within a row. Static Column Mode operation offers high performance while relaxing many critical system timing requirements for fast usable speed.

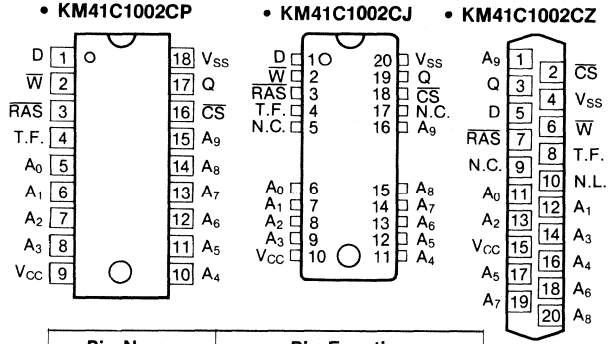
$\overline{CS}$-before-$\overline{RAS}$ Refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

The KM41C1002C is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A_0-A_9	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
T.F.	Test Function
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection
N.L.	No Lead

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling @t_{RC} = min.)	KM41C1002C-6	I_{CC1}	—	70	mA
	KM41C1002C-7		—	65	mA
	KM41C1002C-8		—	60	mA
Standby Current ($\overline{RAS}$ = $\overline{CS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current ($\overline{CS}$ = V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM41C1002C-6	I_{CC3}	—	70	mA
	KM41C1002C-7		—	65	mA
	KM41C1002C-8		—	60	mA
Static Column Mode Current ($\overline{RAS}$ = $\overline{CS}$ = V_{IL}, Address Cycling @t_{PC} = min.)	KM41C1002C-6	I_{CC4}	—	55	mA
	KM41C1002C-7		—	50	mA
	KM41C1002C-8		—	45	mA
Standby Current ($\overline{RAS}$ = $\overline{CS}$ = V_{CC} − 0.2V)		I_{CC5}	—	1	mA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{RC} = min.)	KM41C1002C-6	I_{CC6}	—	70	mA
	KM41C1002C-7		—	65	mA
	KM41C1002C-8		—	60	mA
Input Leakage Current (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. I_{CC1}, I_{CC3} Address can be changed maximum two times while $\overline{RAS}$ = V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CS}$ = V_{IH}.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	—	5	pF
Input Capacitance (A_0-A_9)	C_{IN2}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$)	C_{IN3}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$, See notes 1, 2)

Parameter	Symbol	KM41C1002C-6		KM41C1002C-7		KM41C1002C-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	130		150		170		ns	
Static column mode cycle time	t_{SC}	35		40		45		ns	
Static column mode read-write cycle time	t_{SRWC}	65		75		85		ns	
Access time from RAS	t_{RAC}		60		70		80	ns	3,4,11,15
Access time from CS	t_{CAC}		15		20		20	ns	3,4,5,15
Access time from column address	t_{AA}		30		35		40	ns	3,11,15
Access time from last write	t_{ALW}		60		70		80	ns	3,12
$\overline{CS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Output data hold time from column address	t_{AOH}	5		5		5		ns	
Output data enable time from W	t_{OW}		25		25		25	ns	
Output data hold time from W	t_{WOH}	0		0		0		ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width (static column mode)	t_{RASC}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CS}$ pulse width	t_{CS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	15	100,000	20	100,000	20	100,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
$\overline{CS}$ precharge time (static column mode)	t_{CP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	

AC CHARACTERISTICS (Continued)

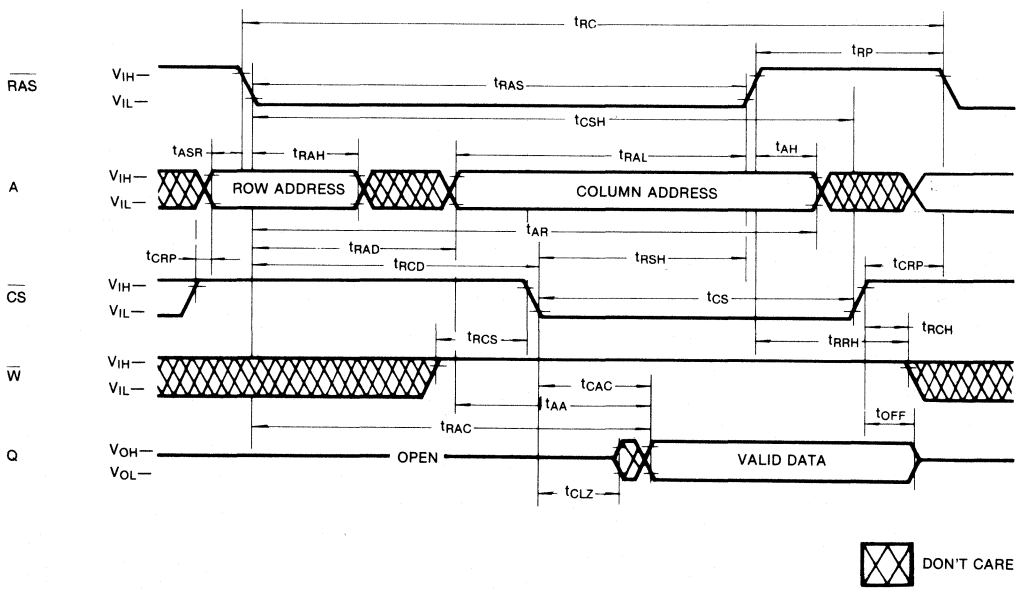
Parameter	Symbol	KM41C1002C-6		KM41C1002C-7		KM41C1002C-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Write address hold time referenced to $\overline{RAS}$	t_{AWR}	50		55		60		ns	6
Column address hold time referenced to $\overline{RAS}$	t_{AR}	70		80		90		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Column address hold time referenced to $\overline{RAS}$ rise	t_{AH}	5		5		5		ns	
Last write to column address delay time	t_{LWAD}	20	30	20	35	20	40	ns	12
Last write to column address hold time	t_{AHLW}	60		70		80		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	50		55		60		ns	6
Write command pulse width	t_{WP}	15		15		15		ns	
Write command inactive time	t_{WI}	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		15		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (512 cycles)	t_{REF}		8		8		8	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CS}$ to $\overline{W}$ delay time	t_{CWD}	15		15		15		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	60		70		80		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	30		35		40		ns	8
$\overline{CS}$ setup time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{SCR}	5		5		5		ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	15		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CS}$ hold time	t_{RPC}	5		5		5		ns	
Refresh counter test $\overline{CS}$ precharge time	t_{CPT}	15		15		15		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AWR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data out will contain the data read from the selected address. if neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met, t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. Operation within the t_{LWAD}(max) limit insures that t_{ALW}(max) can be met. t_{LWAD}(max) is specified as a reference point only. If t_{LWAD} is greater than the specified t_{LWAD}(max) limit, then access time is controlled by t_{AA}.
13. Normal operation requires the 'T.F.' pin to be connected to V_{SS} or TTL logic low level or left unconnected on the printed wiring board.
14. When the 'T.F.' pin is connected to a defined positive voltage, the internal test function may be activated.
15. In a test mode read cycle, the value of t_{RAC}, t_{CAC}, t_{AA} is delayed for 3ns.

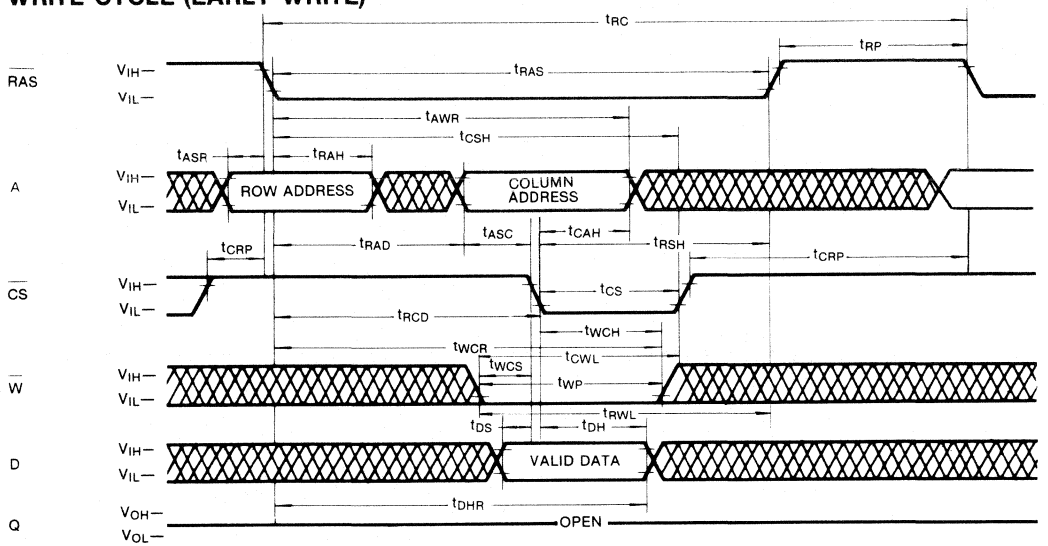
TIMING DIAGRAMS

READ CYCLE

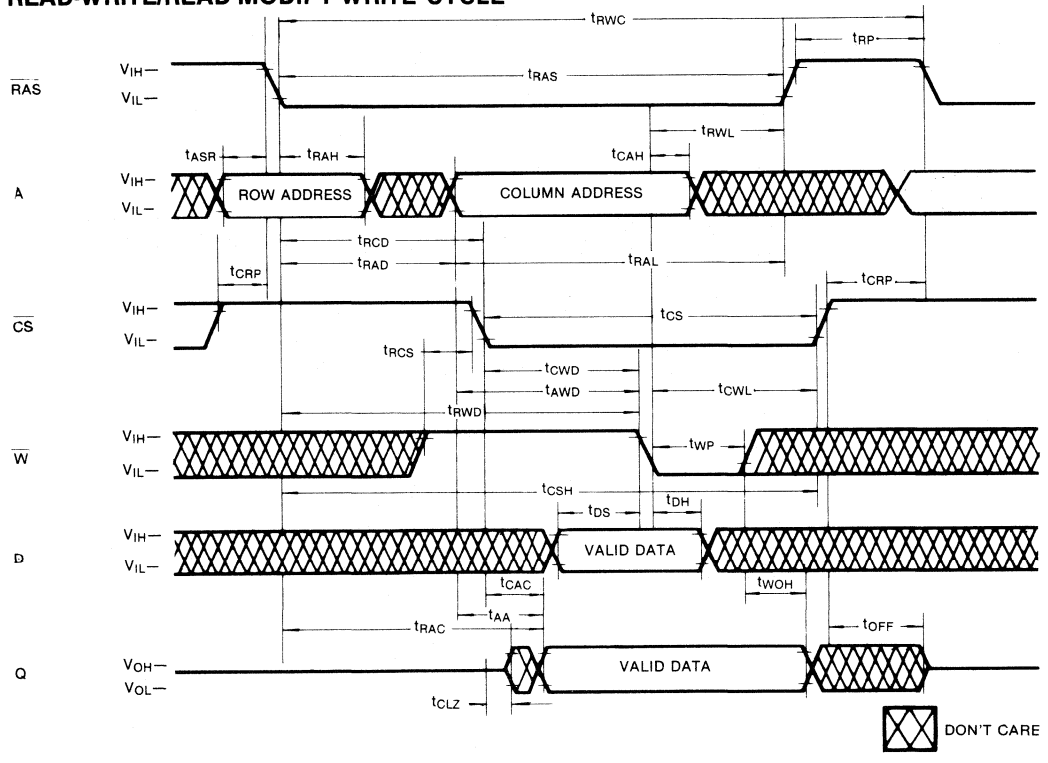


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

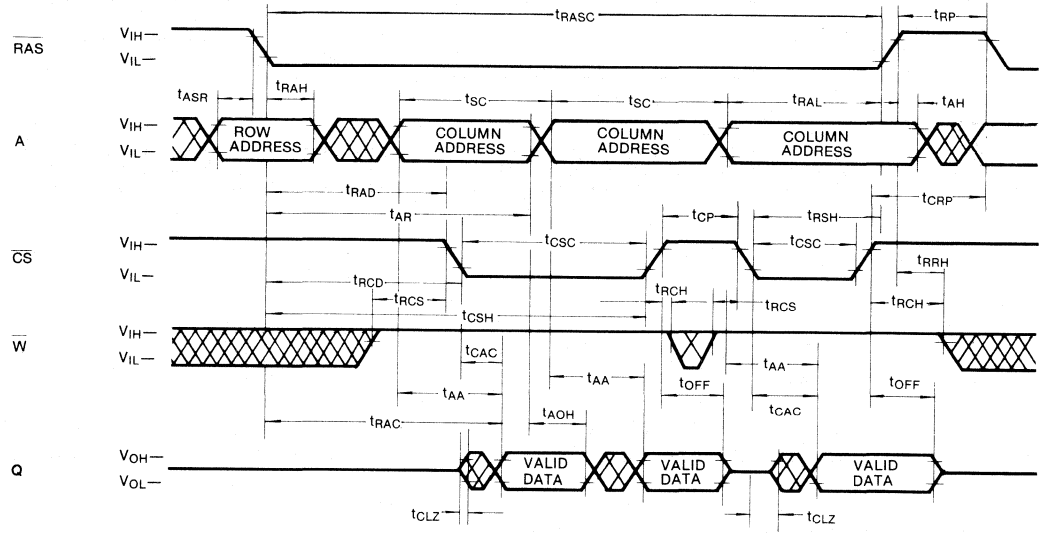


READ-WRITE/READ-MODIFY-WRITE CYCLE

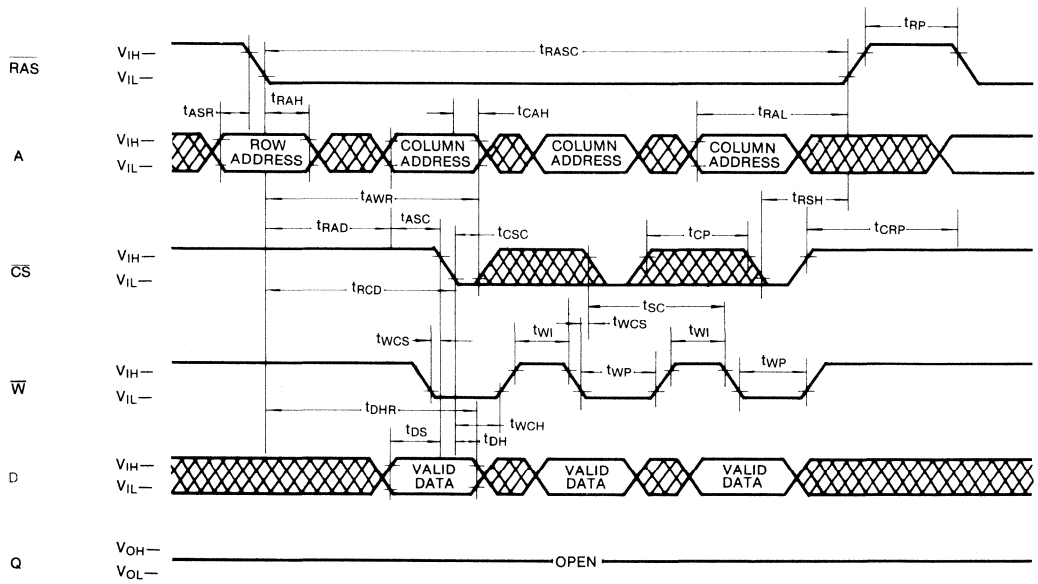


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ CYCLE

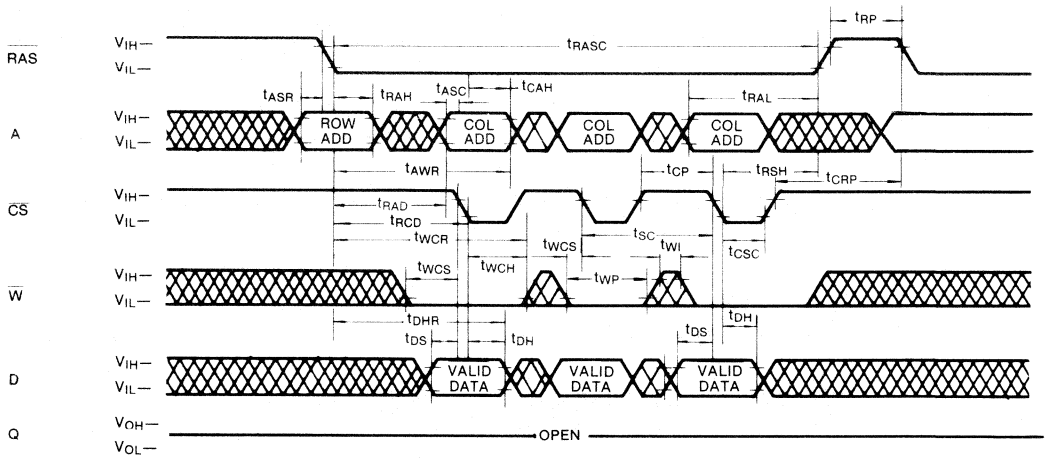


STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ controlled early write)

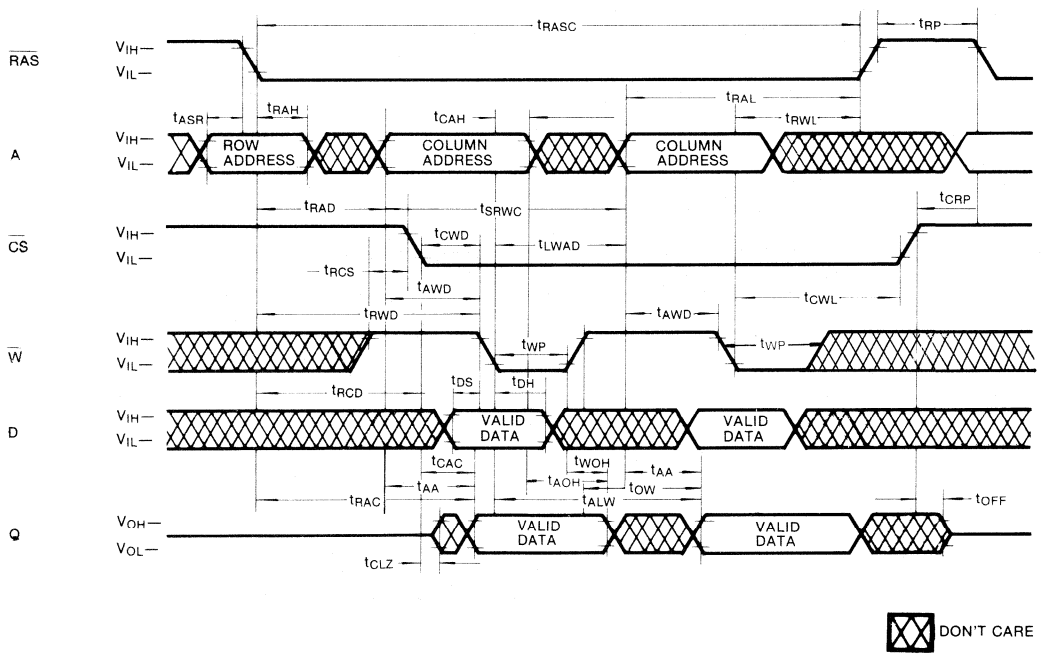


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ controlled early write)

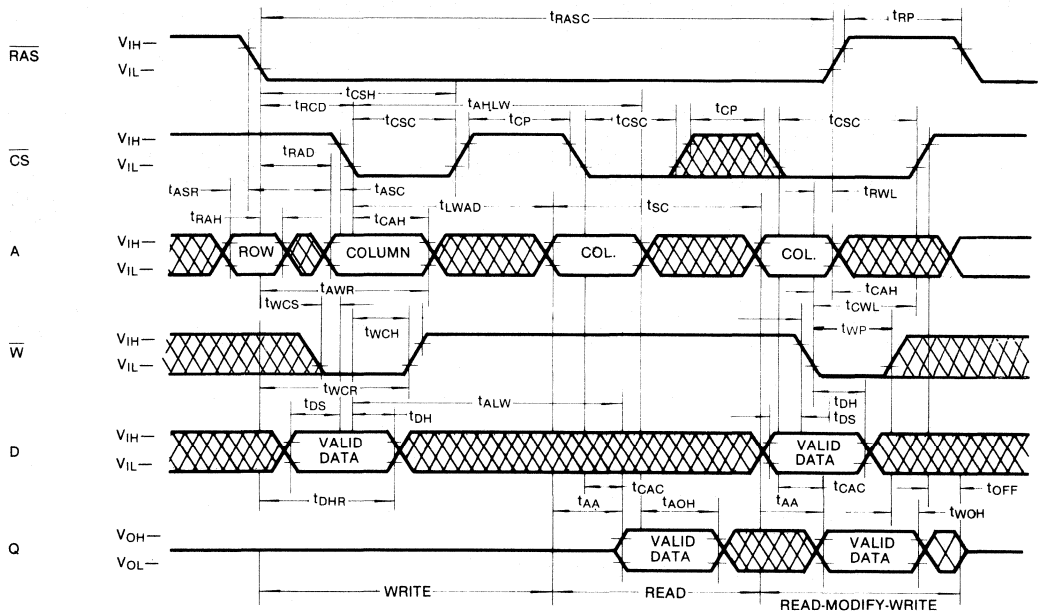


STATIC COLUMN MODE READ-WRITE CYCLE



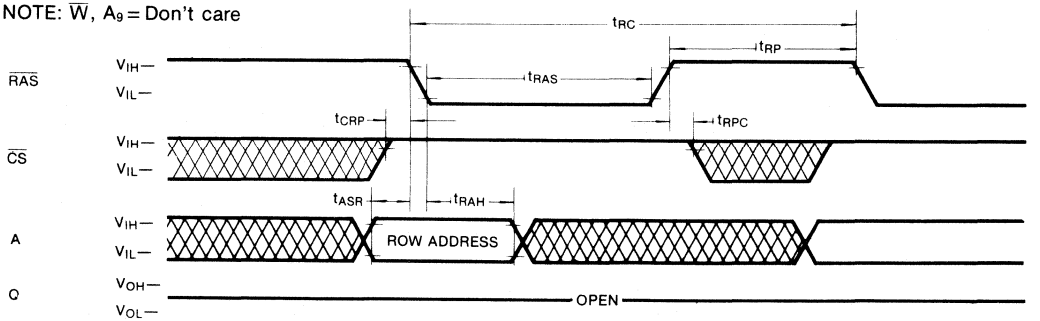
TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE MIXED CYCLE



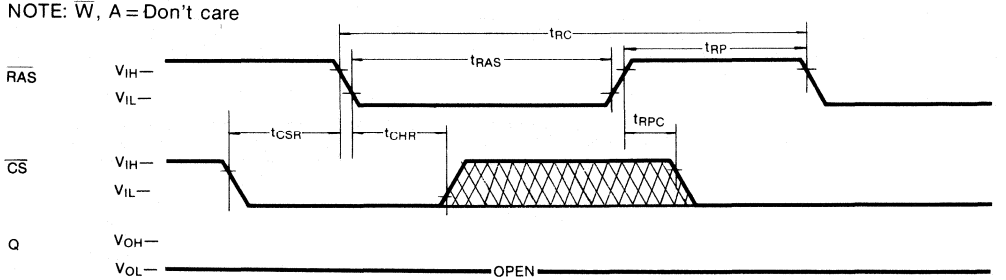
RAS-ONLY REFRESH CYCLE

NOTE: W, A_9 = Don't care



CS-BEFORE-RAS REFRESH CYCLE

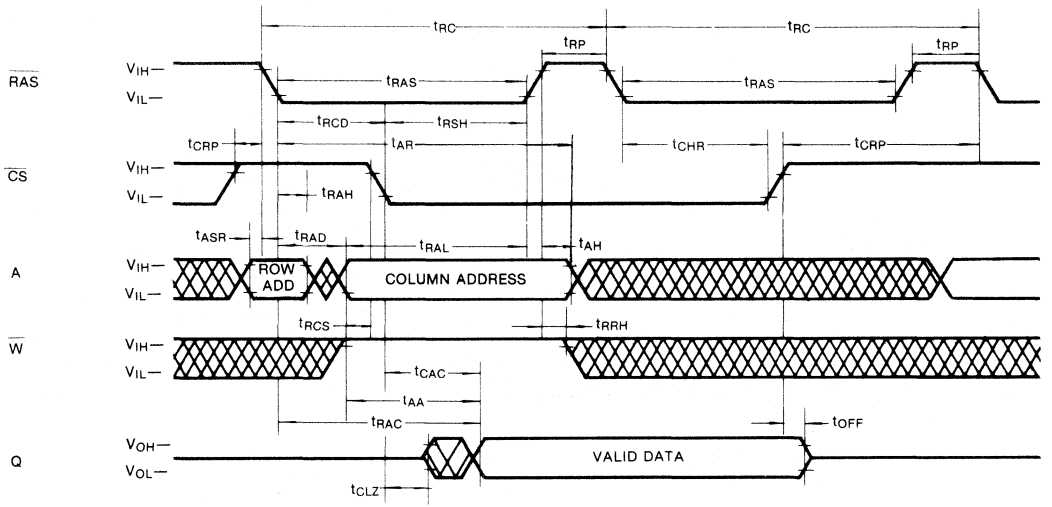
NOTE: W, A = Don't care



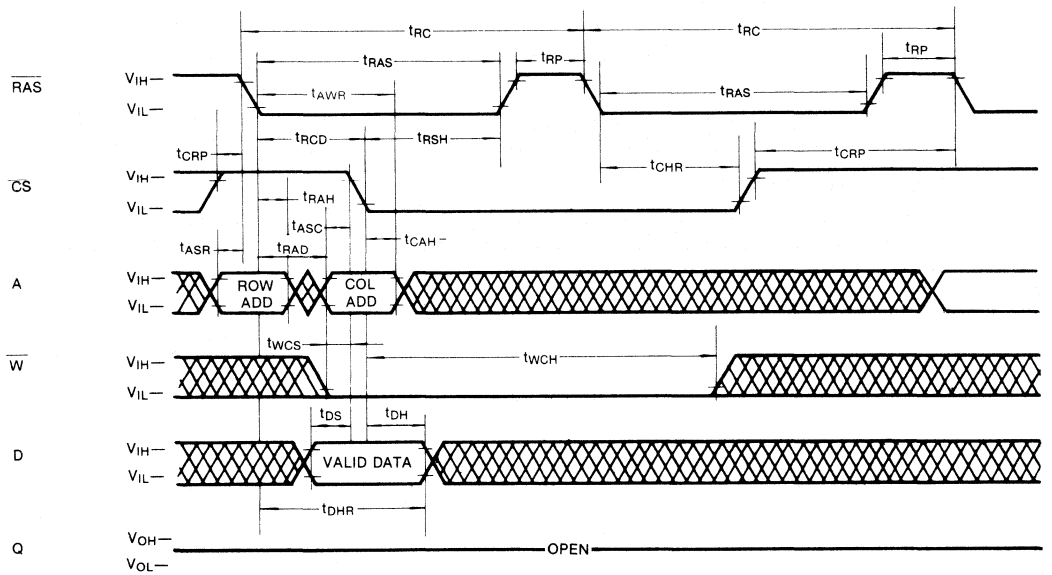
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



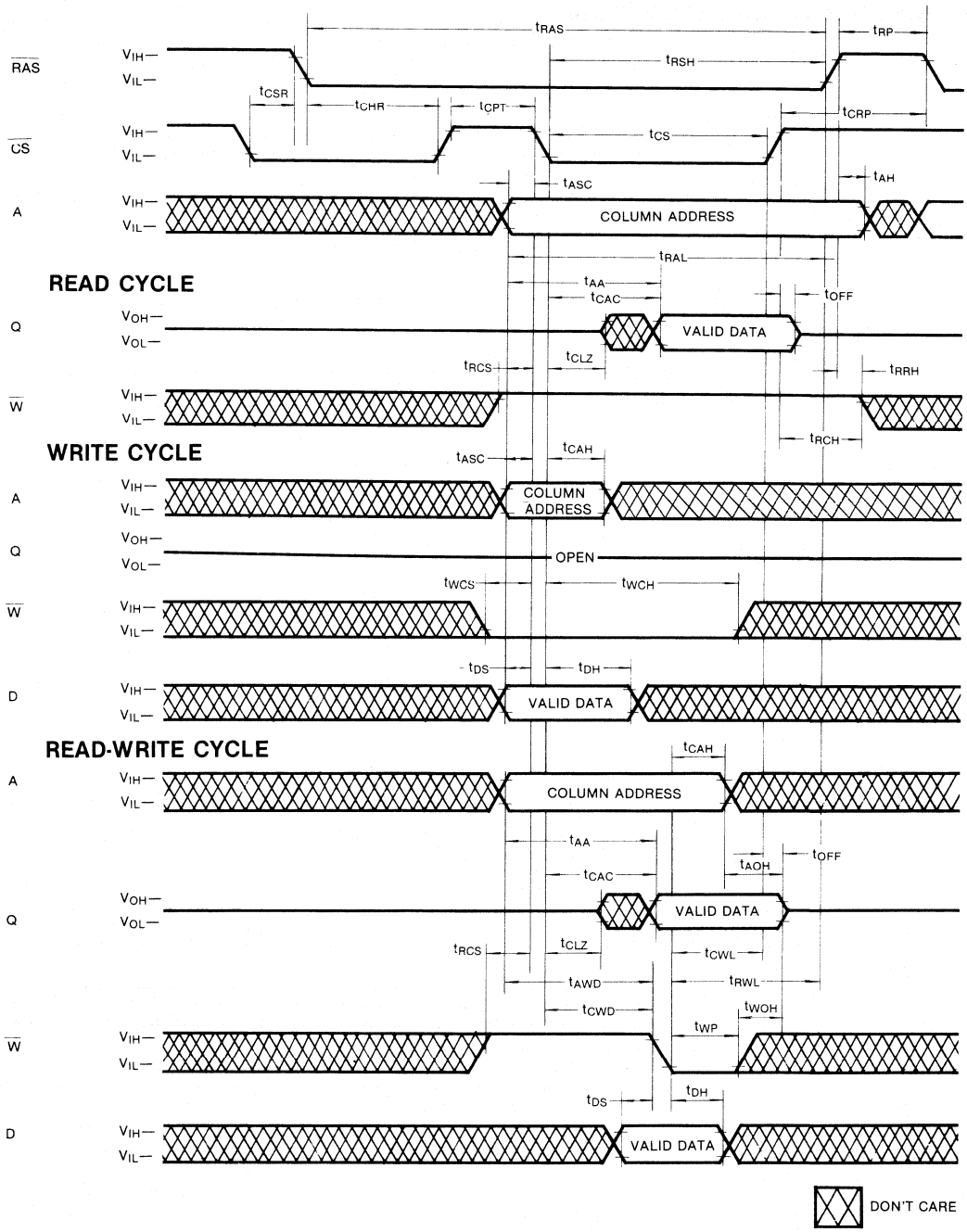
HIDDEN REFRESH CYCLE (WRITE)



DON'T CARE

TIMING DIAGRAMS (Continued)

$\overline{CS}$-BEFORE-$\overline{RAS}$ BEFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM41C1002C contains 1,048,576 memory locations. Twenty address bits are required to address a particular memory location. Since the KM41C1002C has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the chip select input ($\overline{CS}$) and the valid row and column address inputs.

Operation of the KM41C1002C begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CS}$. This is the beginning of any KM41C1002C cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths are specified by t_{RAS}(min) and t_{CS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C1002C begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CS}$ cycle. If $\overline{CS}$ goes low before t_{RCD}(max), the access time to valid data is specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CS}$ and on the valid column address transition.

If $\overline{CS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM41C1002C can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{CWD} and t_{AWD} are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C1002C has a three-state output buffer which is controlled by $\overline{CS}$. Whenever $\overline{CS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C1002C operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Static Column Mode Read, Static Column Mode Read-Modify-Write.

DEVICE OPERATION (Continued)

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Static Column Mode Write, $\overline{CS}$-before-$\overline{RAS}$ Refresh, $\overline{CS}$-only cycle.
Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C1002C is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 8 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CS}$ remains high. This cycle must be repeated for each row.

$\overline{CS}$-before-$\overline{RAS}$ Refresh: The KM41C1002C has $\overline{CS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CS}$ active time and cycling $\overline{RAS}$. The KM41C1002C hidden refresh cycle is actually a $\overline{CS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C1002C by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CS}$-before-$\overline{RAS}$ refresh is the preferred method.

Static Column Mode

Static Column Mode allows high speed read, write or read-modity-write random access to all the memory cells within a selected row. Operation within a selected row is similar to a static RAM. The read, write or readmodify-write cycles may be mixed in any order.
A Static Column mode read cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{W} = V_{IH}$ and $\overline{RAS} = V_{IL}$.

A Static Column mode write cycle starts as a normal cycle. Additional cells within the selected ro are written by applying a new column address while $\overline{RAS} = V_{IL}$ and toggiling either $\overline{W}$ or $\overline{CS}$. The data is written into the cell trigered by the latter fallin edge of $\overline{W}$ or $\overline{CS}$.

$\overline{CS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address — Bits A_0 through A_8 are supplied by the on-chip refresh counter. The A_9 bit is set low internally.

Column Address — Bits A_0 through A_9 are strobed-in by the falling edge of $\overline{CS}$ as in a normal memory clce.

Suggested $\overline{CS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 512 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 512 times so that highs are written into the 512 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM41C1002C could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200μsec is required after power-up

DEVICE OPERATION (Continued)

followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41C1002C inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C1002C input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM41C1002C using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C1002C and they supply much of the current used by the KM41C1002C during cycling.

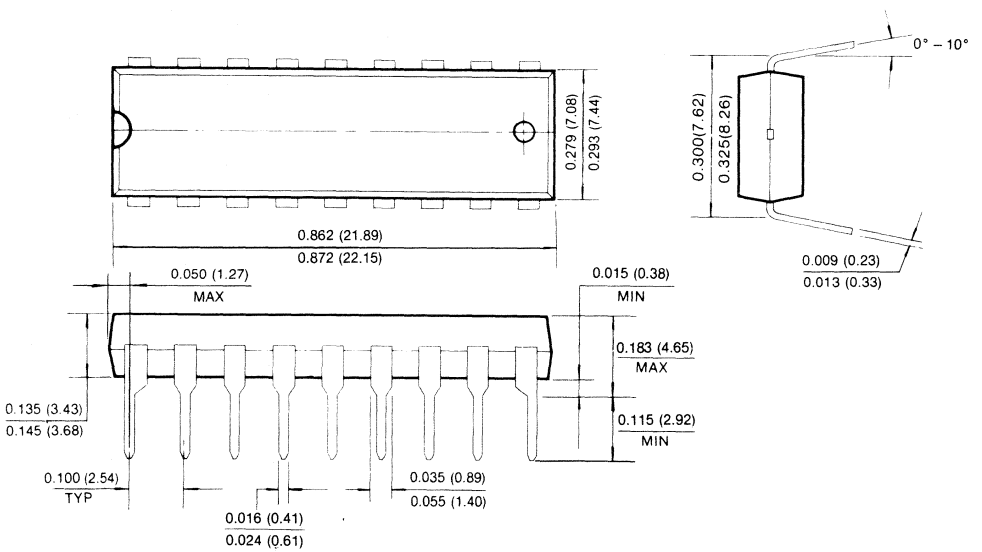
In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

2

PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

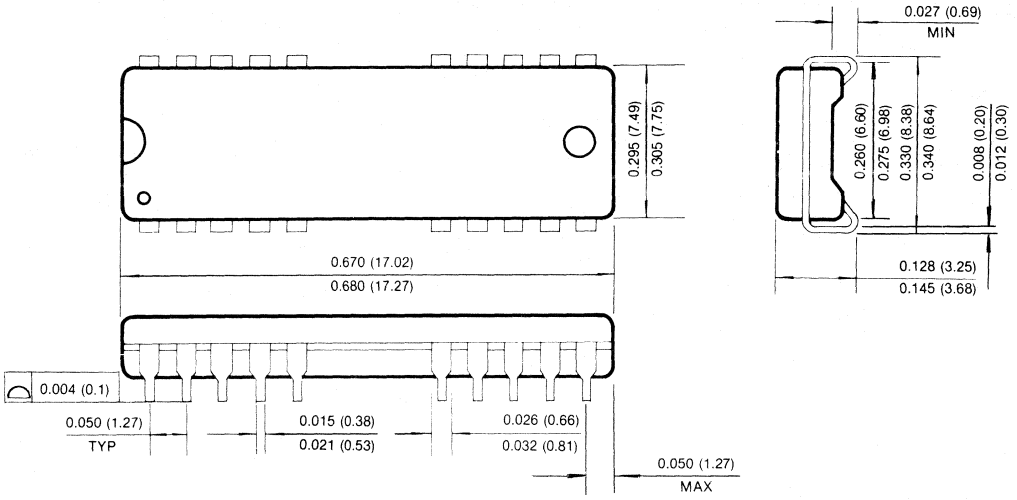
Units: Inches (Millimeters)



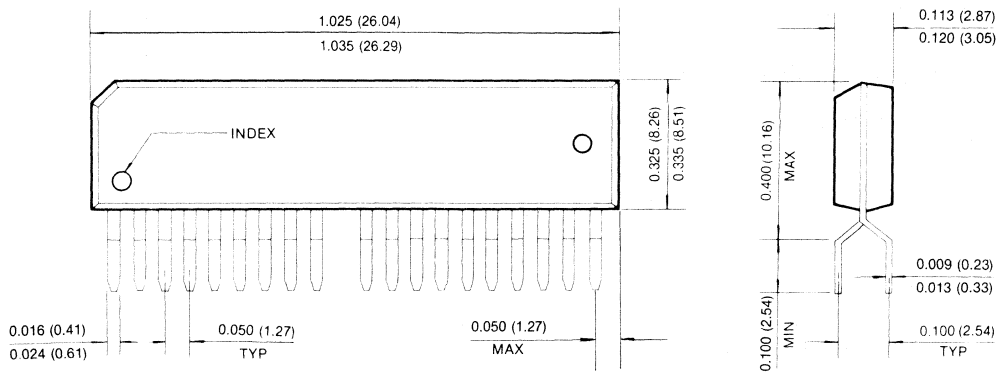
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



256K×4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C256C-6	60ns	15ns	110ns
KM44C256C-7	70ns	20ns	130ns
KM44C256C-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or Output Enable Controlled Write**
- **Single +5V ± 10% power supply**
- **512 cycles/8ms refresh**
- **JEDEC Standard pinout**
- **Available in Plastic DIP, SOJ, ZIP, TSOP (I), TSOP (II) packages.**

GENERAL DESCRIPTION

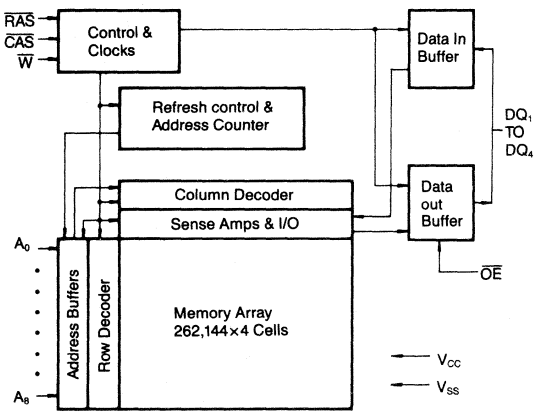
The Samsung KM44C256C is a CMOS high speed 262,144×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance microprocessor computers.

The KM44C256C features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44C256C is fabricated using Samsung's advanced CMOS process.

2

FUNCTIONAL BLOCK DIAGRAM

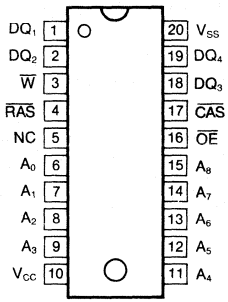


ORDERING INFORMATION

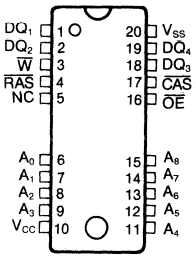
Part No.	Access Time	Package
KM44C256CP-6	60ns	300 mil, 20DIP
KM44C256CP-7	70ns	
KM44C256CP-8	80ns	
KM44C256CJ-6	60ns	300 mil, 20SOJ
KM44C256CJ-7	70ns	
KM44C256CJ-8	80ns	
KM44C256CZ-6	60ns	400 mil, 20ZIP
KM44C256CZ-7	70ns	
KM44C256CZ-8	80ns	
KM44C256CV-6	60ns	20 TOSP (I) (Forward)
KM44C256CV-7	70ns	
KM44C256CV-8	80ns	
KM44C256CVR-6	60ns	20 TOSP (I) (Reverse)
KM44C256CVR-7	70ns	
KM44C256CVR-8	80ns	
KM44C256CT-6	60ns	20 TOSP (II) (Forward)
KM44C256CT-7	70ns	
KM44C256CT-8	80ns	
KM44C256CTR-6	60ns	20 TOSP (II) (Reverse)
KM44C256CTR-7	70ns	
KM44C256CTR-8	80ns	

PIN CONFIGURATION (Top Views)

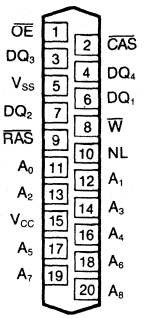
• **KM44C256CP**



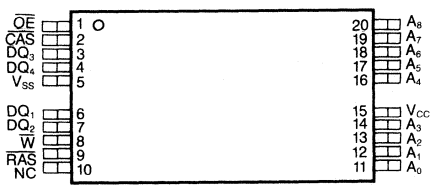
• **KM44C256CJ**



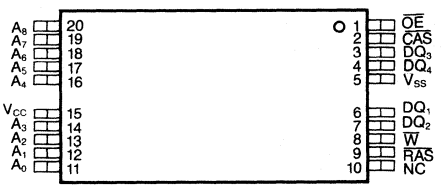
• **KM44C256CZ**



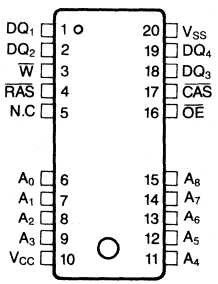
• **KM44C256CV**



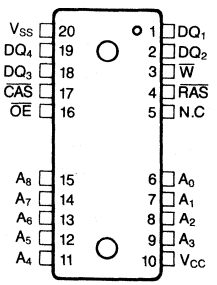
• **KM44C256CVR**



• **KM44C256CT**



• **KM44C256CTR**



Pin Names	Name Function
A_0-A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
DQ_1-DQ_4	Data In/Data Out
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection
NL	No Lead

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, and $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM44C256C-6	I_{CC1}	—	70	mA
	KM44C256C-7		—	65	mA
	KM44C256C-8		—	60	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @ t_{RC}=min.)	KM44C256C-6	I_{CC3}	—	70	mA
	KM44C256C-7		—	65	mA
	KM44C256C-8		—	60	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Address Cycling @ t_{PC}=min.)	KM44C256C-6	I_{CC4}	—	55	mA
	KM44C256C-7		—	50	mA
	KM44C256C-8		—	45	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC}-0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM44C256C-6	I_{CC6}	—	70	mA
	KM44C256C-7		—	65	mA
	KM44C256C-8		—	60	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3} Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance [A_0-A_8]	C_{IN1}	—	6	pF
Input Capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	—	7	pF
Output Capacitance [DQ_1-DQ_4]	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ± 10%, See notes 1, 2)

Parameter	Symbol	KM44C256C-6		KM44C256C-7		KM44C256C-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		175		195		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3, 4, 11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3, 4, 5
Access time from column address	t_{AA}		30		35		40	ns	3, 10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	

AC CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$, See notes 1, 2)

Parameter	Symbol	KM44C256C-6		KM44C256C-7		KM44C256C-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	50		55		60		ns	6
Write command pulse width	t_{WP}	15		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (512 cycles)	t_{REF}		8		8		8	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		45		45		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		95		105		ns	8
Column address to $\overline{W}$ dealy time	t_{AWD}	55		60		65		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	15		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		35		40	ns	3
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	80		85		90		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	15		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	15		20		20		ns	

NOTES

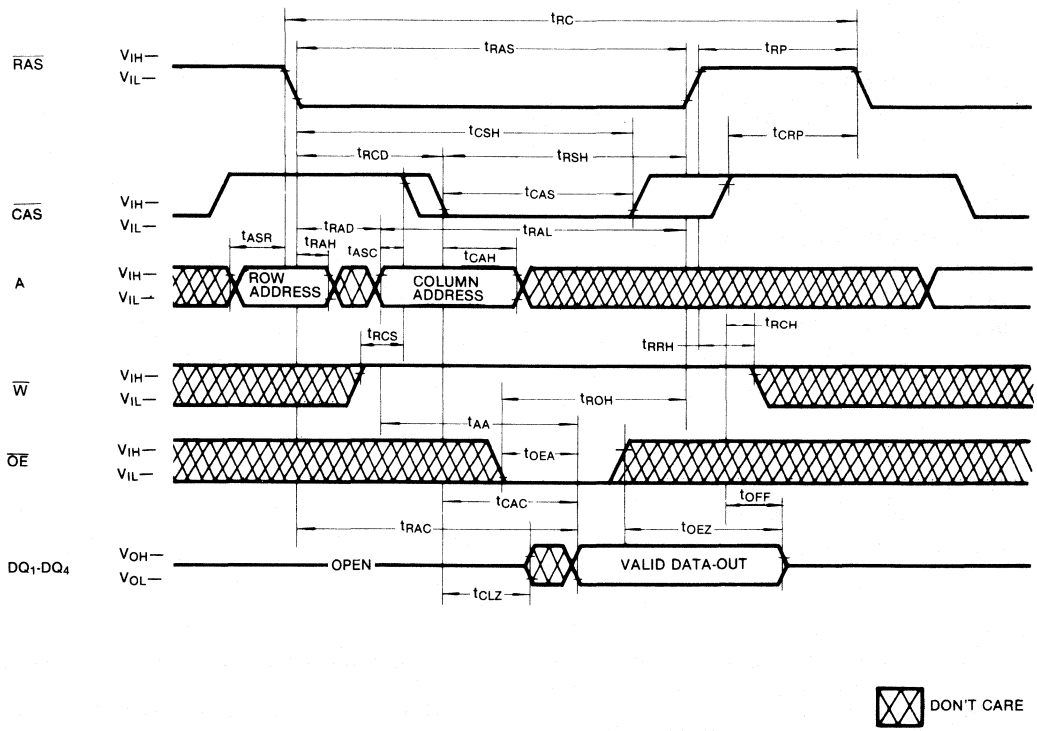
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

NOTES (Continued)

5. Assumes that $t_{RCD} \geq t_{RCD}(max)$.
6. t_{WCR}, t_{DHR} are referenced to $t_{RAD}(max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}(min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(min)$, $t_{RWD} \geq t_{RWD}(min)$ and $t_{AWD} \geq t_{AWD}(min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RAC}(max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled by t_{AA}.

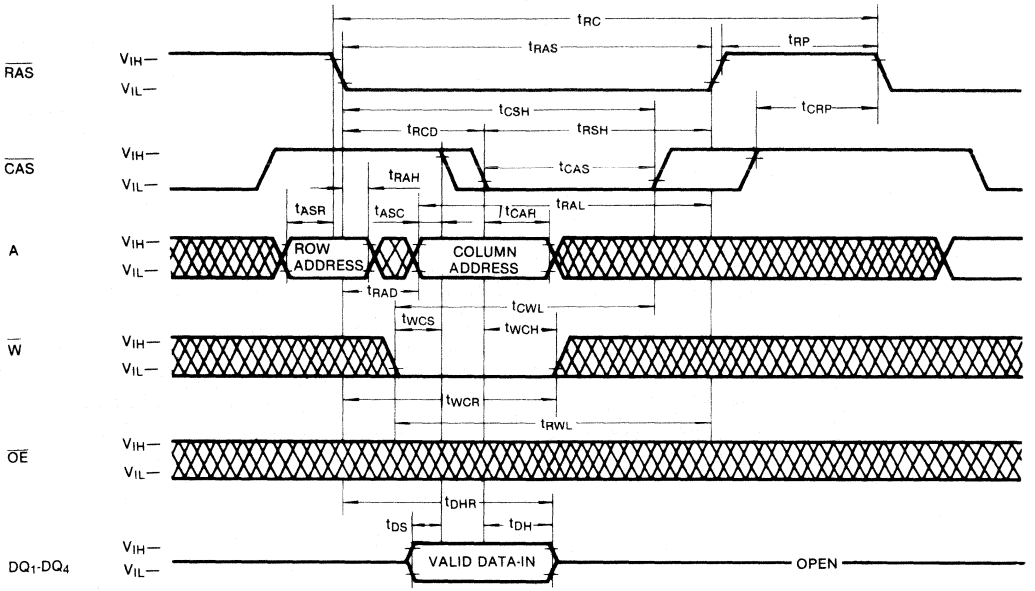
TIMING DIAGRAMS

READ CYCLE

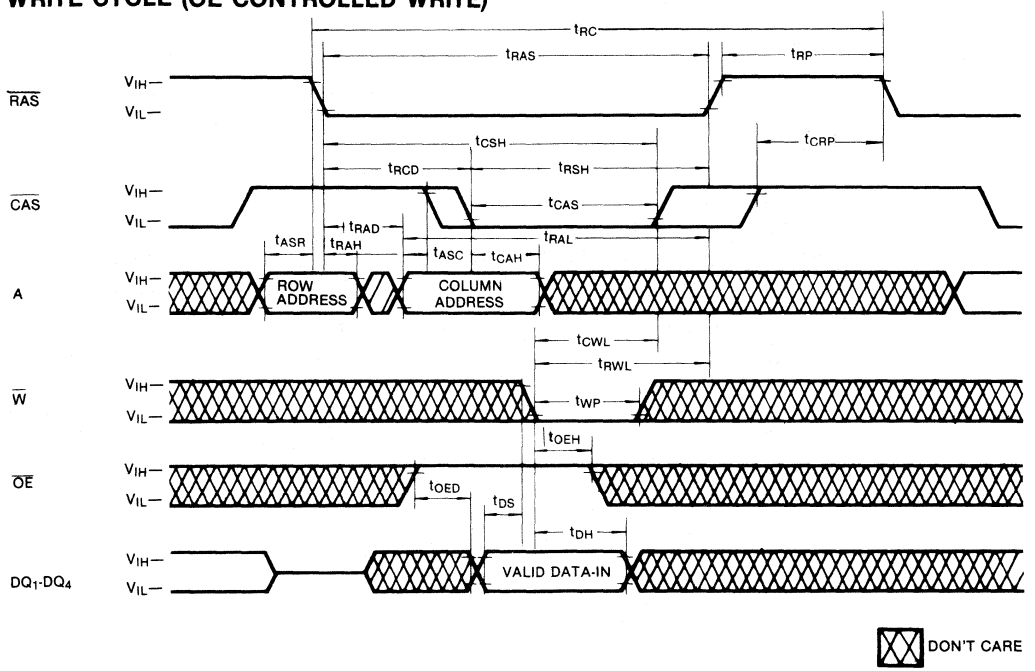


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

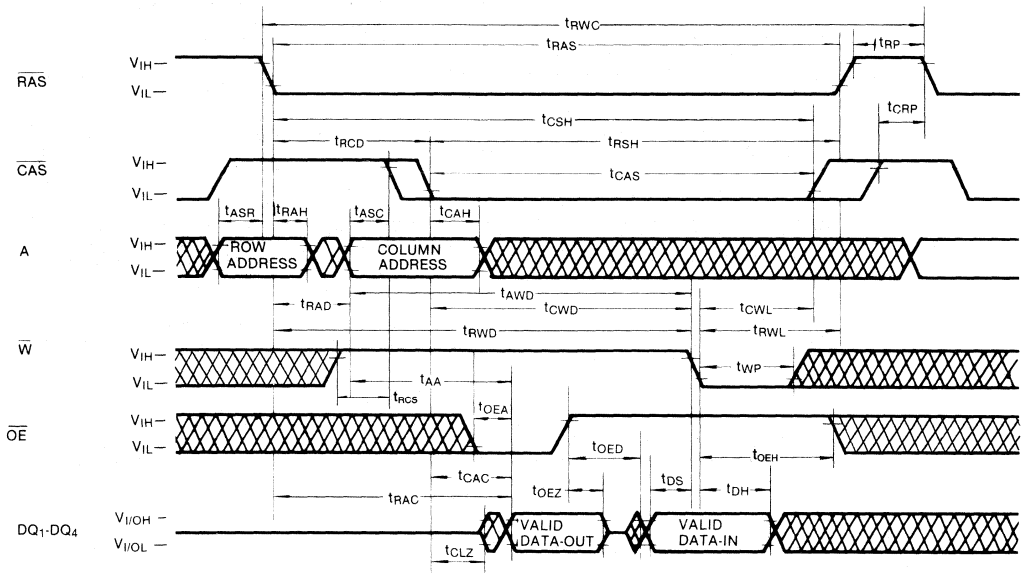


WRITE CYCLE (OE CONTROLLED WRITE)

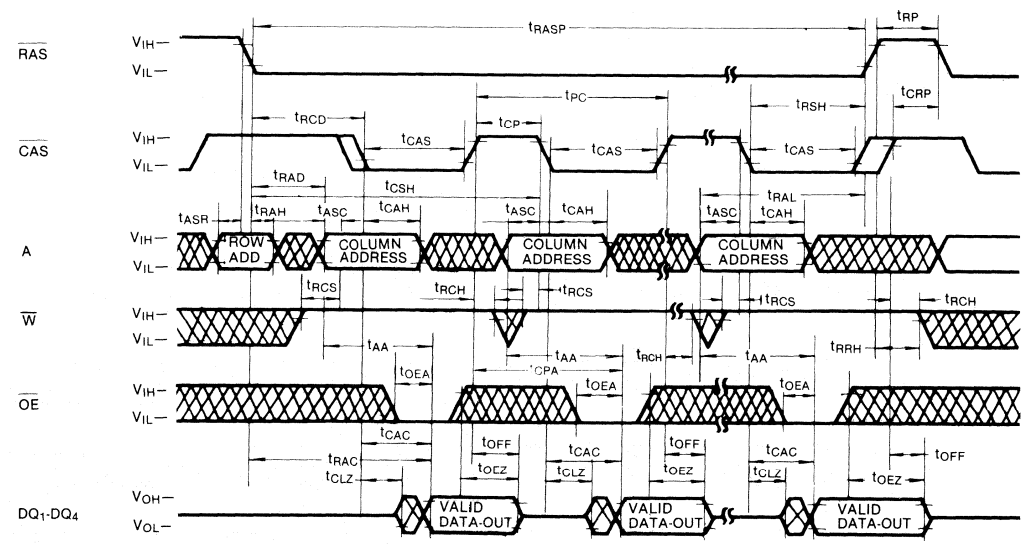


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



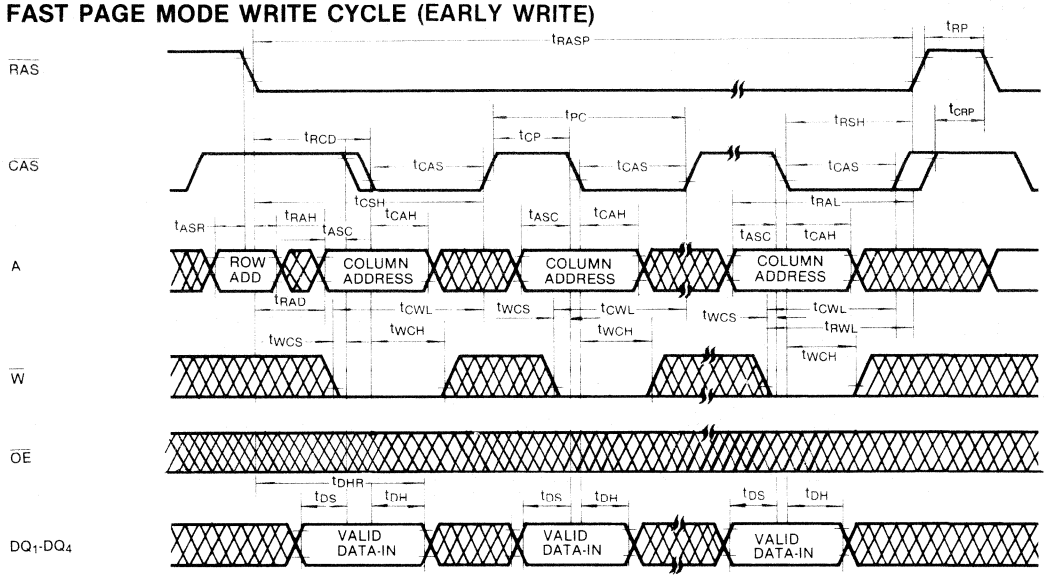
FAST PAGE MODE READ CYCLE



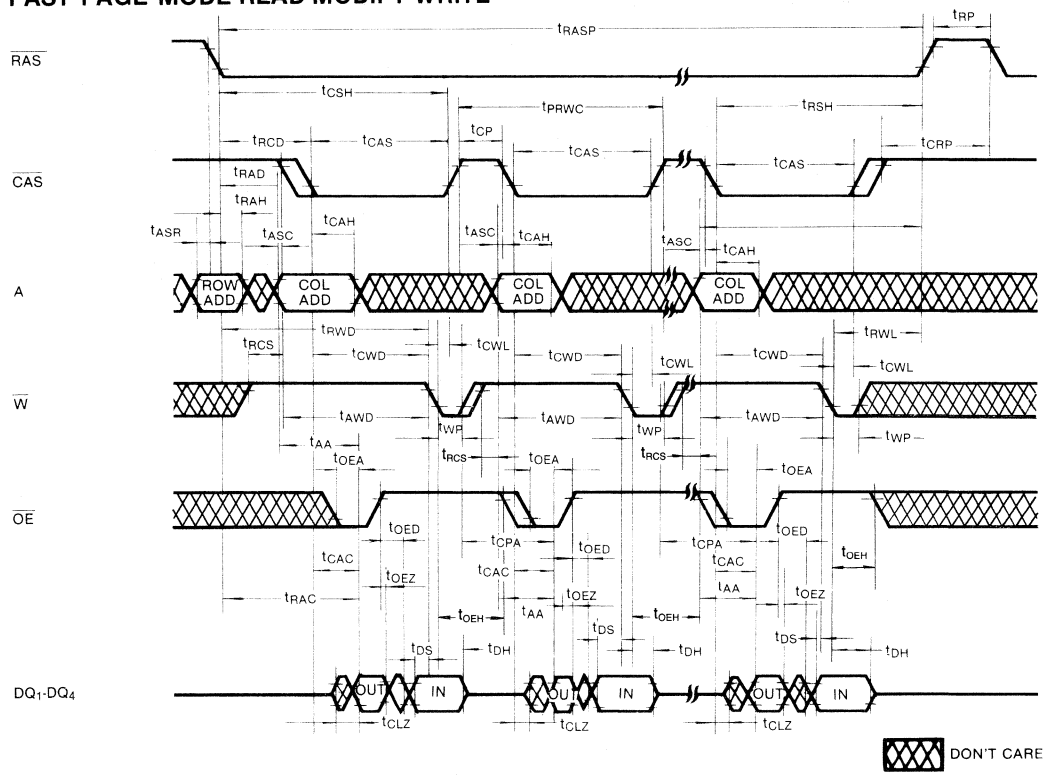
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



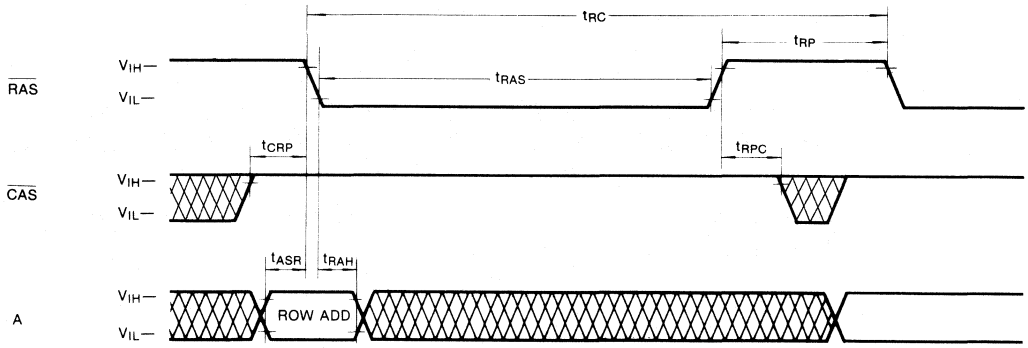
FAST PAGE MODE READ-MODIFY-WRITE



TIMING DIAGRAMS (Continued)

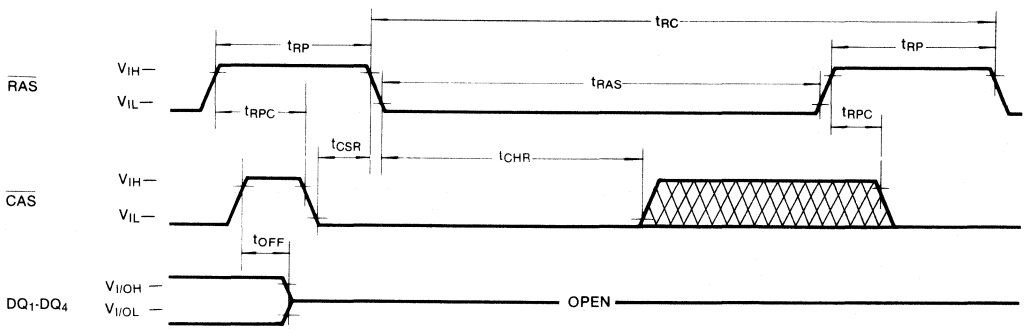
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

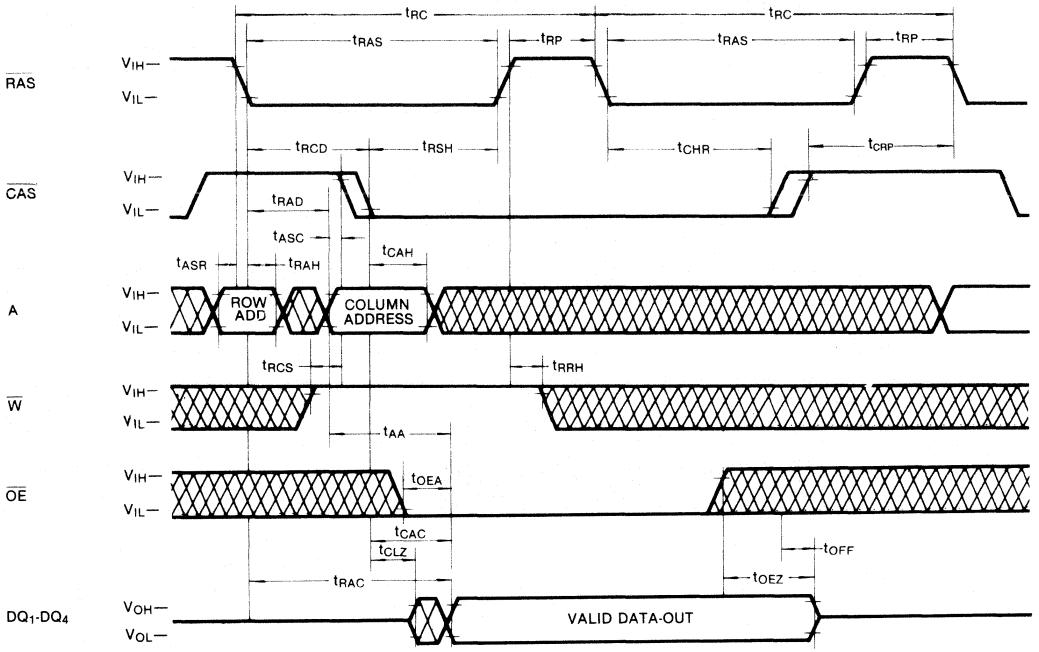
Note: $\overline{W}$, $\overline{OE}$, A = Don't care



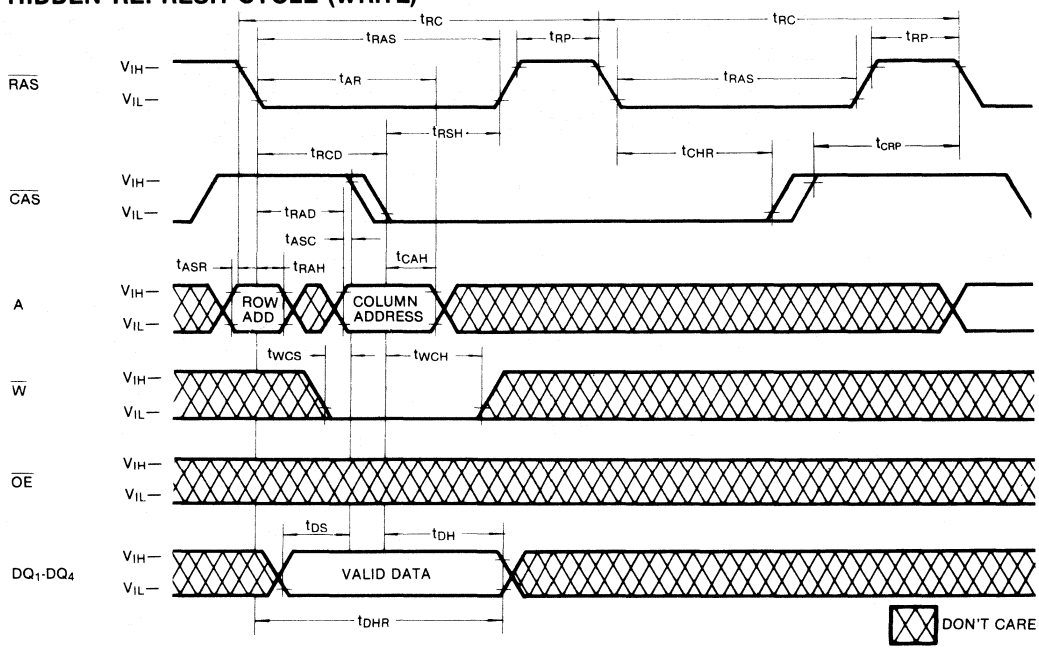
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

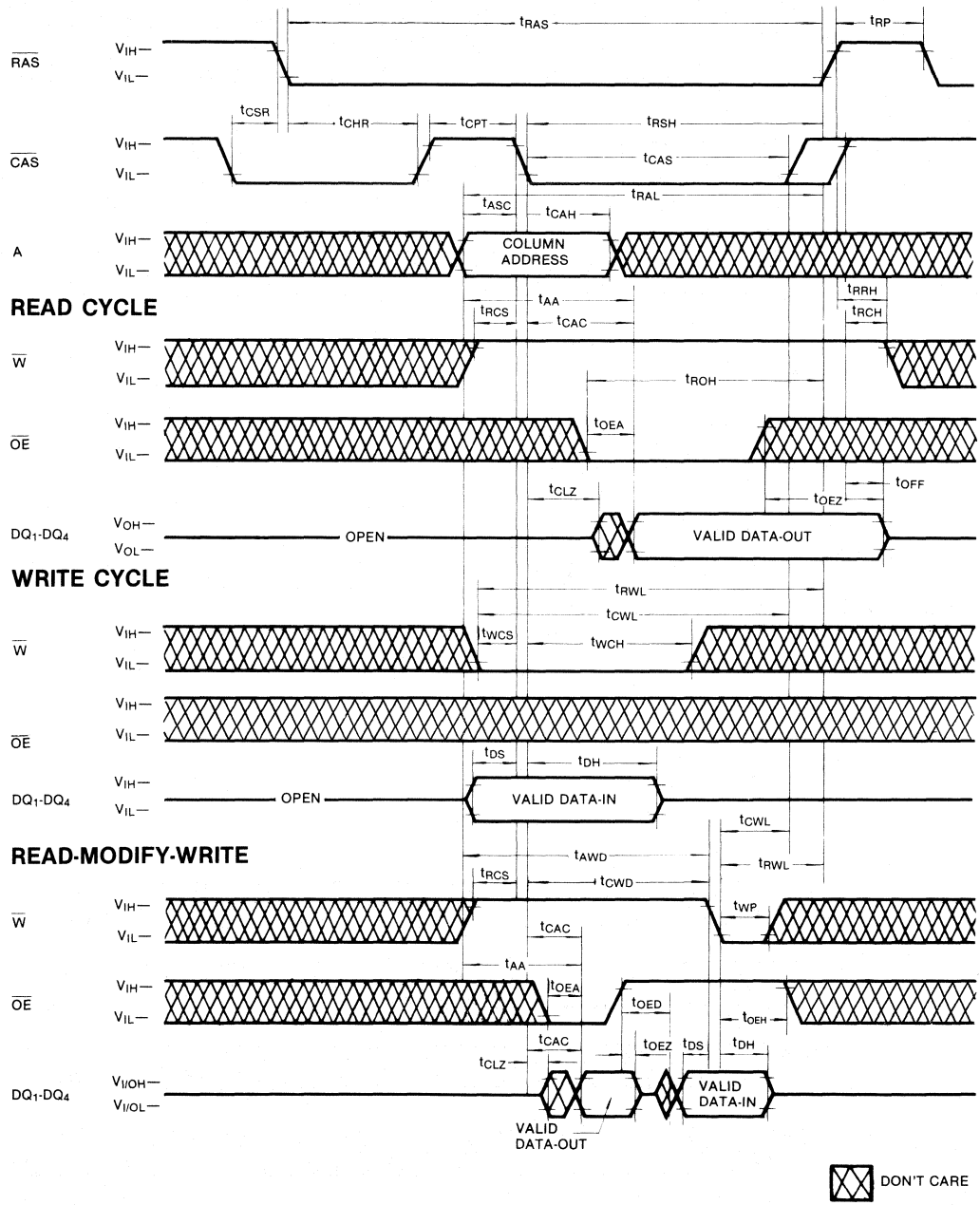


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM44C256C contains 1,048,576 memory locations organized as 262,144 four-bit words. Eighteen address bits are required to address a particular 4-bit word in the memory array. Since the KM44C256C has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the KM44C256C begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C256C cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (tRP) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by tRAS(min) and tCAS(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, tRP, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C256C begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before tRCD(max) and if the column address is valid before tRAD(max) then the access time to valid data is specified by tRAC(min). However, if $\overline{CAS}$ goes low after tRCD(max) or if the column address becomes valid after tRAD(max), access is specified by tCAC or tAA. In order to achieve the minimum access time, tRAC(min), it is necessary to meet both tRCD(max) and tRAD(max).

The KM44C256C has common data I/O pins. For this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by tOEA and tOEZ.

Write

The KM44C256C can perform early write, and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in he Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. This output enable input ($\overline{OE}$) must be low during the time defined by tOEA and tOEZ for data to appear at the outputs. If tCWD and tRWD are not met the output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM44C256C's DQ pins.

Data Output

The KM44C256C has a three state output buffer which are controlled by $\overline{CAS}$ and $\overline{OE}$. When either $\overline{CAS}$ or $\overline{OE}$ is high (VIH) the output are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by tCLZ after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after tCLZ and before the valid data appears at the output. The timing parameters tCAC, tRAC and tAA specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C256C operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (tCWD or tRWD are not met)

DEVICE OPERATION (Continued)

Refresh

The data in the KM44C256C is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 8 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A0-A8).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C256C has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (tCSR) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C256C hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C256C by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A0 through A8 are supplied by the on-chip refresh counter.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM44C256C could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C256C inputs act like unterminated transmission lines resulting in significant positive and negative overshoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C256C input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

DEVICE OPERATION (Continued)

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the VCC to VSS voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM44C256C using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C256C and they supply much of the current used by the KM44C256C during cycling.

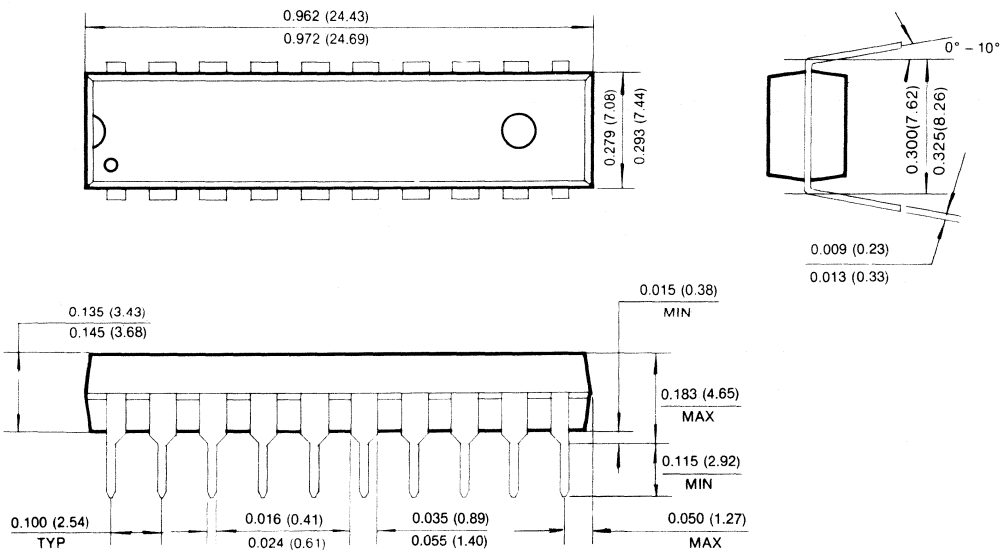
In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

2

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

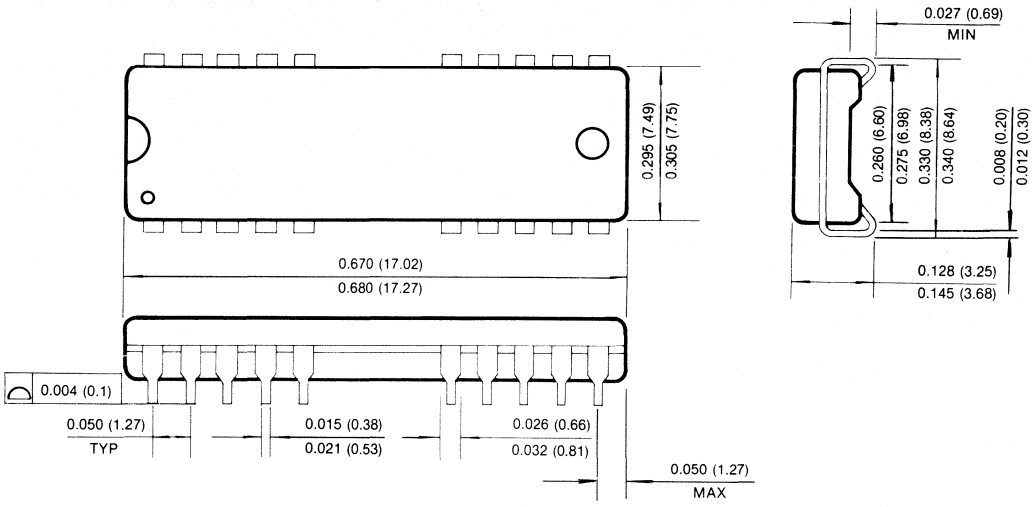
Units: Inches (Millimeters)



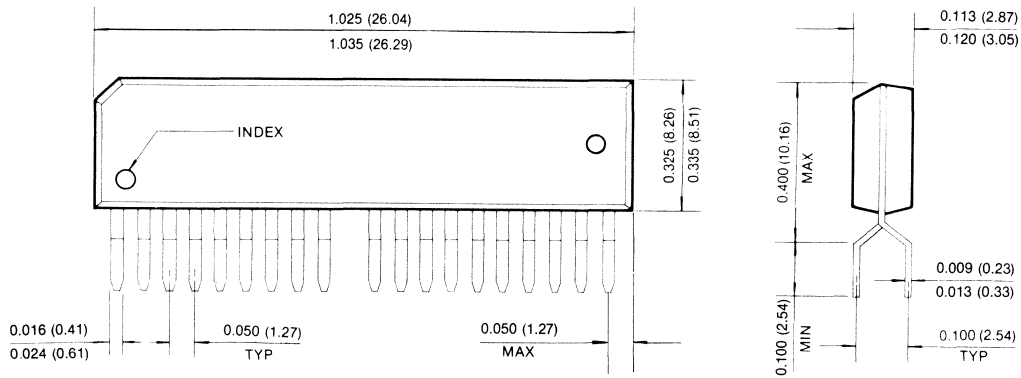
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



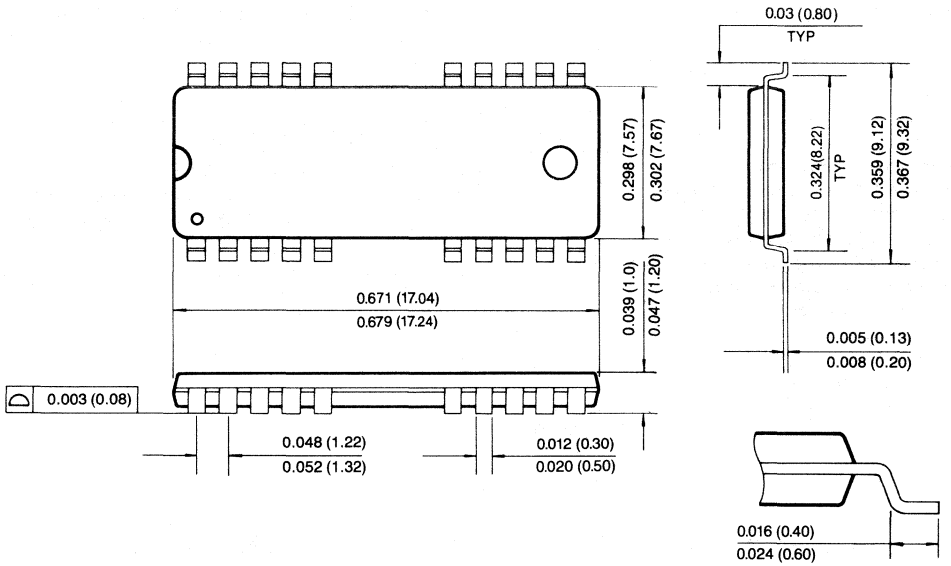
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



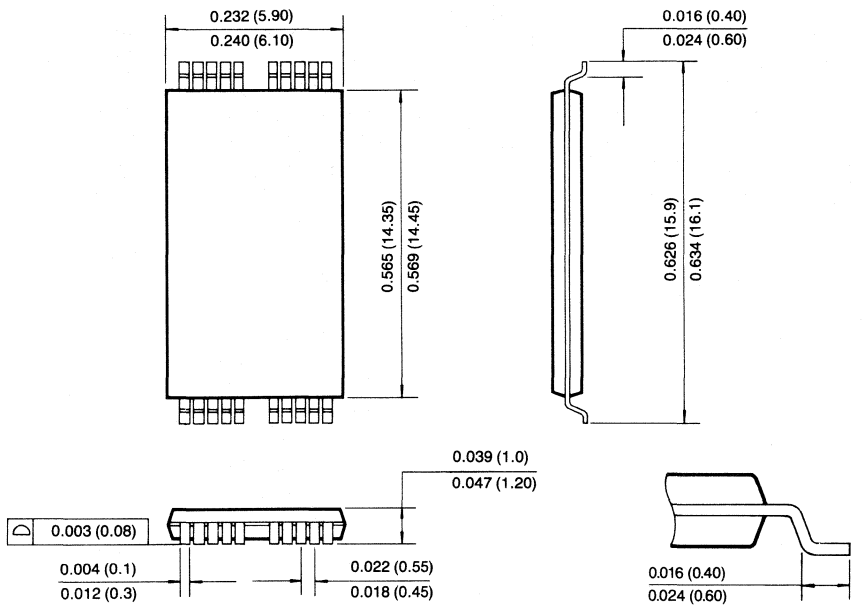
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (I) (Forward and Reverse Type)



256Kx4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C256CL-6	60ns	15ns	110ns
KM44C256CL-7	70ns	20ns	130ns
KM44C256CL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or Output Enable Controlled Write**
- **Single +5V ± 10% power supply**
- **Low power dissipation**
  - **I_{CC5}: 200μA**
  - **I_{CC7}: 200μA (Battery Backup Mode)**
- **512 cycle/64ms refresh**
- JEDEC standard pinout
- **Available in Plastic DIP, SOJ, ZIP, TSOP (I), TSOP (II) packages.**

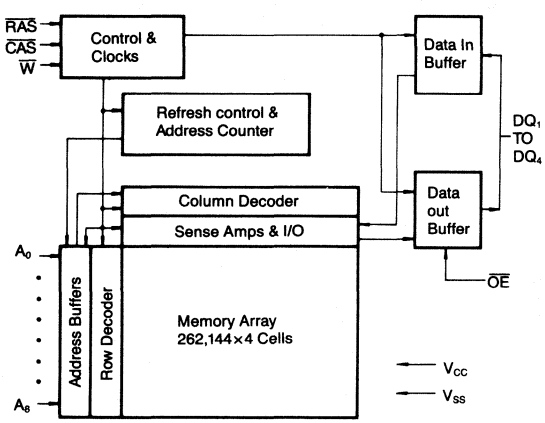
GENERAL DESCRIPTION

The Samsung KM44C256CL is a CMOS high speed 262,144 x 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance microprocessor computers.

The KM44C256CL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44C256CL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

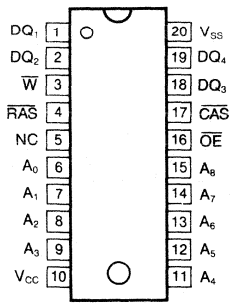


ORDERING INFORMATION

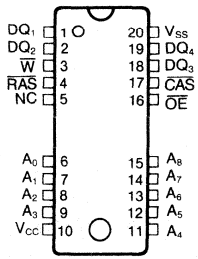
Part No.	Access Time	Package
KM44C256CLP-6	60ns	300 mil. 20DIP
KM44C256CLP-7	70ns	
KM44C256CLP-8	80ns	
KM44C256CLJ-6	60ns	300 mil. 20SOJ
KM44C256CLJ-7	70ns	
KM44C256CLJ-8	80ns	
KM44C256CLZ-6	60ns	400 mil. 20ZIP
KM44C256CLZ-7	70ns	
KM44C256CLZ-8	80ns	
KM44C256CLV-6	60ns	20 TOSP (I) (Forward)
KM44C256CLV-7	70ns	
KM44C256CLV-8	80ns	
KM44C256CLVR-6	60ns	20 TOSP (I) (Reverse)
KM44C256CLVR-7	70ns	
KM44C256CLVR-8	80ns	
KM44C256CLT-6	60ns	20 TOSP (II) (Forward)
KM44C256CLT-7	70ns	
KM44C256CLT-8	80ns	
KM44C256CLTR-6	60ns	20 TOSP (II) (Reverse)
KM44C256CLTR-7	70ns	
KM44C256CLTR-8	80ns	

PIN CONFIGURATION (Top Views)

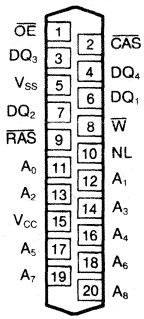
• KM44C256CLP



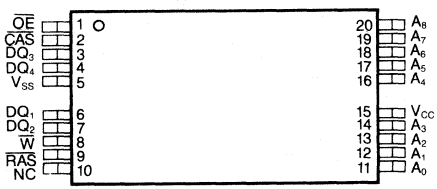
• KM44C256CLJ



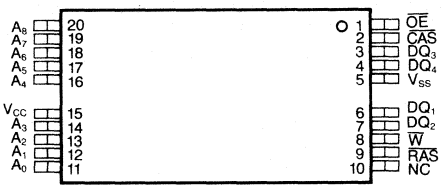
• KM44C256CLZ



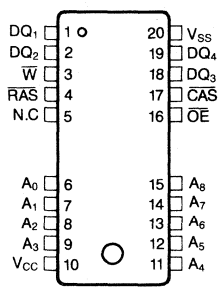
• KM44C256CLV



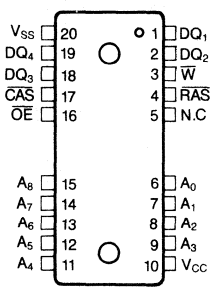
• KM44C256CLVR



• KM44C256CLT



• KM44C256CLTR



Pin Names	Pin Function
A_0-A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
DQ_1-DQ_4	Data In/Data Out
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection
NL	No Lead

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, and $\overline{CAS}$, Address Cycling @t_{RC} = min.)	KM44C256CL-6	I_{CC1}	—	70	mA
	KM44C256CL-7		—	65	mA
	KM44C256CL-8		—	60	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM44C256CL-6	I_{CC3}	—	70	mA
	KM44C256CL-7		—	65	mA
	KM44C256CL-8		—	60	mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC} = min.)	KM44C256CL-6	I_{CC4}	—	55	mA
	KM44C256CL-7		—	50	mA
	KM44C256CL-8		—	45	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC}-0.2V)		I_{CC5}	—	200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC} = min.)	KM44C256CL-6	I_{CC6}	—	70	mA
	KM44C256CL-7		—	65	mA
	KM44C256CL-8		—	60	mA
Battery Back Up Current Average Power Supply Current, Battery back up Mode ($\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{W}$ = V_{CC} − 0.2V or 0.2V, $A_0 \sim A_8$ = V_{CC} − 0.2V or 0.2V, D_{IN} = V_{CC} − 0.2V, 0.2V or OPEN: t_{RC} = 125μS, t_{RAS} = t_{RAS} min. ~ 1μS)	KM44C256CL-6 KM44C256CL-7 KM44C256CL-8	I_{CC7}	—	200	μA
Input Leakage Current (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0 ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3} Address can be changed maximum two times while $\overline{RAS}$ = V_{IL}, I_{CC4}, Address can be changed maximum once while $\overline{CAS}$ = V_{IH}.

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance [A_0-A_8]	C_{IN1}	—	6	pF
Input Capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	—	7	pF
Output Capacitance [DQ_1-DQ_4]	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ± 10%, See notes 1, 2)

Parameter	Symbol	KM44C256CL-6		KM44C256CL-7		KM44C256CL-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		175		195		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3, 4, 11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3, 4, 5
Access time from column address	t_{AA}		30		35		40	ns	3, 10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	

AC CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$, See notes 1, 2)

Parameter	Symbol	KM44C256CL-6		KM44C256CL-7		KM44C256CL-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	50		55		60		ns	6
Write command pulse width	t_{WP}	15		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (512 cycles)	t_{REF}		64		64		64	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		45		45		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		95		105		ns	8
Column address to $\overline{W}$ dealy time	t_{AWD}	55		60		65		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	15		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		35		40	ns	3
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	80		85		90		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	15		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	15		20		20		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

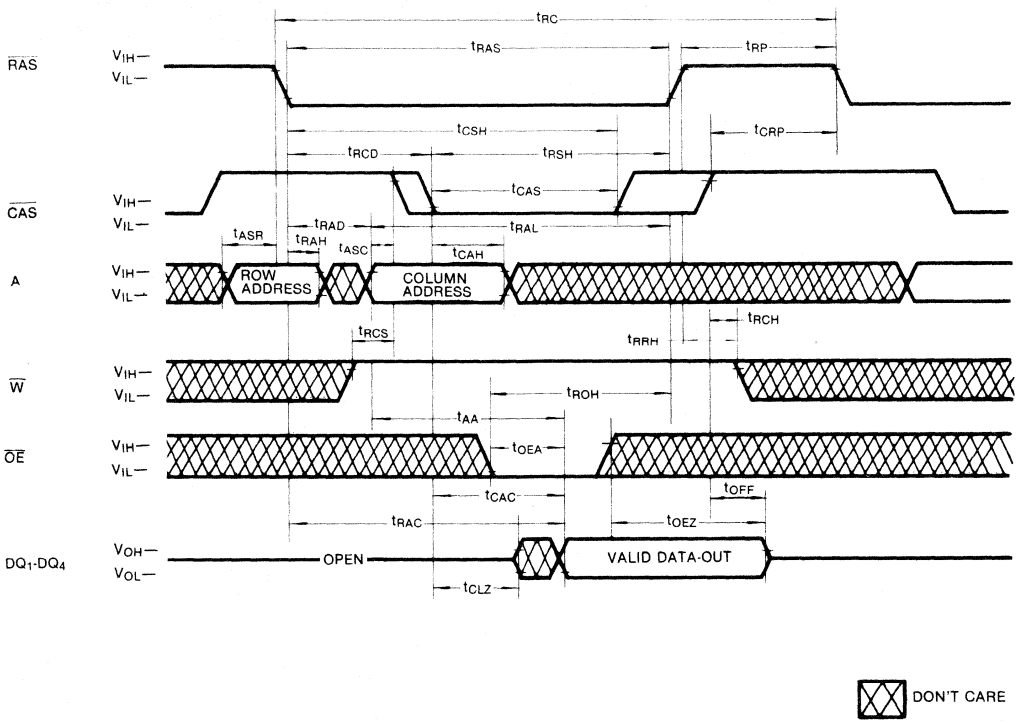
NOTES (Continued)

5. Assumes that $t_{RCD} \geq t_{RCD}(max)$.
6. t_{WCR}, t_{DHR} are referenced to $t_{RAD}(max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}(min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(min)$, $t_{RWD} \geq t_{RWD}(min)$ and $t_{AWD} \geq t_{AWD}(min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RAC}(max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled by t_{AA}.

2

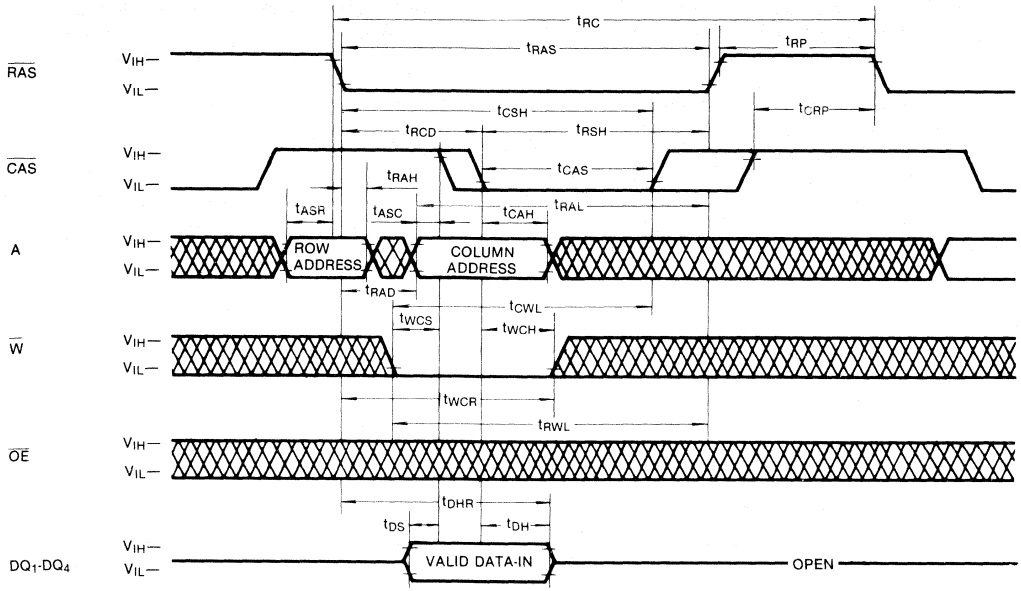
TIMING DIAGRAMS

READ CYCLE

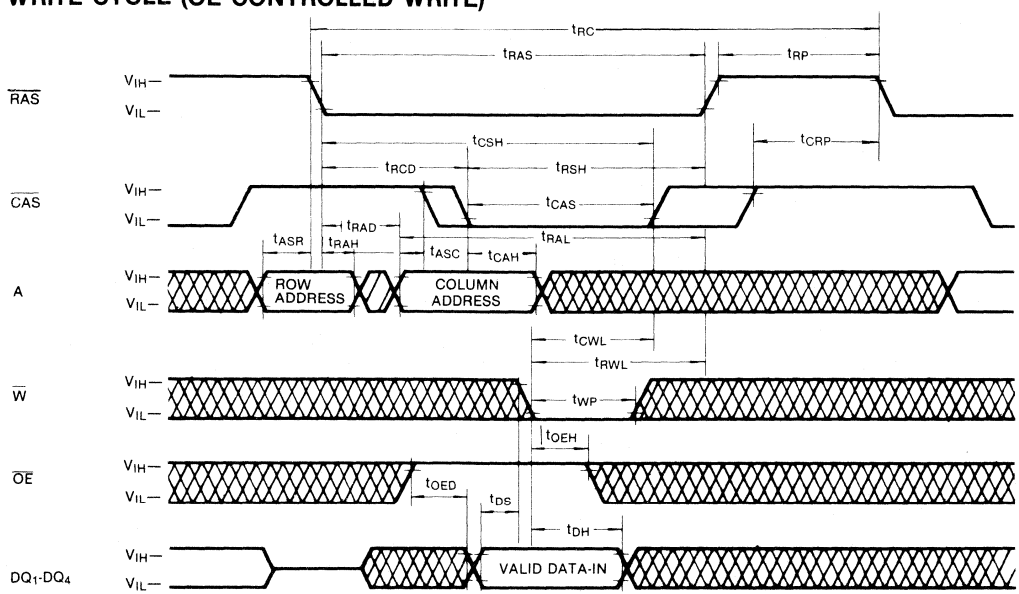


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

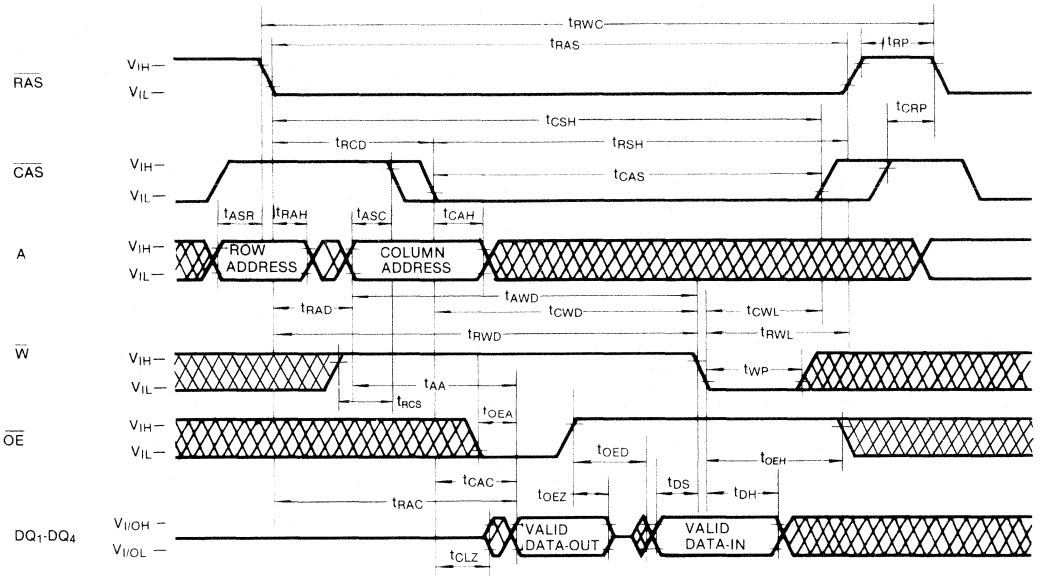


WRITE CYCLE (OE CONTROLLED WRITE)

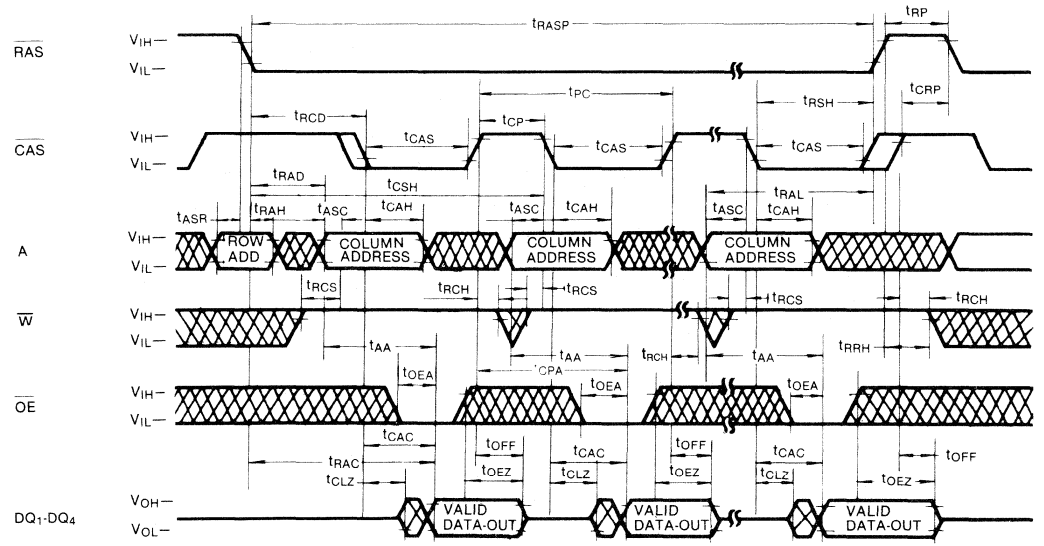


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



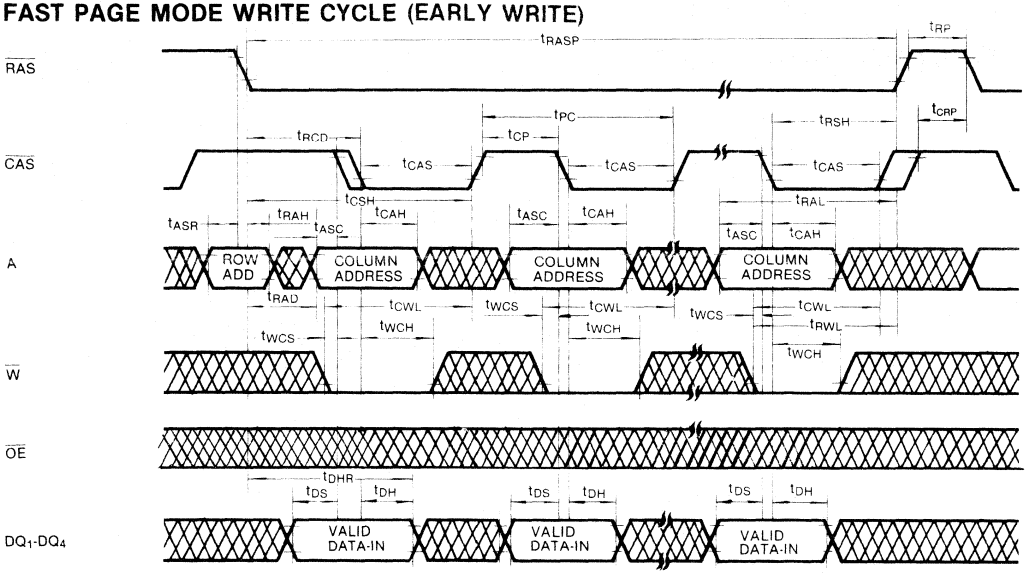
FAST PAGE MODE READ CYCLE



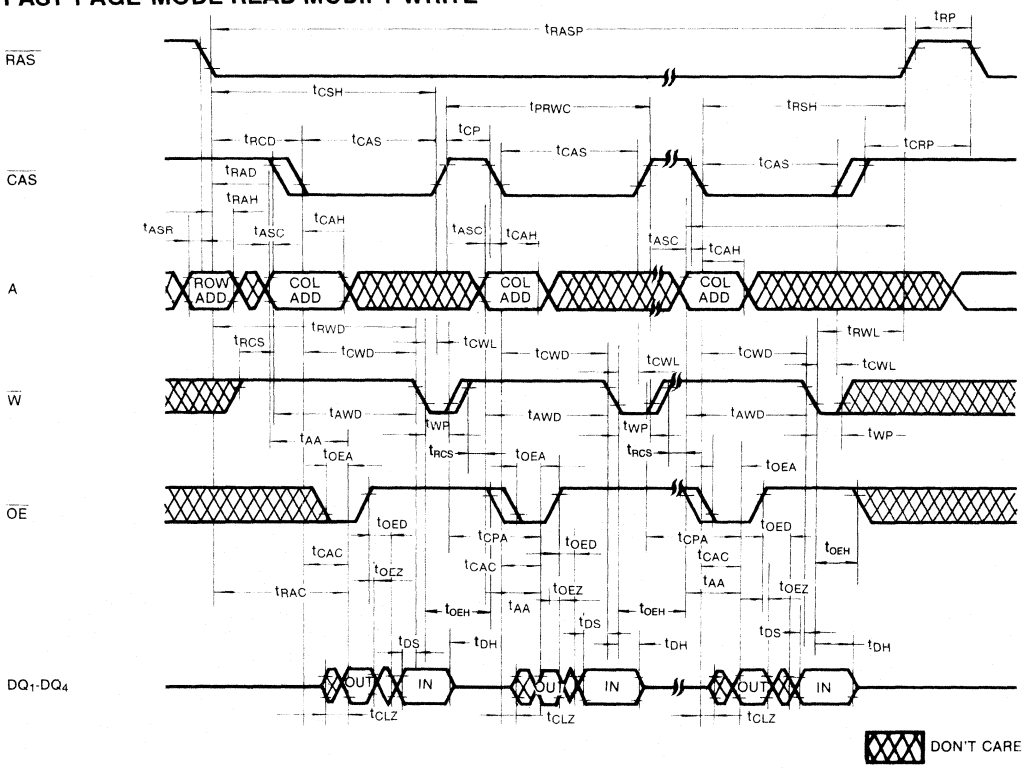
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



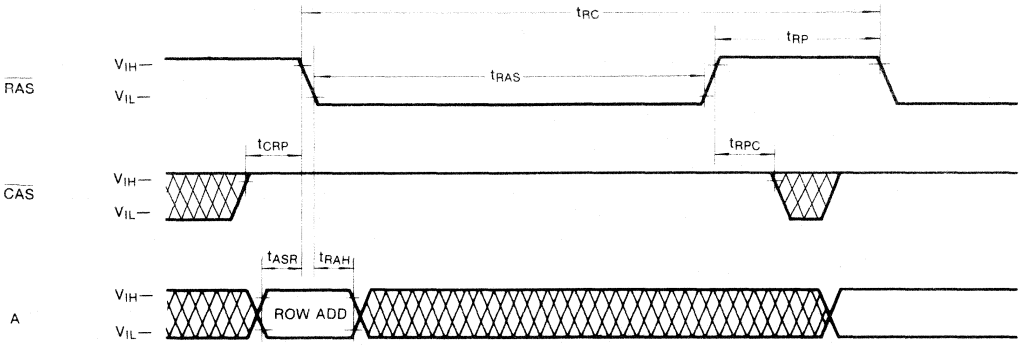
FAST PAGE MODE READ-MODIFY-WRITE



TIMING DIAGRAMS (Continued)

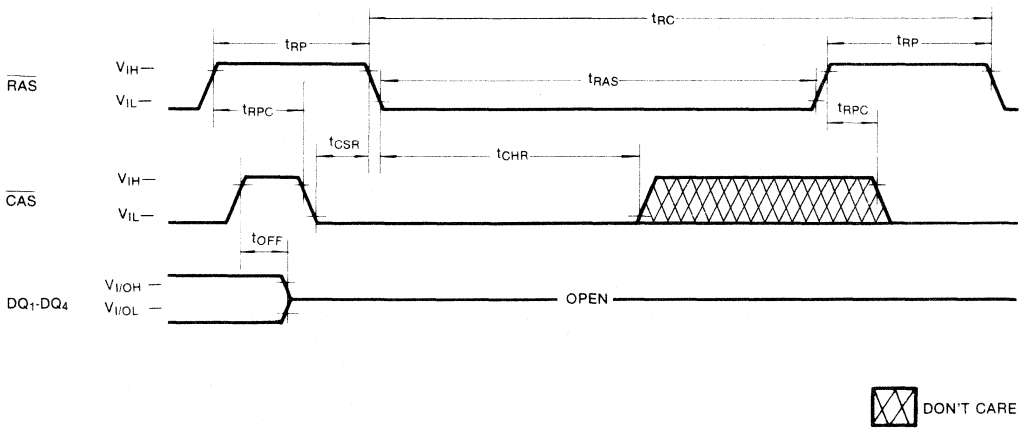
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



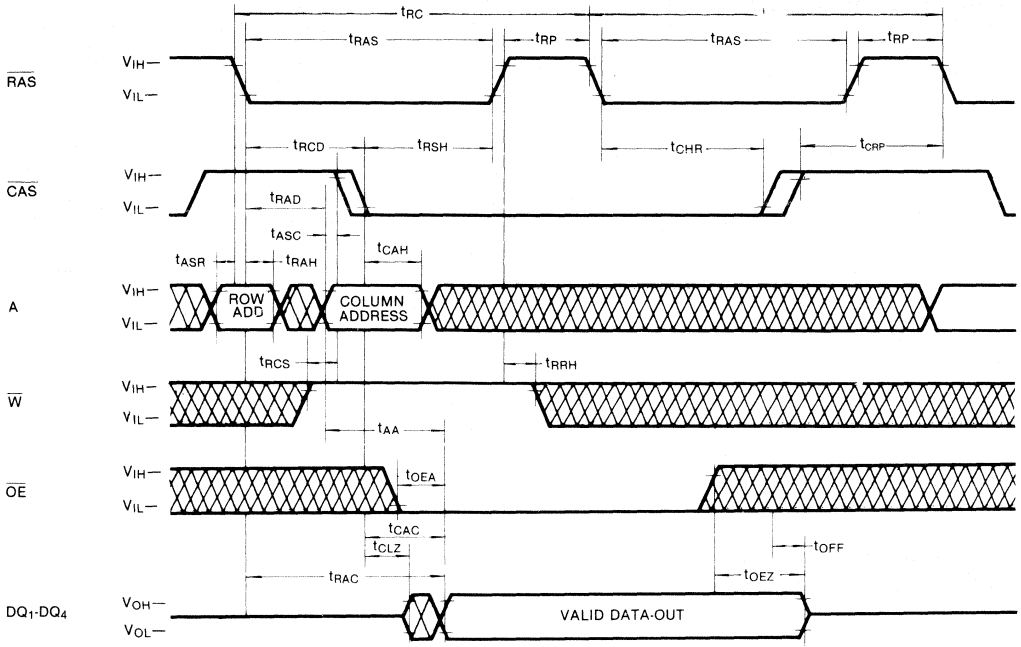
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$, A = Don't care

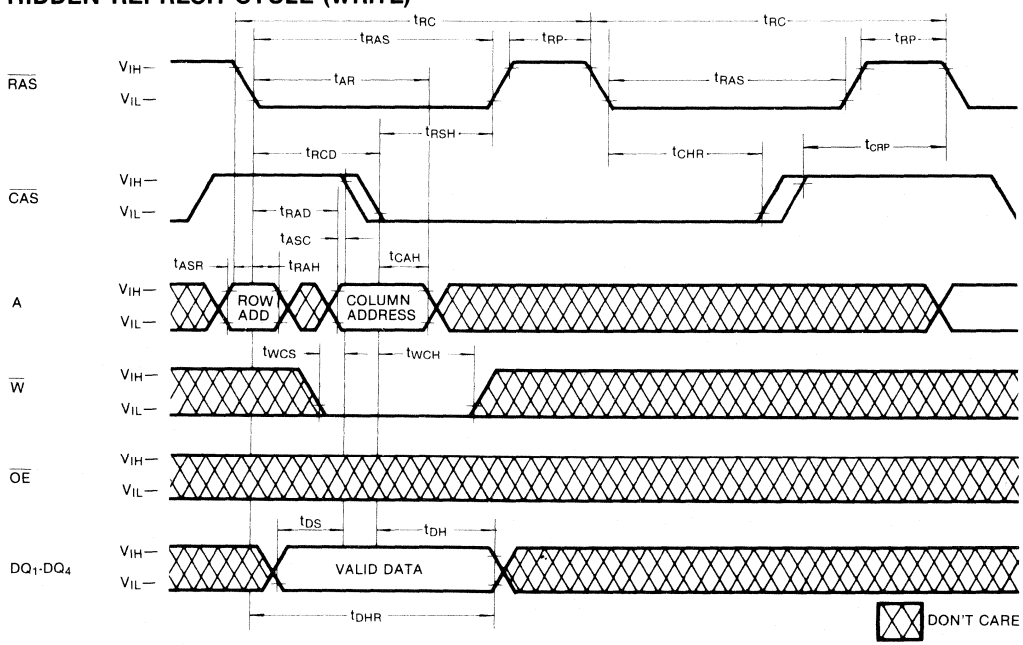


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

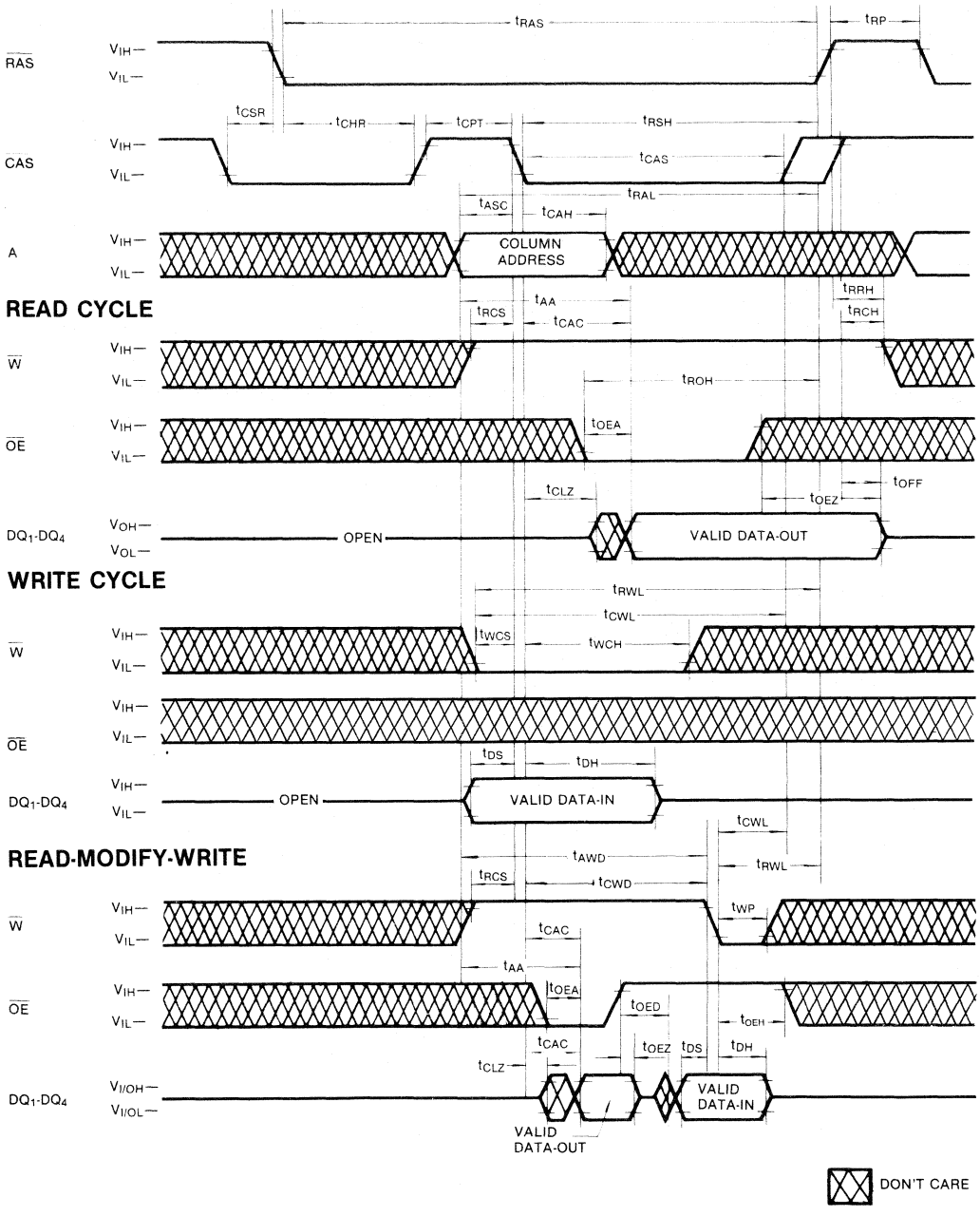


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM44C256CL contains 1,048,576 memory locations organized as 262,144 four-bit words. Eighteen address bits are required to address a particular 4-bit word in the memory array. Since the KM44C256CL has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the KM44C256CL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C256CL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (tRP) requirement.

RAS and CAS Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by tRAS(min) and tCAS(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, tRP, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C256CL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before tRCD(max) and if the column address is valid before tRAD(max) then the access time to valid data is specified by tRAC(min). However, if $\overline{CAS}$ goes low after tRCD(max) or if the column address becomes valid after tRAD(max), access is specified by tCAC or tAA. In order to achieve the minimum access time, tRAC(min), it is necessary to meet both tRCD(max) and tRAD(max).

The KM44C256CL has common data I/O pins. For this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by tOEA and tOEZ.

Write

The KM44C256CL can perform early write, and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in he Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. This output enable input ($\overline{OE}$) must be low during the time defined by tOEA and tOEZ for data to appear at the outputs. If tCWD and tRWD are not met the output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM44C256CL's DQ pins.

Data Output

The KM44C256CL has a three state output buffer which are controlled by $\overline{CAS}$ and $\overline{OE}$. When either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}) the output are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by tCLZ after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after tCLZ and before the valid data appears at the output. The timing parameters tCAC, tRAC and tAA specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C256C operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (tCWD or tRWD are not met)

DEVICE OPERATION (Continued)

Refresh

The data in the KM44C256CL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 64 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A0-A8).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C256CL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (tCSR) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. **The KM44C256CL hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.**

Other Refresh Methods: **It is also possible to refresh the KM44C256CL by using read, write or read-modify-write** cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A0 through A8 are supplied by the on-chip refresh counter.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the**KM44C256CL** could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the **KM44C256CL inputs act like unterminated transmission** lines resulting in significant positive and negative overshoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input **line placed close to the KM44C256CL input pin. The optimum** value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

DEVICE OPERATION (Continued)

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

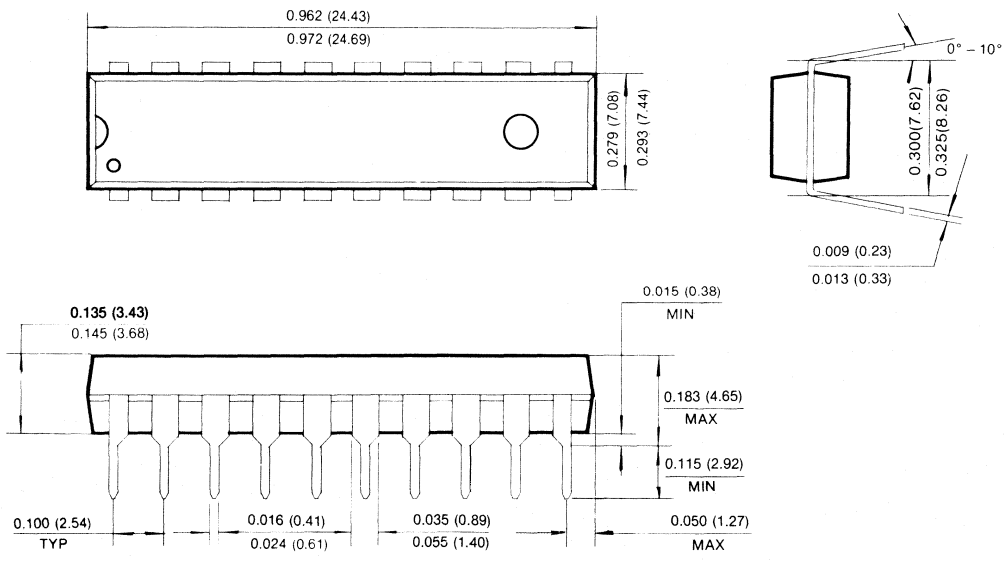
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground **pins of each KM44C256CL using the shortest possible** traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated **by the KM44C256CL and they supply much of the current used by the KM44C256CL during cycling.**

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

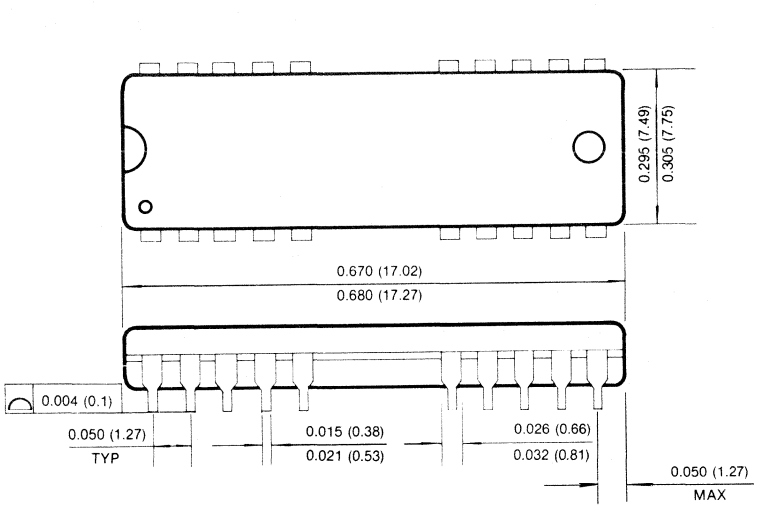
Units: Inches (Millimeters)



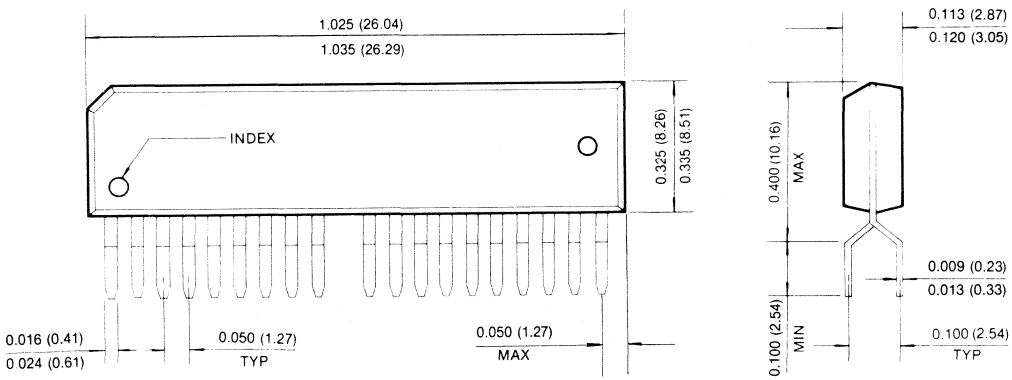
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



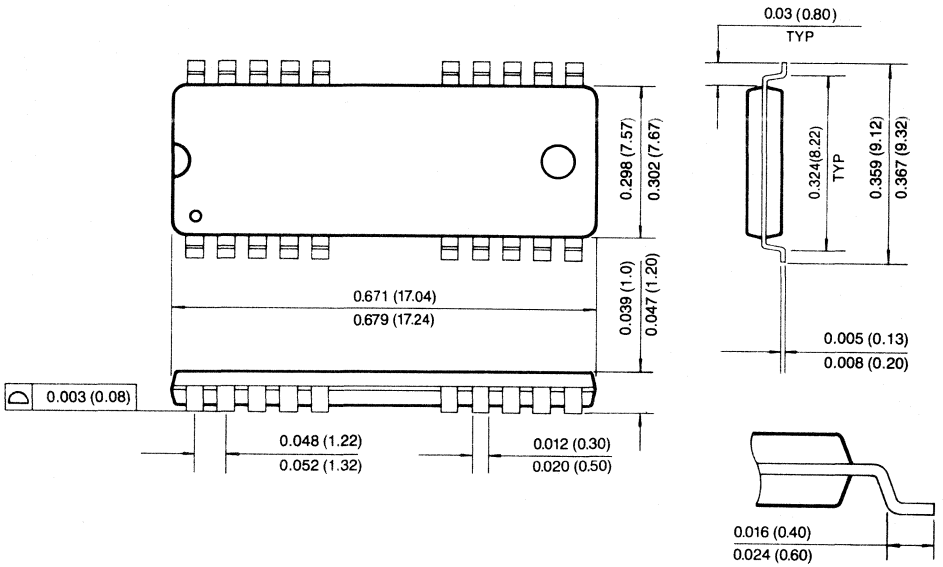
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



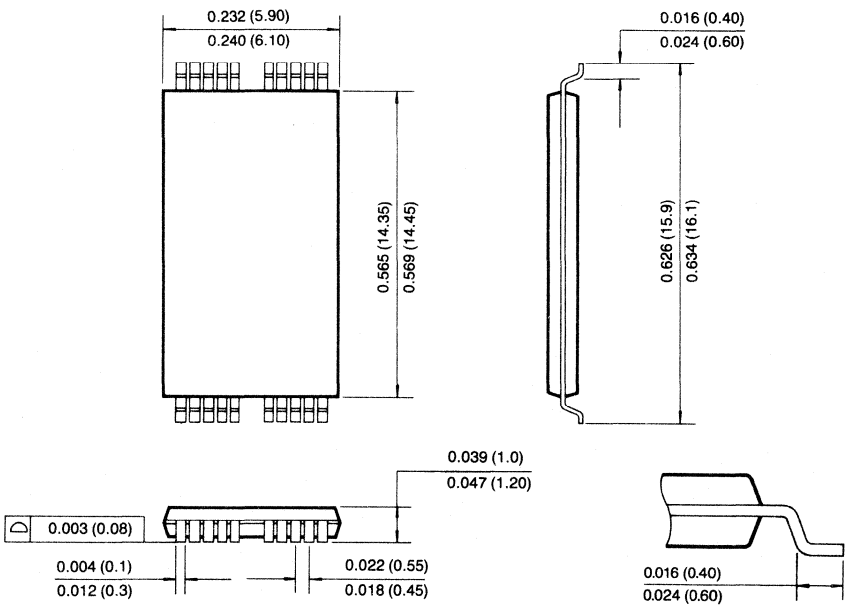
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (I) (Forward and Reverse Type)



256K×4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C256CSL-6	60ns	15ns	110ns
KM44C256CSL-7	70ns	20ns	130ns
KM44C256CSL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or Output Enable Controlled Write**
- **Single +5V ± 10% power supply**
- **Low power dissipation**
  - **I_{CC5}: 100μA**
  - **I_{CC7}: 100μA**
- **512 cycle/128ms refresh**
- JEDEC standard pinout
- **Available in Plastic DIP, SOJ, ZIP, TSOP (I), TSOP (II) packages.**

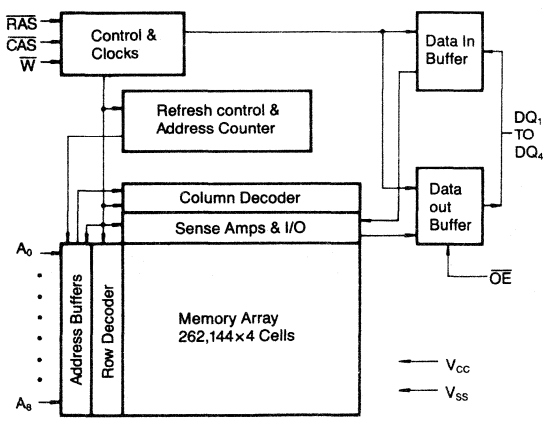
GENERAL DESCRIPTION

The Samsung KM44C256CSL is a CMOS high speed 262,144 × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance microprocessor computers.

The KM44C256CSL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44C256CSL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

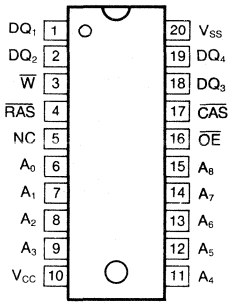


ORDERING INFORMATION

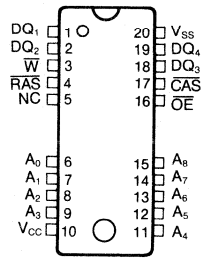
Part No.	Access Time	Package
KM44C256CSLP-6	60ns	300 mil. 20DIP
KM44C256CSLP-7	70ns	
KM44C256CSLP-8	80ns	
KM44C256CSLJ-6	60ns	300 mil. 20SOJ
KM44C256CSLJ-7	70ns	
KM44C256CSLJ-8	80ns	
KM44C256CSLZ-6	60ns	400 mil. 20ZIP
KM44C256CSLZ-7	70ns	
KM44C256CSLZ-8	80ns	
KM44C256CSLV-6	60ns	20 TOSP (I) (Forward)
KM44C256CSLV-7	70ns	
KM44C256CSLV-8	80ns	
KM44C256CSLVR-6	60ns	20 TOSP (I) (Reverse)
KM44C256CSLVR-7	70ns	
KM44C256CSLVR-8	80ns	
KM44C256CSLT-6	60ns	20 TOSP (II) (Forward)
KM44C256CSLT-7	70ns	
KM44C256CSLT-8	80ns	
KM44C256CSLTR-6	60ns	20 TOSP (II) (Reverse)
KM44C256CSLTR-7	70ns	
KM44C256CSLTR-8	80ns	

PIN CONFIGURATION (Top Views)

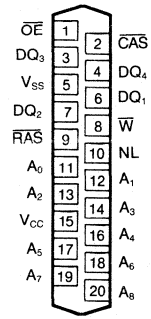
• KM44C256CSLP



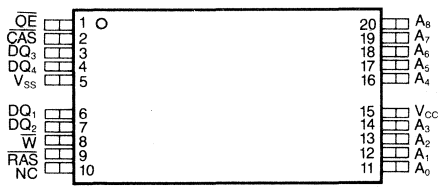
• KM44C256CSLJ



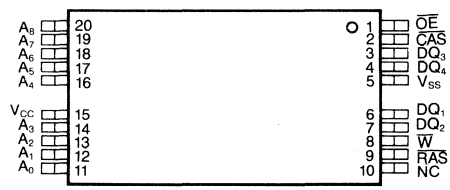
• KM44C256CSLZ



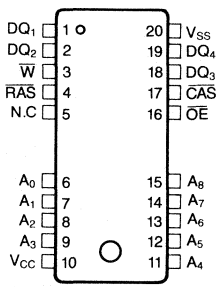
• KM44C256 CSLV



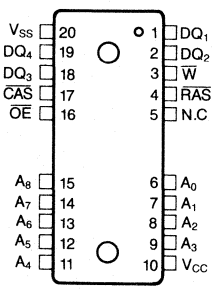
• KM44C256 CSLVR



• KM44C256 CSLT



• KM44C256 CSLTR



Pin Names	Pin Function
A_0-A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
DQ_1-DQ_4	Data In/Data Out
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection
NL	No Lead

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, and $\overline{CAS}$, Address Cycling @t_{RC} = min.)	KM44C256CSL-6	I_{CC1}	—	70	mA
	KM44C256CSL-7		—	65	mA
	KM44C256CSL-8		—	60	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM44C256CSL-6	I_{CC3}	—	70	mA
	KM44C256CSL-7		—	65	mA
	KM44C256CSL-8		—	60	mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC} = min.)	KM44C256CSL-6	I_{CC4}	—	55	mA
	KM44C256CSL-7		—	50	mA
	KM44C256CSL-8		—	45	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC}-0.2V)		I_{CC5}	—	100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC} = min.)	KM44C256CSL-6	I_{CC6}	—	70	mA
	KM44C256CSL-7		—	65	mA
	KM44C256CSL-8		—	60	mA
Battery Back Up Current Average Power Supply Current, Battery back up Mode ($\overline{CAS}$ = $\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V, $\overline{W}$ = V_{CC} − 0.2V or 0.2V, A_0 ~ A_8 = V_{CC} − 0.2V or 0.2V, D_{IN} = V_{CC} − 0.2V, 0.2V or OPEN: t_{RC} = 250μS, t_{RAS} = t_{RAS} min. ~ 1μS)	KM44C256CSL-6 KM44C256CSL-7 KM44C256CSL-8	I_{CC7}	—	100	μA
Input Leakage Current (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0 ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3} Address can be changed maximum two times while $\overline{RAS}$ = V_{IL}, I_{CC4}, Address can be changed maximum once while $\overline{CAS}$ = V_{IH}.

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance [A_0-A_8]	C_{IN1}	—	6	pF
Input Capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	—	7	pF
Output Capacitance [DQ_1-DQ_4]	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ± 10%, See notes 1, 2)

Parameter	Symbol	KM44C256CSL-6		KM44C256CSL-7		KM44C256CSL-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		175		195		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3, 4, 11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3, 4, 5
Access time from column address	t_{AA}		30		35		40	ns	3, 10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	

AC CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$, See notes 1, 2)

Parameter	Symbol	KM44C256CSL-6		KM44C256CSL-7		KM44C256CSL-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	50		55		60		ns	6
Write command pulse width	t_{WP}	15		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (512 cycles)	t_{REF}		128		128		128	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		45		45		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		95		105		ns	8
Column address to $\overline{W}$ dealy time	t_{AWD}	55		60		65		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	15		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		35		40	ns	3
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	80		85		90		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	15		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	15		20		20		ns	

NOTES

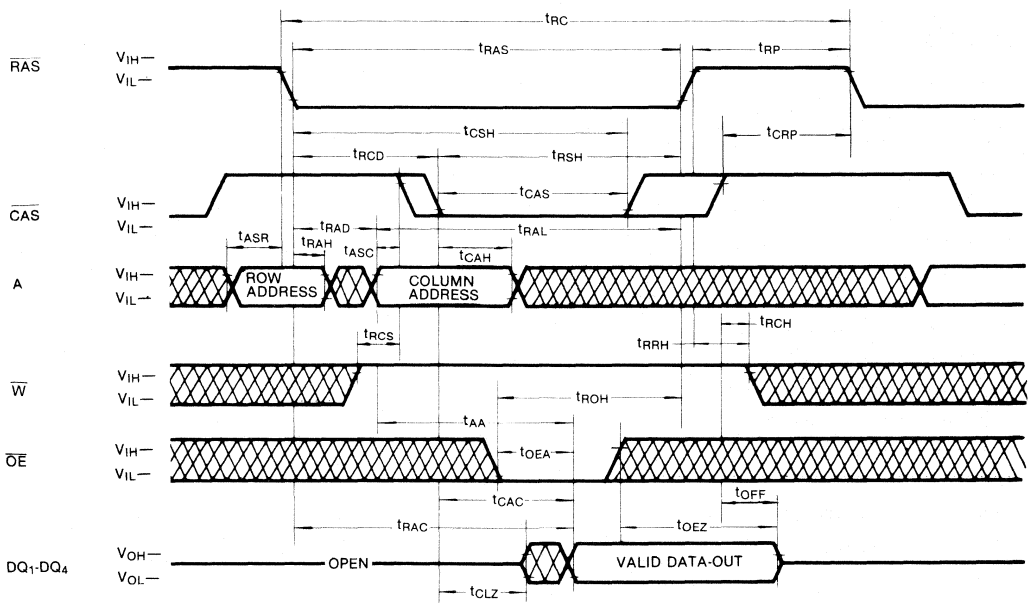
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

NOTES (Continued)

5. Assumes that $t_{RCD} \geq t_{RCD}(max)$.
6. t_{WCR}, t_{DHR} are referenced to $t_{RAD}(max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}(min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(min)$, $t_{RWD} \geq t_{RWD}(min)$ and $t_{AWD} \geq t_{AWD}(min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RAC}(max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled by t_{AA}.

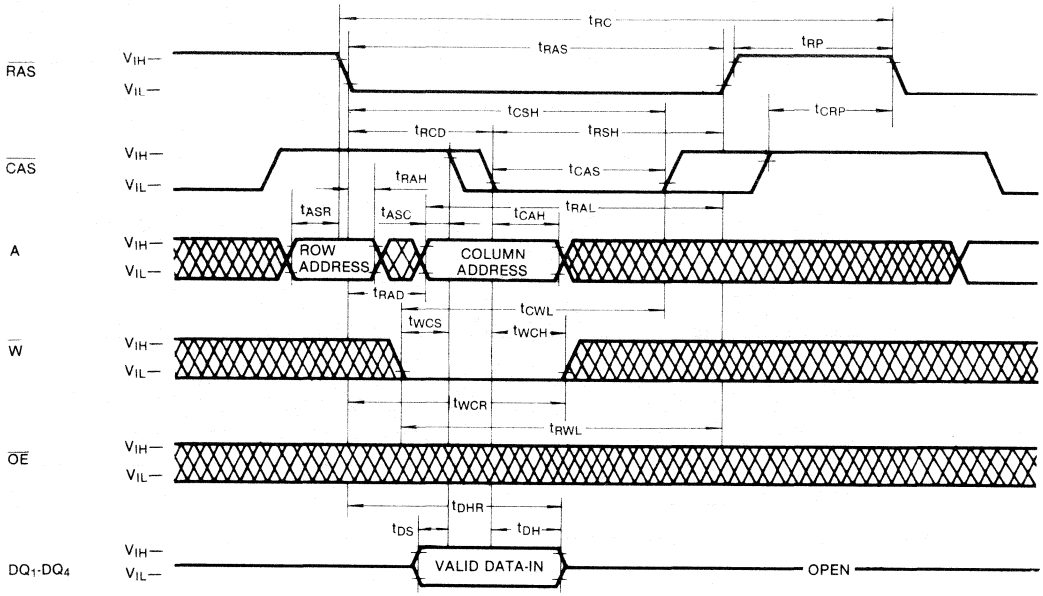
TIMING DIAGRAMS

READ CYCLE

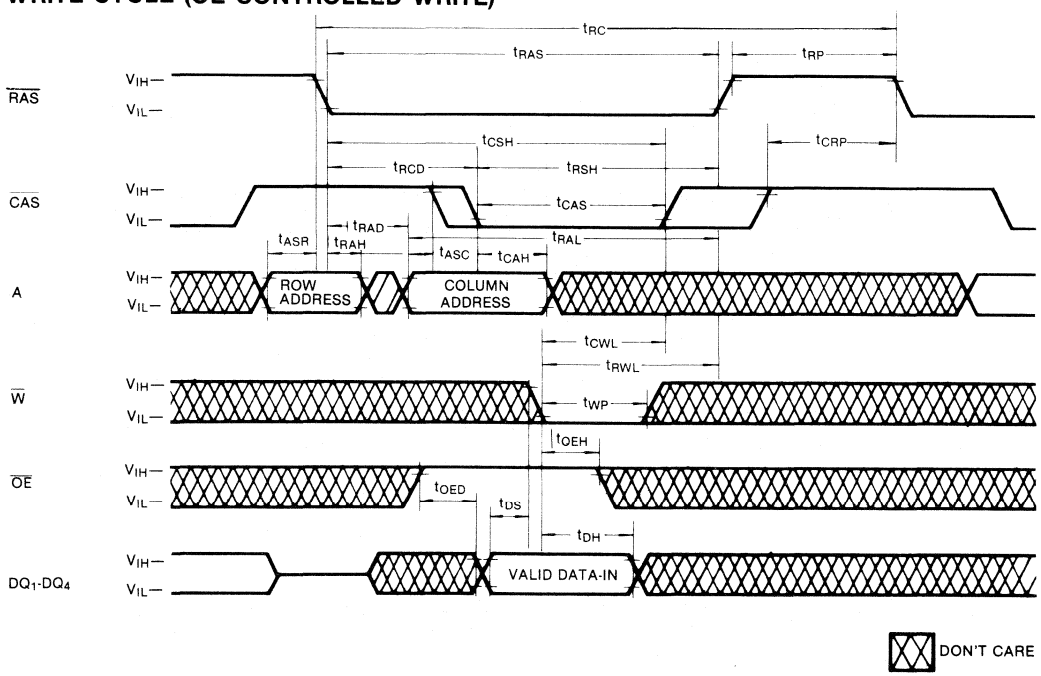


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

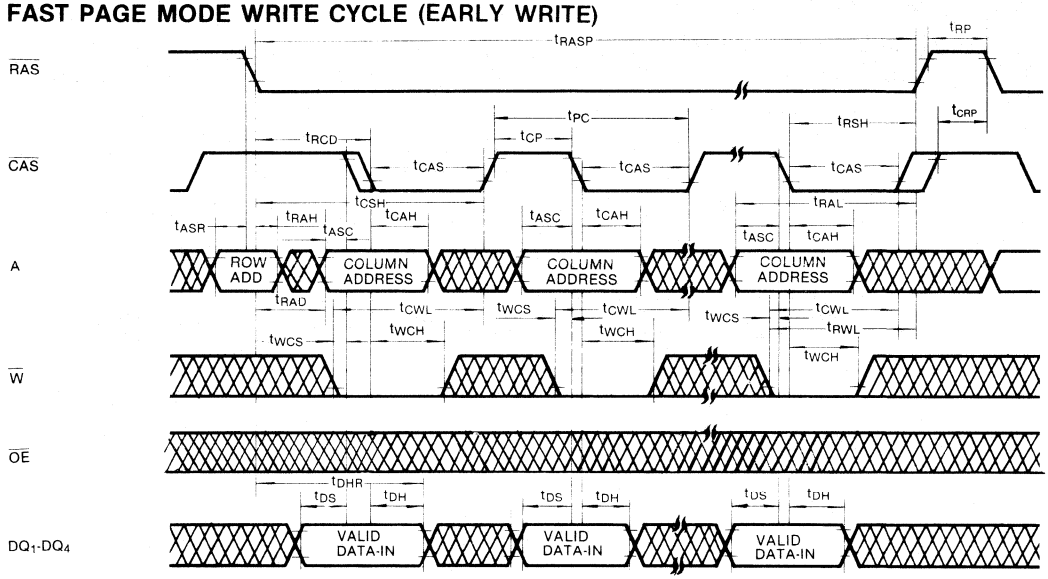


WRITE CYCLE (OE CONTROLLED WRITE)

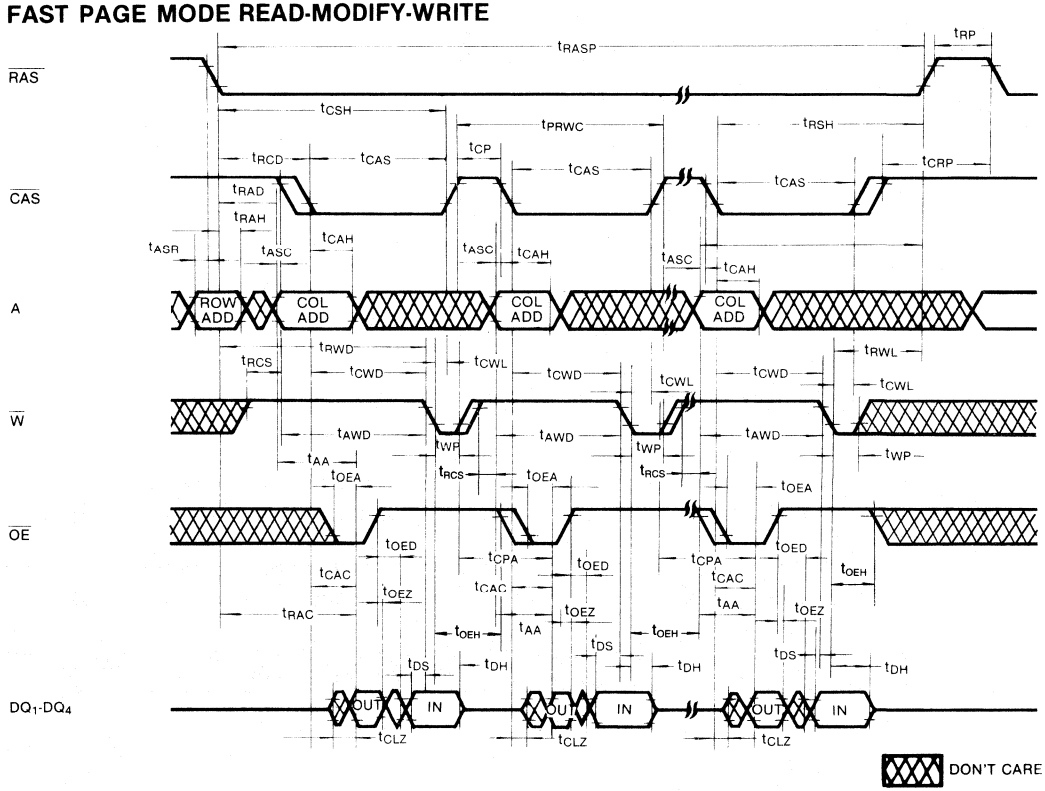


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

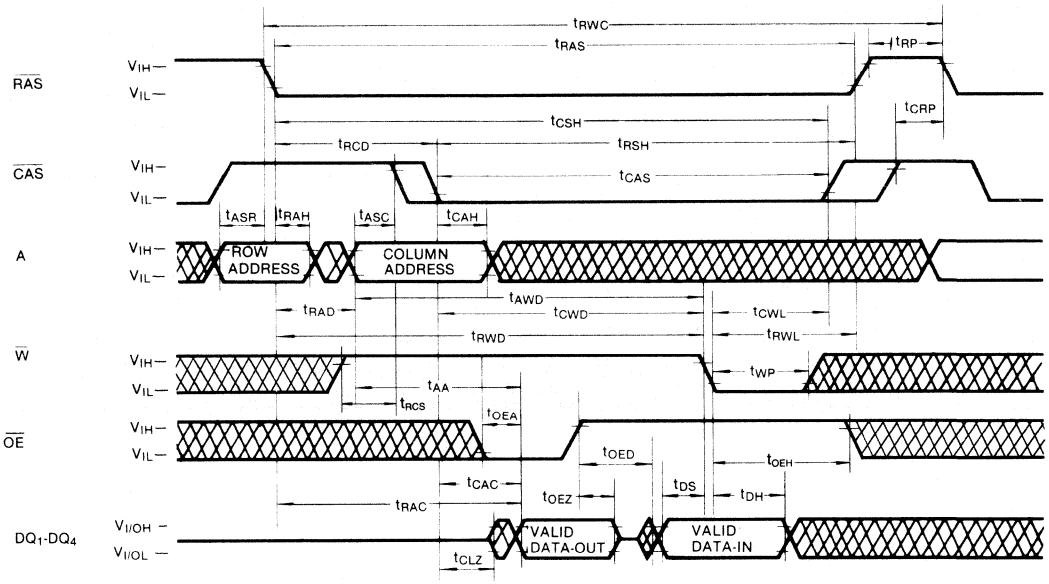


FAST PAGE MODE READ-MODIFY-WRITE

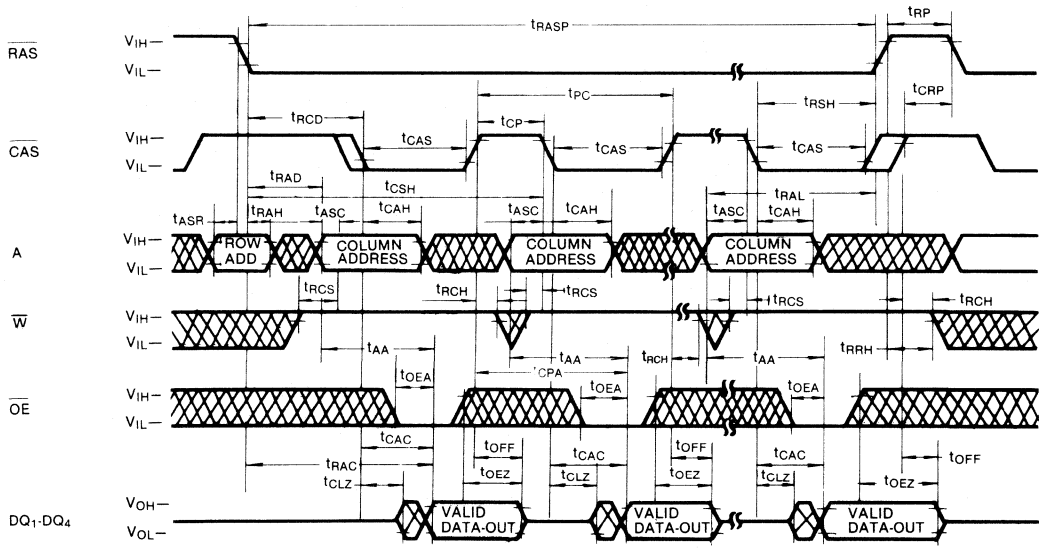


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE

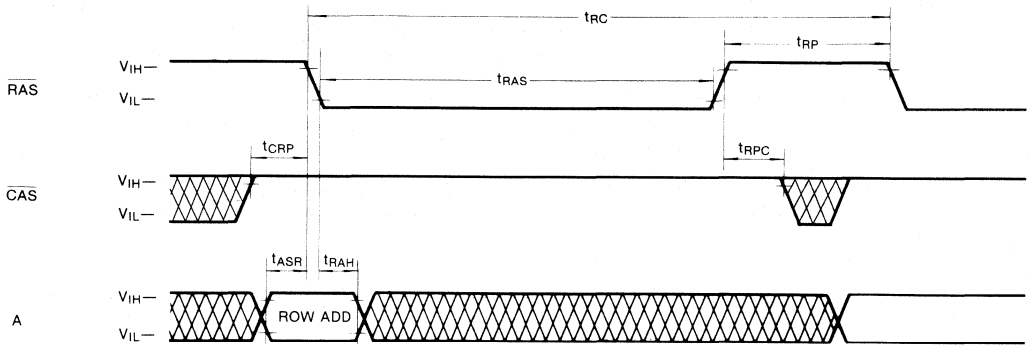


DON'T CARE

TIMING DIAGRAMS (Continued)

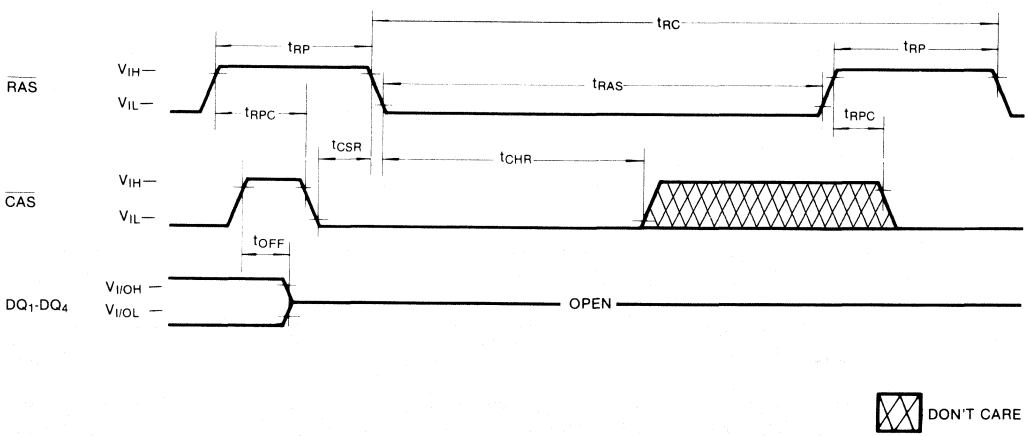
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



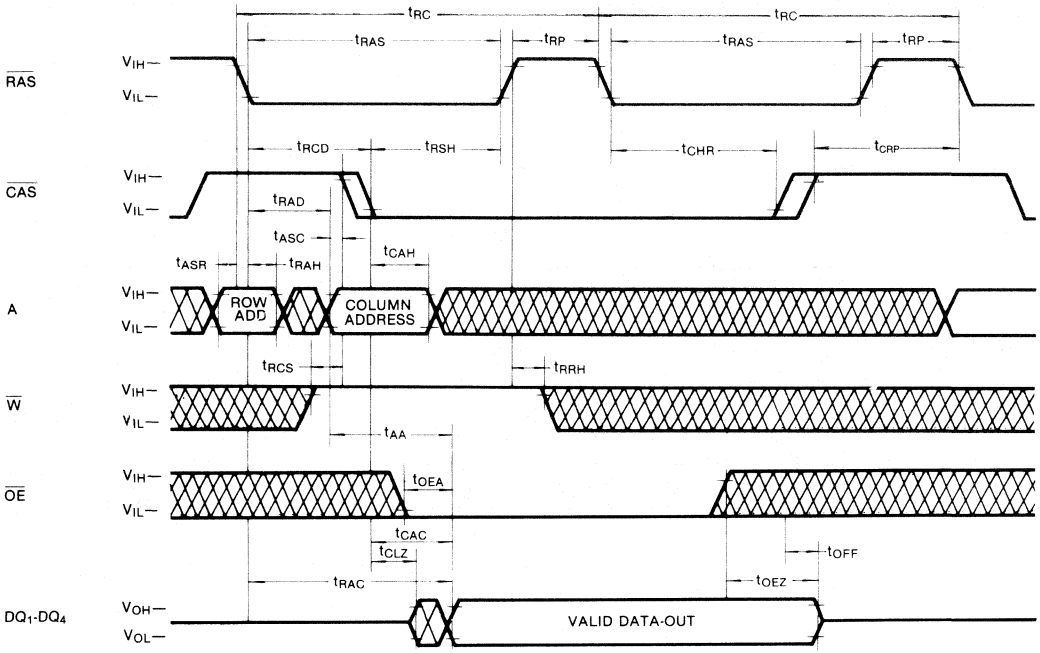
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$, A = Don't care

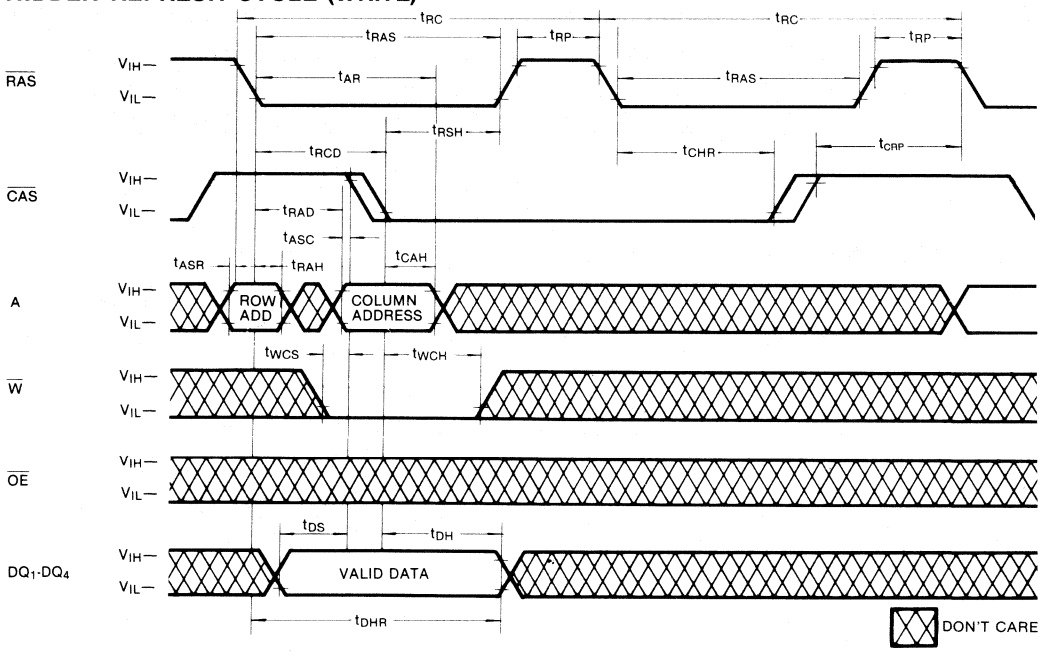


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

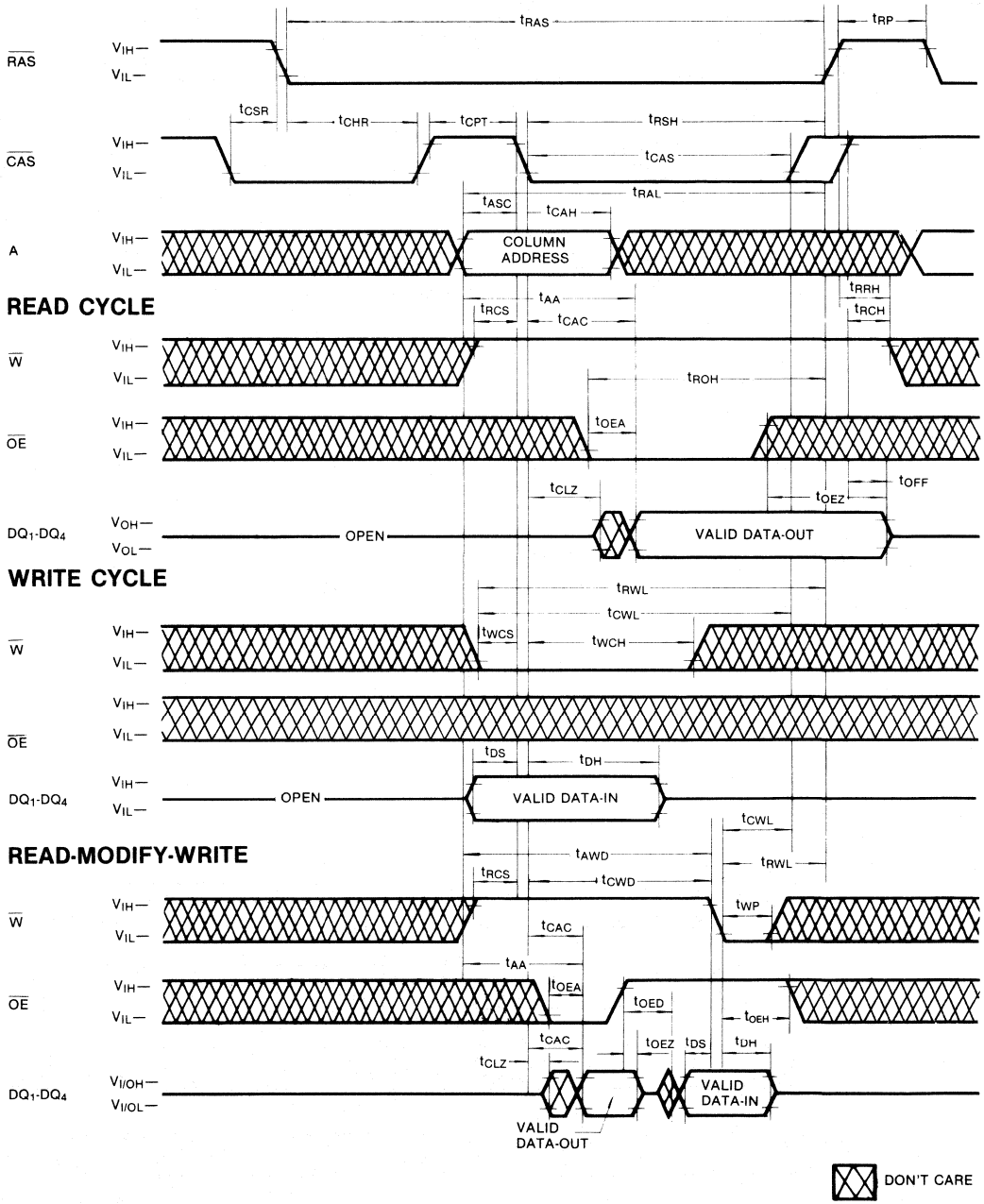


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM44C256CSL contains 1,048,576 memory locations organized as 262,144 four-bit words. Eighteen address bits are required to address a particular 4-bit word in the memory array. Since the KM44C256CSL has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the KM44C256CSL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C256CSL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (tRP) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by tRAS(min) and tCAS(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, tRP, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C256CSL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before tRCD(max) and if the column address is valid before tRAD(max) then the access time to valid data is specified by tRAC(min). However, if $\overline{CAS}$ goes low after tRCD(max) or if the column address becomes valid after tRAD(max), access is specified by tCAC or tAA. In order to achieve the minimum access time, tRAC(min), it is necessary to meet both tRCD(max) and tRAD(max).

The KM44C256CSL has common data I/O pins. For this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by tOEA and tOEZ.

Write

The KM44C256CSL can perform early write, and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in he Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. This output enable input ($\overline{OE}$) must be low during the time defined by tOEA and tOEZ for data to appear at the outputs. If tCWD and tRWD are not met the output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM44C256CSL's DQ pins.

Data Output

The KM44C256CSL has a three state output buffer which are controlled by $\overline{CAS}$ and $\overline{OE}$. When either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}) the output are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by tCLZ after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after tCLZ and before the valid data appears at the output. The timing parameters tCAC, tRAC and tAA specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C256CSL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (tCWD or tRWD are not met)

DEVICE OPERATION (Continued)

Refresh

The data in the KM44C256CSL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 128 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A0-A8).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C256CSL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (tCSR) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C256CSL hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C256CSL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A0 through A8 are supplied by the on-chip refresh counter.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-up

If $\overline{RAS}=V_{SS}$ during power-up, the KM44C256CSL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C256CSL inputs act like unterminated transmission lines resulting in significant positive and negative overshoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C256CSL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

DEVICE OPERATION (Continued)

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground **pins of each KM44C256CSL using the shortest possible** traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated **by the KM44C256CSL and they supply much of the current used by the KM44C256CSL during cycling.**

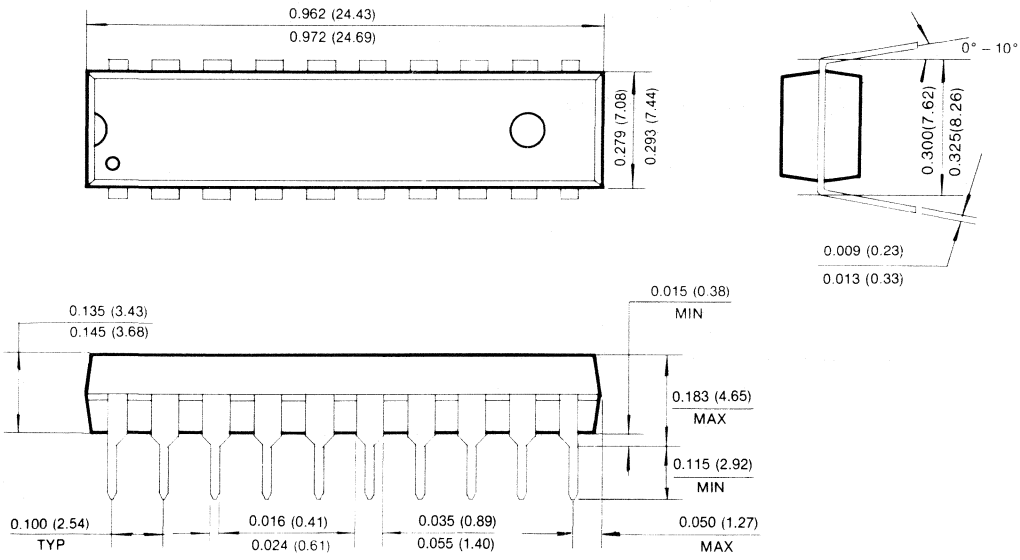
In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

2

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

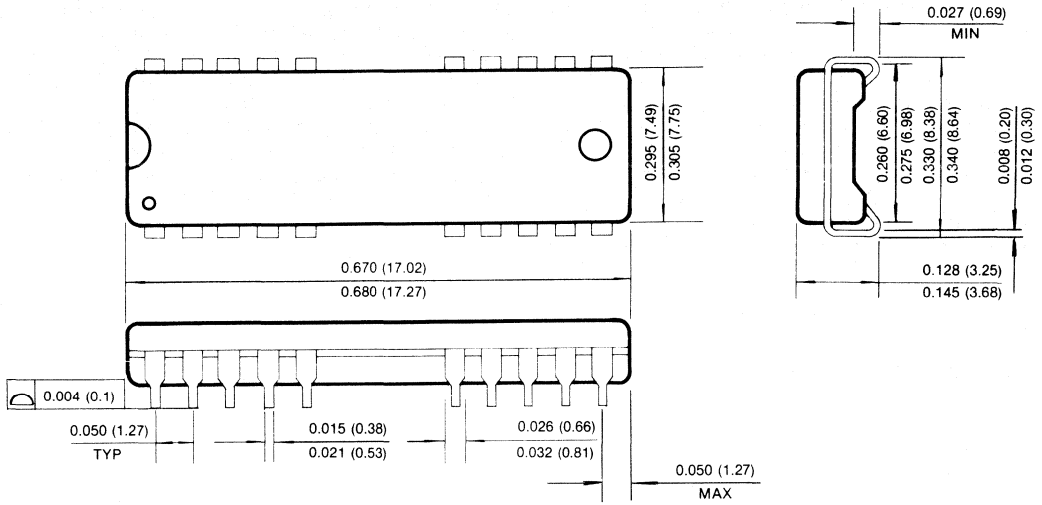
Units: Inches (Millimeters)



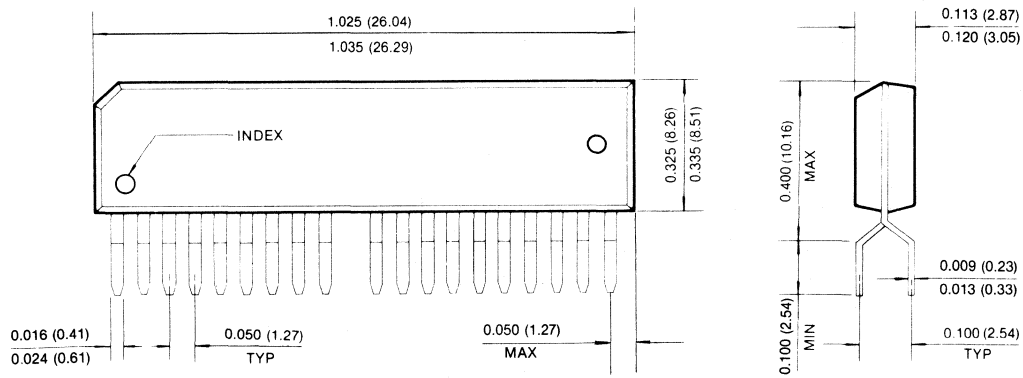
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



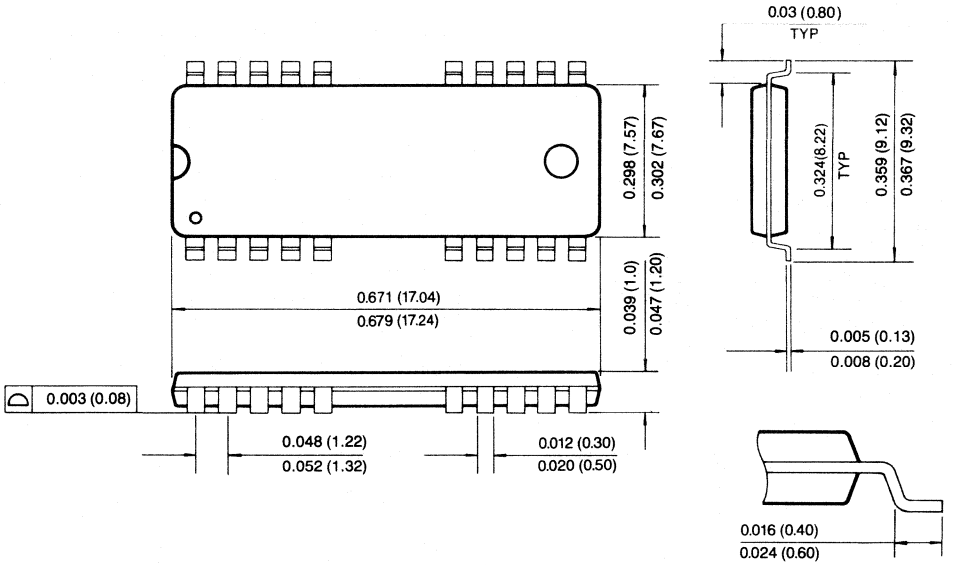
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



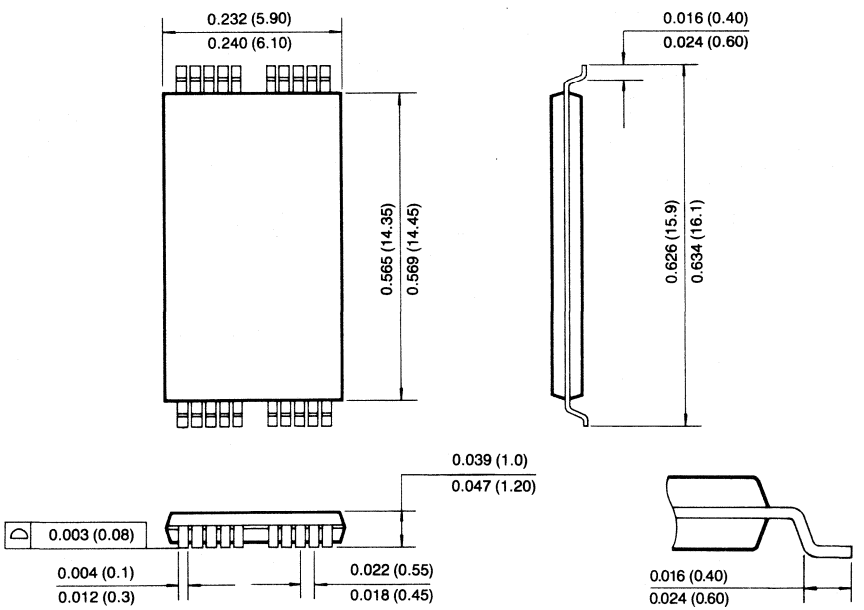
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (I) (Forward and Reverse Type)



256K X 4 Bit CMOS Dynamic RAM with Fast Page Mode (Write Per Bit Mode)

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C266C-6	60ns	15ns	110ns
KM44C266C-7	70ns	20ns	130ns
KM44C266C-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Write Per Bit Mode Capability**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and output**
- **Early write or Output Enable Controlled Write**
- **Single +5V±10% power supply**
- **512 cycles/8ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic DIP, SOJ and ZIP**

GENERAL DESCRIPTION

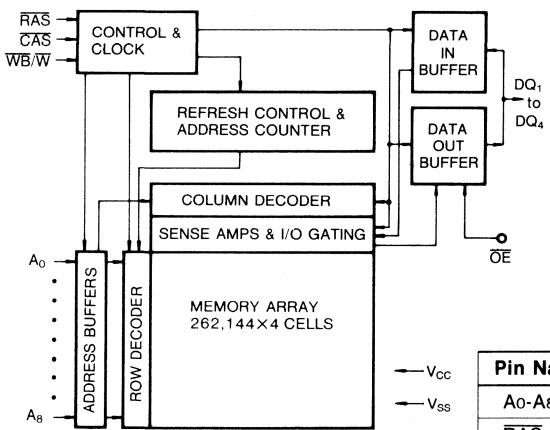
The Samsung KM44C266C is a high speed CMOS 262,144×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C266C features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

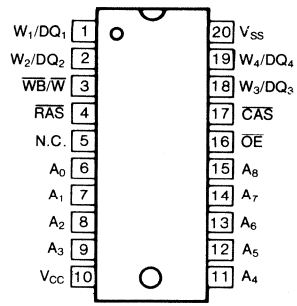
The KM44C266C is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

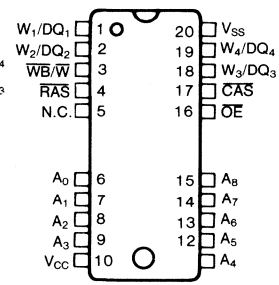


PIN CONFIGURATION (Top Views)

- **KM44C266CP**

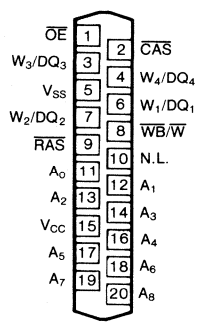


- **KM44C266CJ**



Pin Name	Pin Function
A0-A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB}/\overline{W}$	Write Per Bit/Read/Write Input
$\overline{OE}$	Data Output Enable
$W_1/DQ_1 \sim W_4/DQ_4$	Write Select/Data In, Out
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection
N.L.	No Lead

- **KM44C266CZ**



ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC} = min.)	KM44C266C-6	I_{CC1}	—	70	mA
	KM44C266C-7		—	65	mA
	KM44C266C-8		—	60	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM44C266C-6	I_{CC3}	—	70	mA
	KM44C266C-7		—	65	mA
	KM44C266C-8		—	60	mA
Fast Page Mode Current* ($\overline{CAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC} = min.)	KM44C266C-6	I_{CC4}	—	55	mA
	KM44C266C-7		—	50	mA
	KM44C266C-8		—	45	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min.)	KM44C266C-6	I_{CC6}	—	70	mA
	KM44C266C-7		—	65	mA
	KM44C266C-8		—	60	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test = 0V)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. I_{CC1}, I_{CC3} Address can be changed maximum two times while $\overline{RAS}$ = V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CAS}$ = V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_8, D)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (W_1/DQ_1-W_4/DQ_4)	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC} = 5.0V ± 10%, See notes 1, 2)

Parameter	Symbol	KM44C266C-6		KM44C266C-7		KM44C266C-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		175		195		ns	
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-write cycle time	t_{PRWC}	80		85		90		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		35		40	ns	3
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
$\overline{CAS}$ precharge time (CBR mode)	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	15		15		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	50		55		60		ns	6

AC CHARACTERISTICS (Continued)

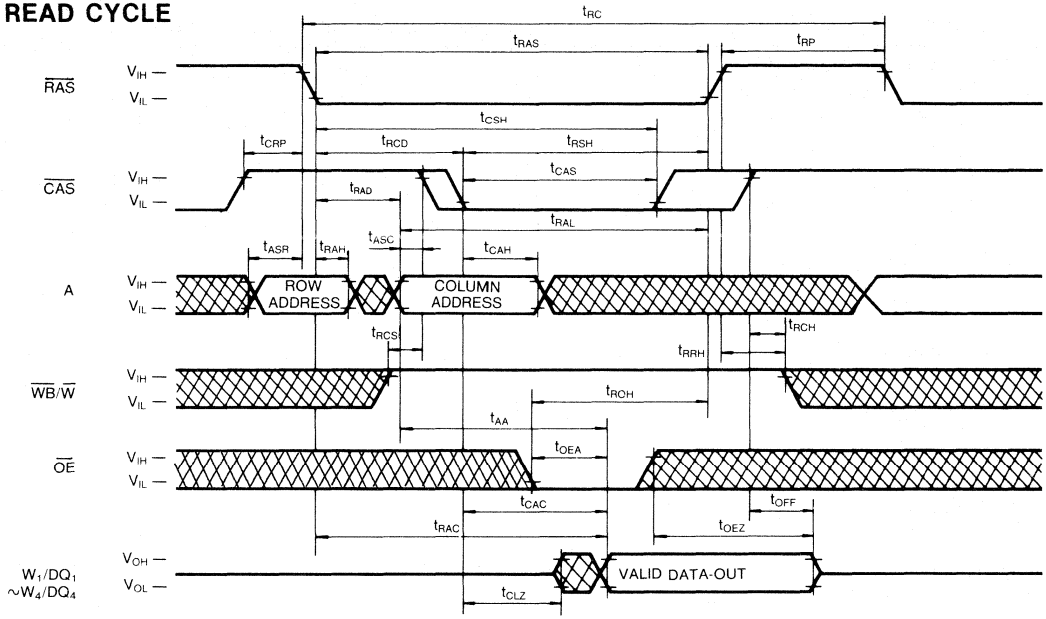
Parameter	Symbol	KM44C266C-6		KM44C266C-7		KM44C266C-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command pulse width	t_{WP}	15		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period	t_{REF}		8		8		8	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		45		45		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		95		105		ns	8
Column address to W delay time	t_{AWD}	55		60		65		ns	8
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	15		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	20		25		30		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	15		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	15		20		20		ns	
Write per bit set-up time	t_{WBS}	0		0		0		ns	
Write per bit hold time	t_{WBH}	10		10		15		ns	
Write per bit selection set-up time	t_{WDS}	0		0		0		ns	
Write per bit selection hold time	t_{WDH}	10		10		15		ns	

NOTES

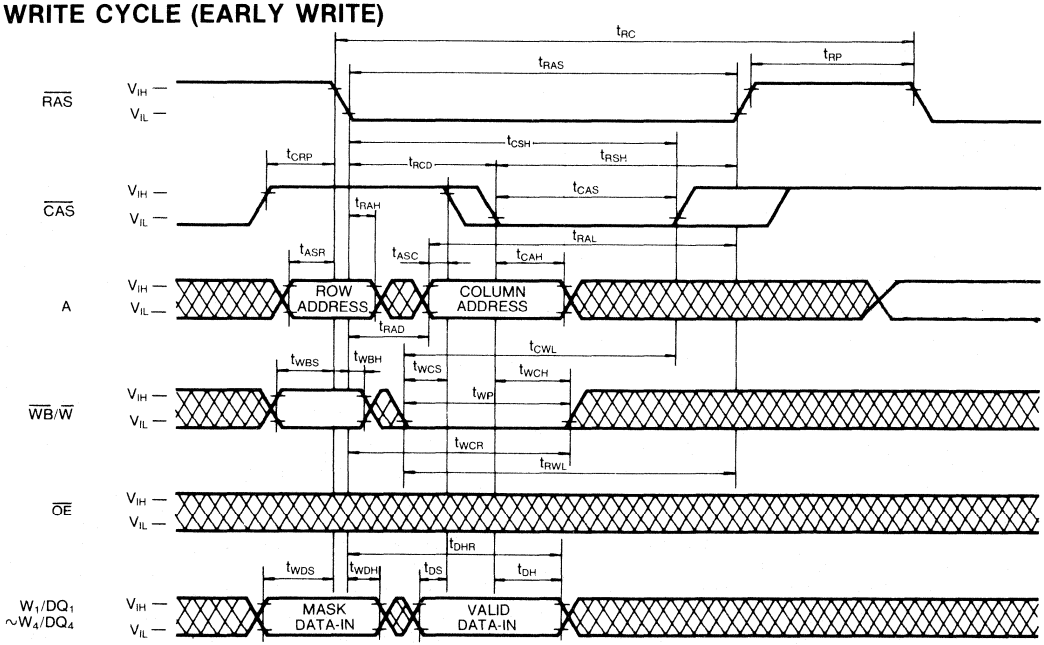
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \leq t_{RCD}$(max).
6. t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the W leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. Operation within the t_{LWAD}(max) limit insures that t_{ALW}(max) can be met. t_{LWAD}(max) is specified as a reference point only. If t_{LWAD} is greater than the specified t_{LWAD}(max) limit, then access time is controlled by t_{AA}.

TIMING DIAGRAMS

READ CYCLE

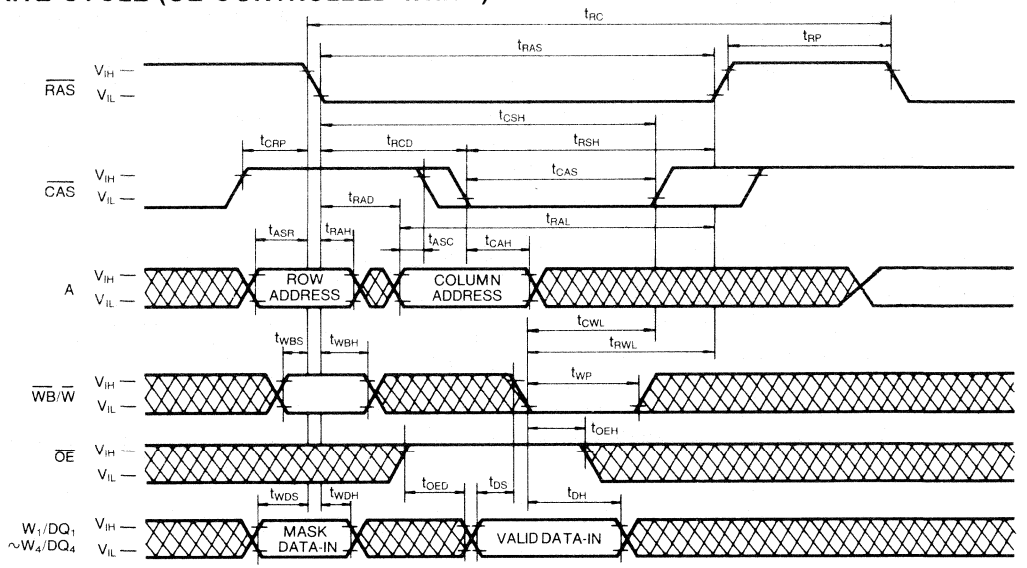


WRITE CYCLE (EARLY WRITE)

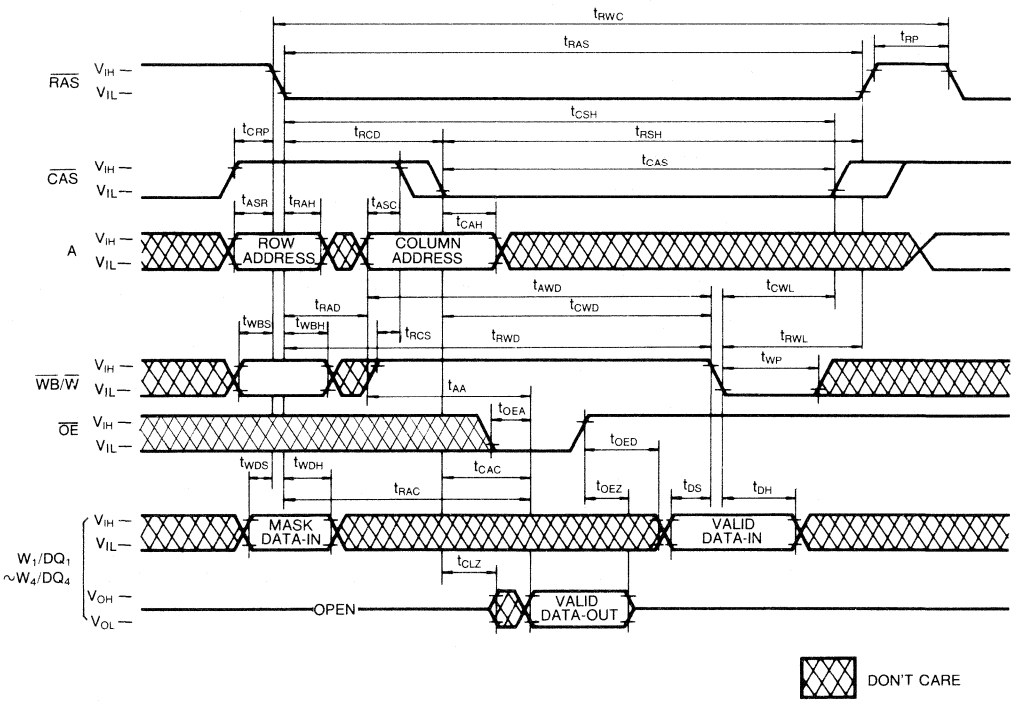


TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

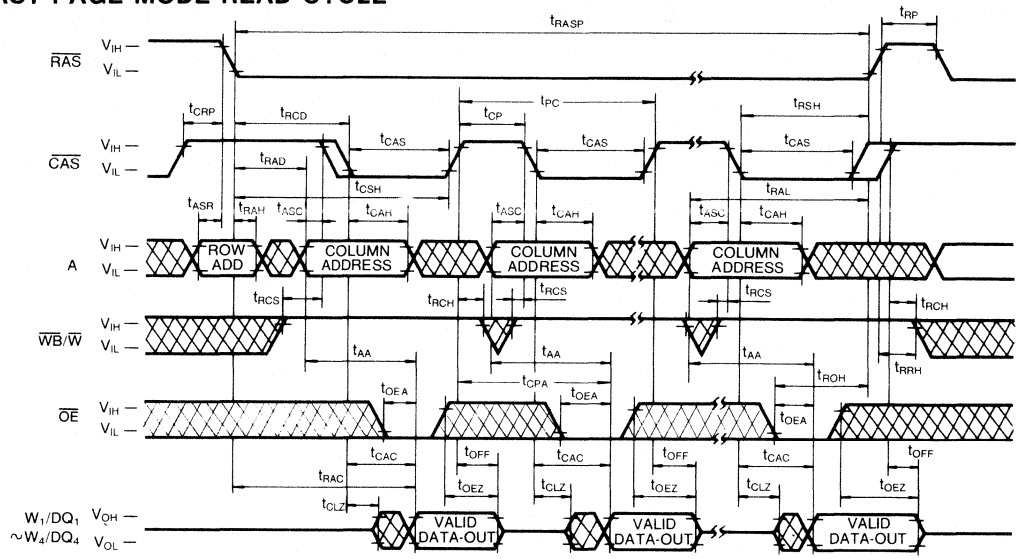


READ-MODIFY-WRITE CYCLE

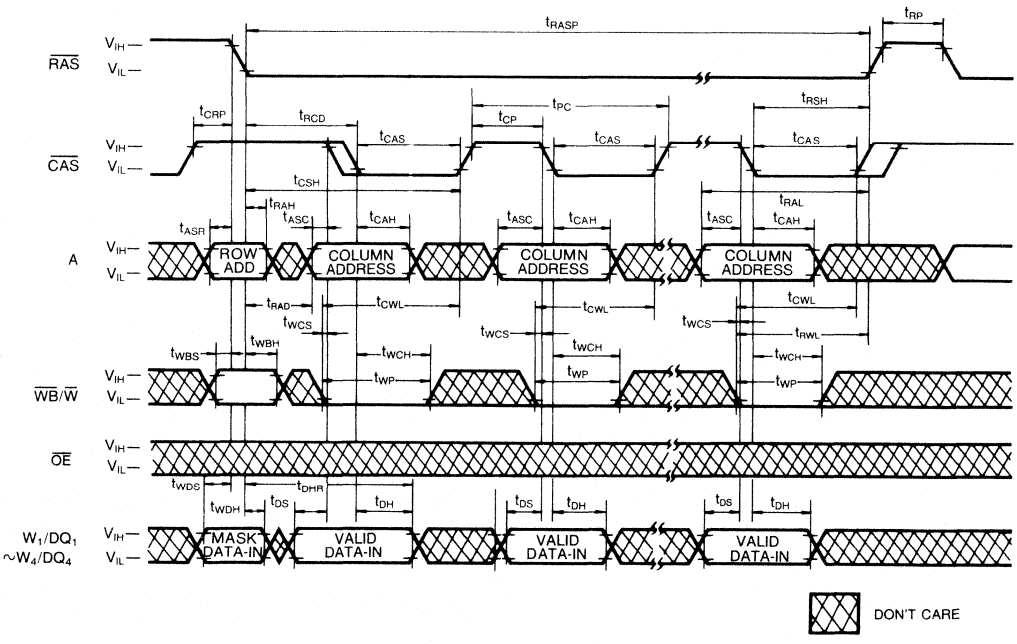


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE

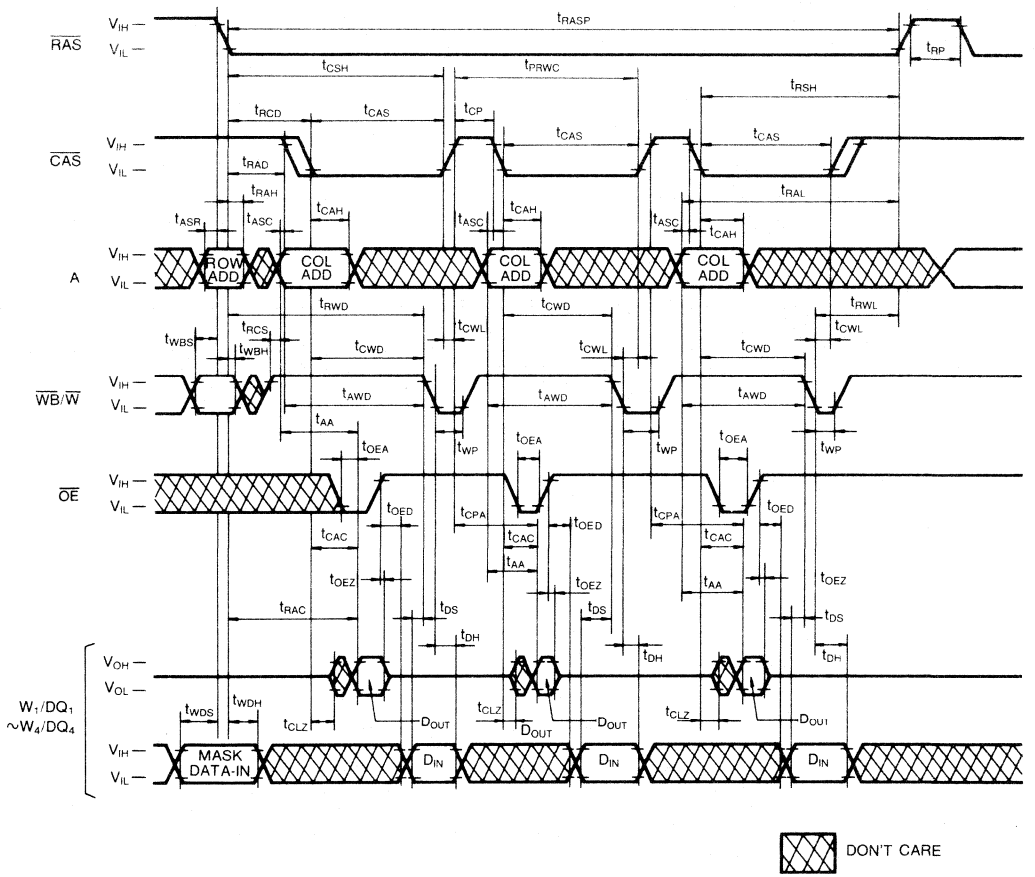


FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

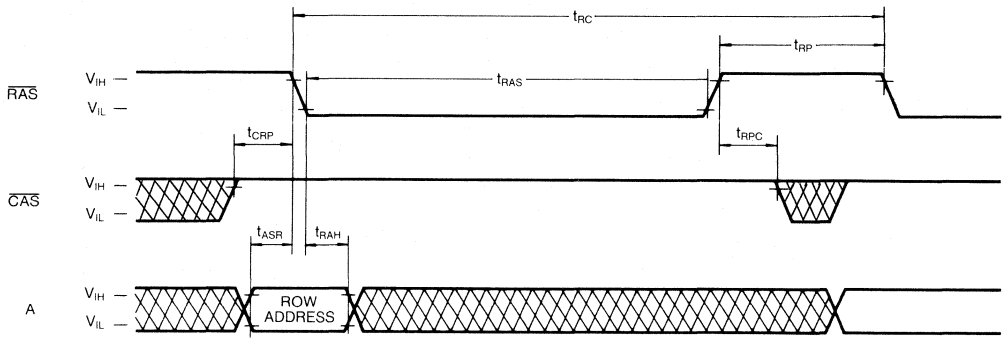
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

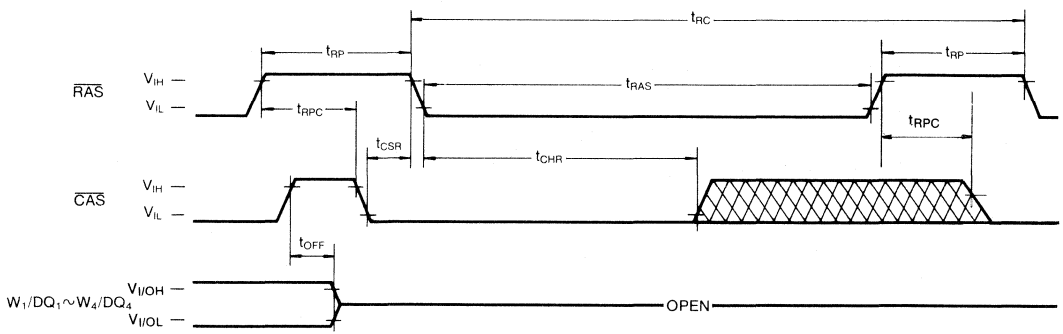
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{WB}/\overline{W}$, $\overline{OE}$=Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

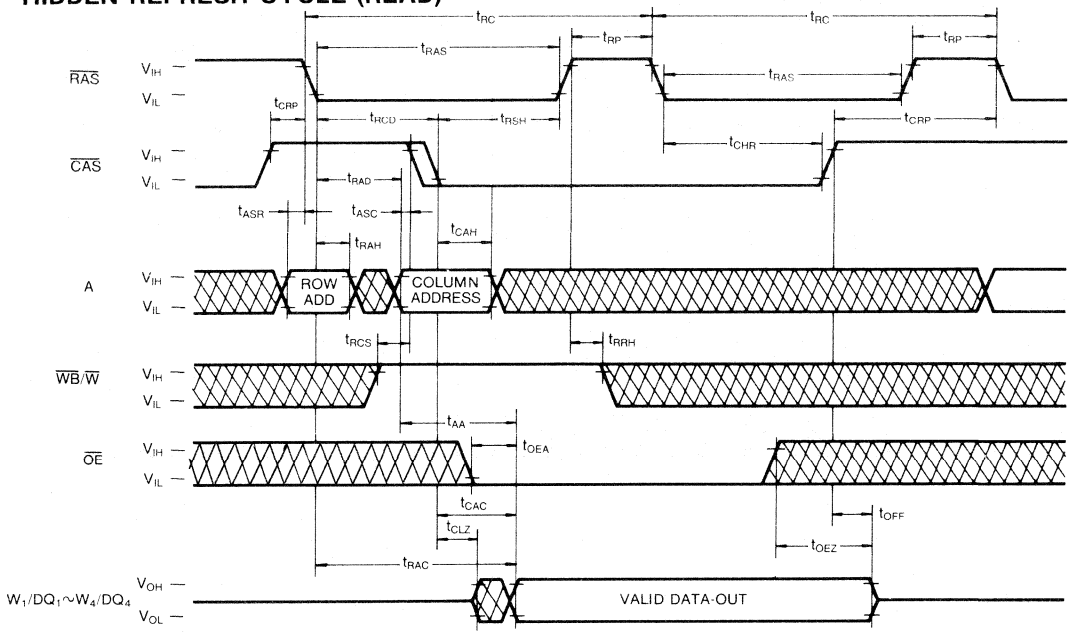
NOTE: $\overline{WB}/\overline{W}$, $\overline{OE}$, A=Don't Care



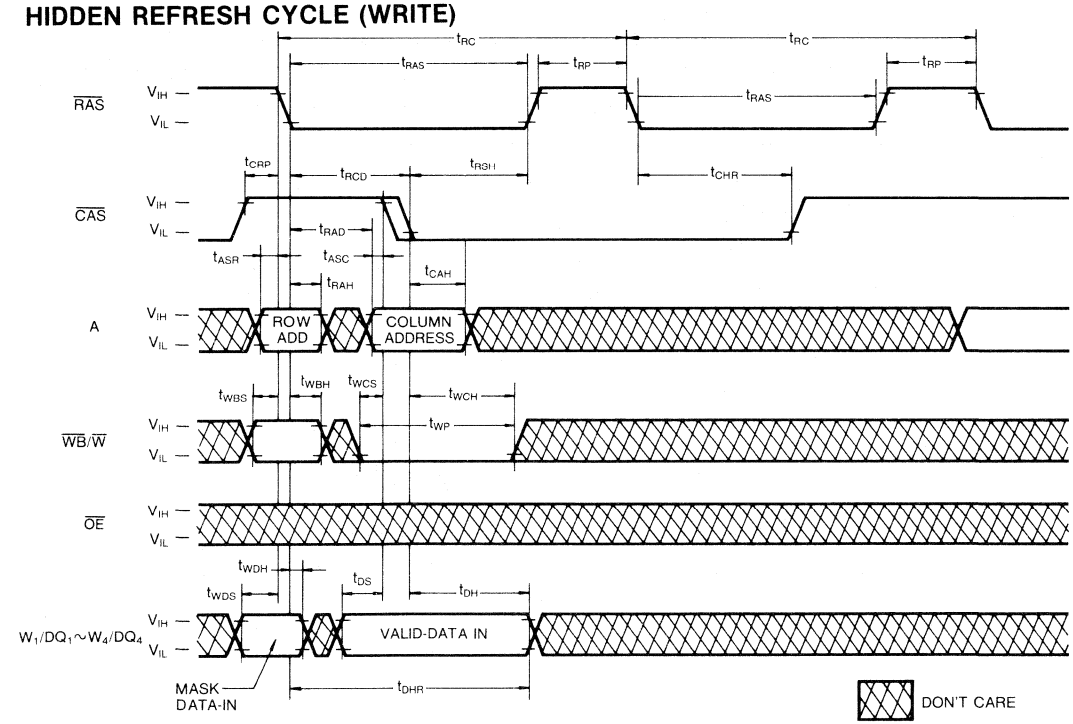
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

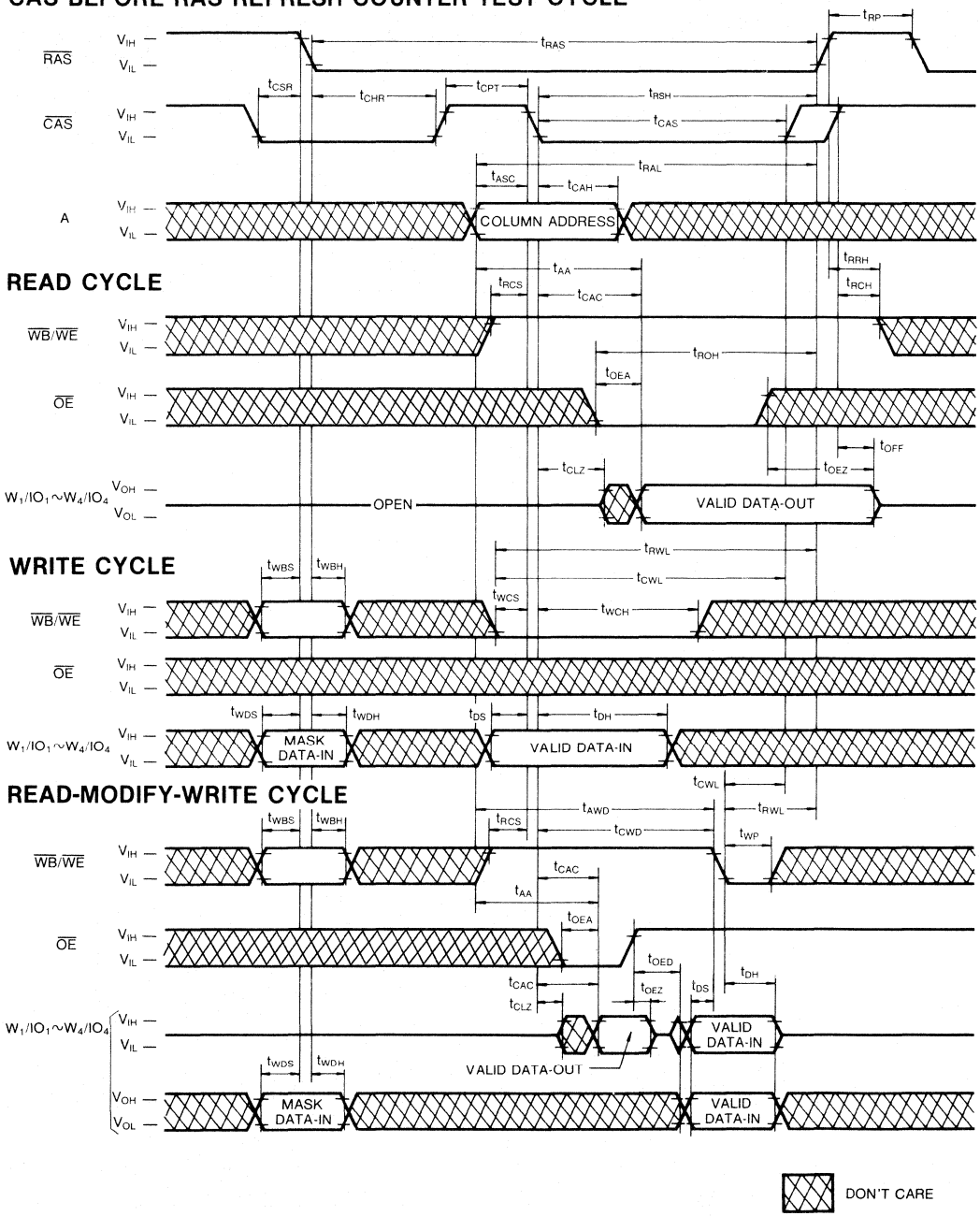


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM44C266C contains 1,048,576 memory locations organized as 262,144 four-bit words. Eighteen address bits are required to address a particular 4-bit word in the memory array. Since the KM44C266C has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the KM44C266C begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C266C cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by $t_{RAS(min)}$ and $t_{CAS(min)}$ respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C266C begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before $t_{RCD(max)}$ and if the column address is valid before $t_{RAD(max)}$ then the access time to valid data is specified by $t_{RAC(min)}$. However, if $\overline{CAS}$ goes low after $t_{RAD(max)}$, access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, $t_{RAC(min)}$, it is necessary to meet both $t_{RCD(max)}$ and $t_{RAD(max)}$.

The KM44C266C has common data I/O pins. For this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44C266C can perform early write. $\overline{OE}$ controlled write and read-modify-write cycles. Each of these write cycles is achieved by maintaing the write per bit write enable ($\overline{WB}/\overline{W}$) input high at the falling edge of $\overline{RAS}$. If write-per bit function is performed, $\overline{WB}/\overline{W}$ is kept low at the falling edge of $\overline{RAS}$. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CAS}$ IN any type of write cycle, Data-in must be valid at or before the failing edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain the he Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. This output enable input ($\overline{OE}$) must be low during the time defined by $t_{OEA}$and t_{OEZ} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met the output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM44C266C 's DQ pins.

Write-Per-Bit

Write-per-bit function is performed in the write cycle, that is early write. $\overline{OE}$ controlled write, read-modify-write. Write-per-bit markes it possible selectively to write one or more of the four I/O pins. To perform write per-bit function at the falling edge of $\overline{RAS}$ the write-per-bit/Write enable ($\overline{WB}/\overline{W}$) is kept low and at the same time Mask data of input pins to write among 4 I/O pins must be in high. If I/O pins that Mask data is kept low, write operation is inhibited.

Data Output

The KM44C266C , has a three state output buffer which are controlled by $\overline{CAS}$ and $\overline{OE}$. When either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}) the output are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} sepcify

DEVICE OPERATION (Continued)

when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C266C operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} are not met)

Refresh

The data in the KM44C266C is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 8 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A_0-A_8).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C266C has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C266C hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C266C by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A_0 through A_8 are supplied by the on-chip refresh counter. The A_9 bit is set low internally.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle.

Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-up

If $\overline{RAS}=V_{SS}$ during power-up, the KM44C266C could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up courrent.

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C266C inputs act like unterminated transmission lines resulting in significant positive and negative overshoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C266C input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. the recommended methods are

DEVICE OPERATION (Continued)

gridded power and ground lines orseparate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with may DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

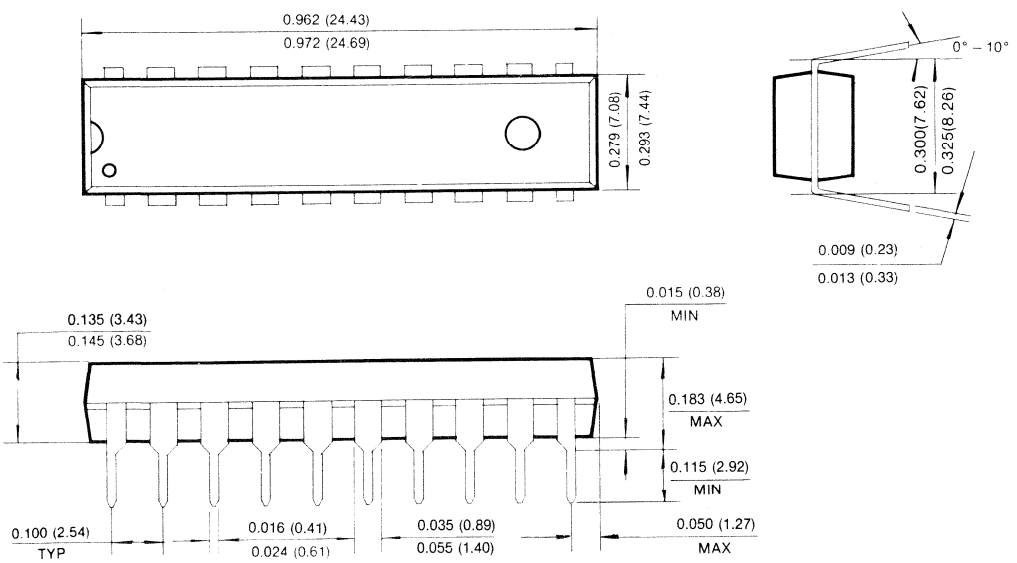
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM44C266C using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C266C and they supply much of the current used by the KM44C266C during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

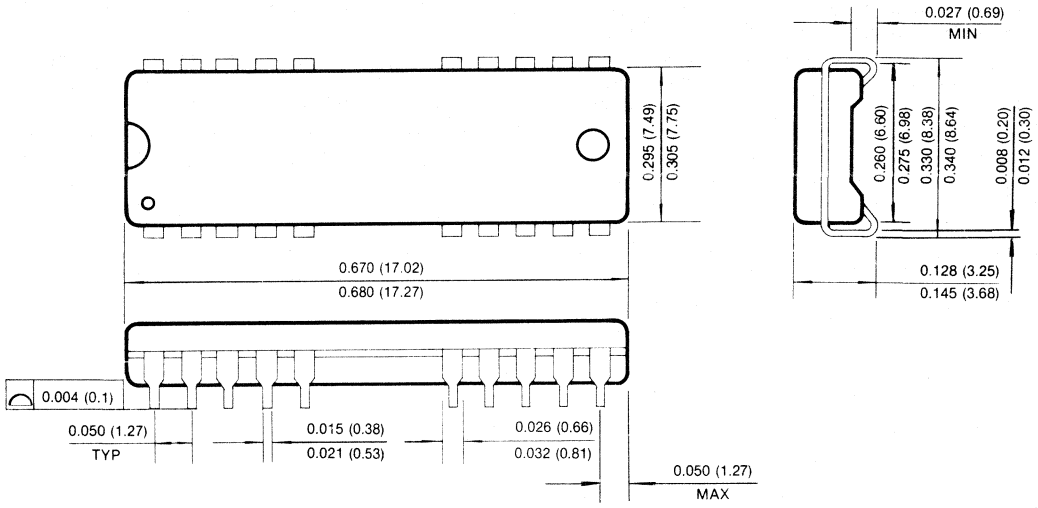
Units: Inches (Millimeters)



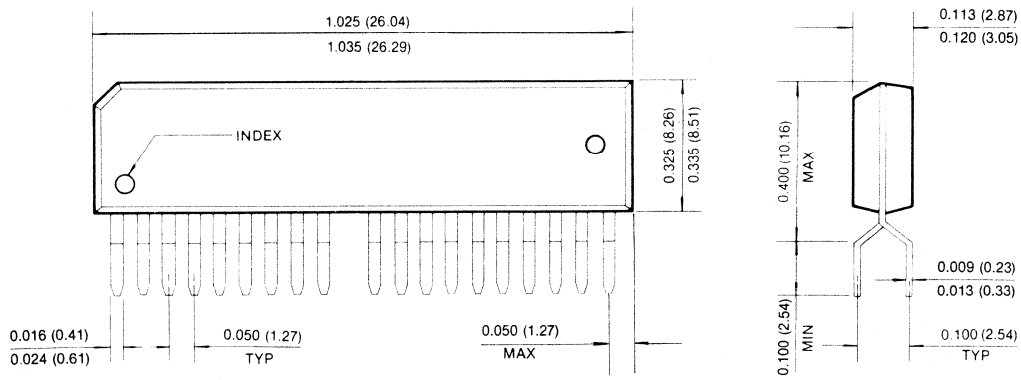
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



262,144 x 4 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C258C-6	60ns	15ns	110ns
KM44C258C-7	70ns	20ns	130ns
KM44C258C-8	80ns	20ns	150ns

- **Static Column Mode operation**
- **$\overline{CS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and output**
- **Early Write or Output Enable Controlled Write**
- **Single +5V ± 10% power supply**
- **512 cycles/8ms refresh**
- **JEDEC standard pinout**
- **Available in plastic DIP, SOJ and ZIP**

GENERAL DESCRIPTION

The Samsung KM44C258C is a CMOS high speed 262,144 x 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

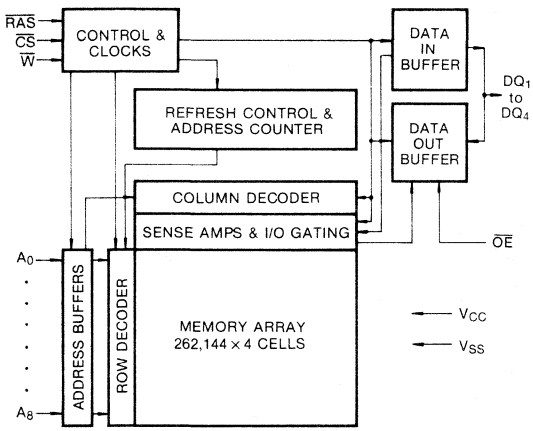
Static Column Mode Operation allows high speed random or sequential access within a row. The KM44C258C offers high performance while relaxing many critical system timing requirements for fast usable speed.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and outputs are fully TTL compatible.

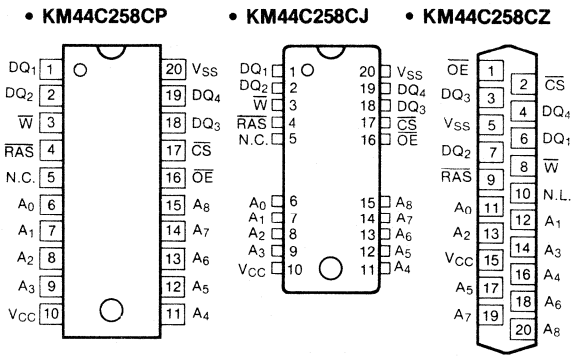
The KM44C258C is fabricated using Samsung's advanced CMOS process.

2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A_0-A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select input
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
DQ_1-DQ_4	Data In/Data Out
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection
N.L.	No Lead

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling @t_{RC} = min.)	KM44C258C-6	I_{CC1}	—	70	mA
	KM44C258C-7		—	65	mA
	KM44C258C-8		—	60	mA
Standby Current ($\overline{RAS}$ = $\overline{CS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current ($\overline{CS}$ = V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM44C258C-6	I_{CC3}	—	70	mA
	KM44C258C-7		—	65	mA
	KM44C258C-8		—	60	mA
Static Column Mode Current ($\overline{RAS}$ = $\overline{CS}$ = V_{IL}, Address Cycling @t_{PC} = min.)	KM44C258C-6	I_{CC4}	—	55	mA
	KM44C258C-7		—	50	mA
	KM44C258C-8		—	45	mA
Standby Current ($\overline{RAS}$ = $\overline{CS}$ = V_{CC} − 0.2V)		I_{CC5}	—	1	mA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{RC} = min.)	KM44C258C-6	I_{CC6}	—	70	mA
	KM44C258C-7		—	65	mA
	KM44C258C-8		—	60	mA
Input Leakage Current (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. I_{CC1}, I_{CC3} Address can be changed maximum two times while $\overline{RAS}$ = V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CS}$ = V_{IH}.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_8)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{DQ}	—	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$, See notes 1, 2)

Parameter	Symbol	KM44C258C-6		KM44C258C-7		KM44C258C-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		175		195		ns	
Static column mode cycle time	t_{SC}	35		40		45		ns	
Static column mode read-write cycle time	t_{SRWC}	90		100		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
Access time from last write	t_{ALW}		60		70		80	ns	3,12
$\overline{CS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Output data hold time from column address	t_{AOH}	5		5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		25		25		25	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width (static column mode)	t_{RASC}	60	100,000	70	100,000	80	100,000	ns	
$\overline{CS}$ to $\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{RAS}$ to $\overline{CS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CS}$ pulse width	t_{CS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	15	100,000	20	100,000	20	100,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
$\overline{CS}$ precharge time (static column mode)	t_{CP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	

AC CHARACTERISTICS (Continued)

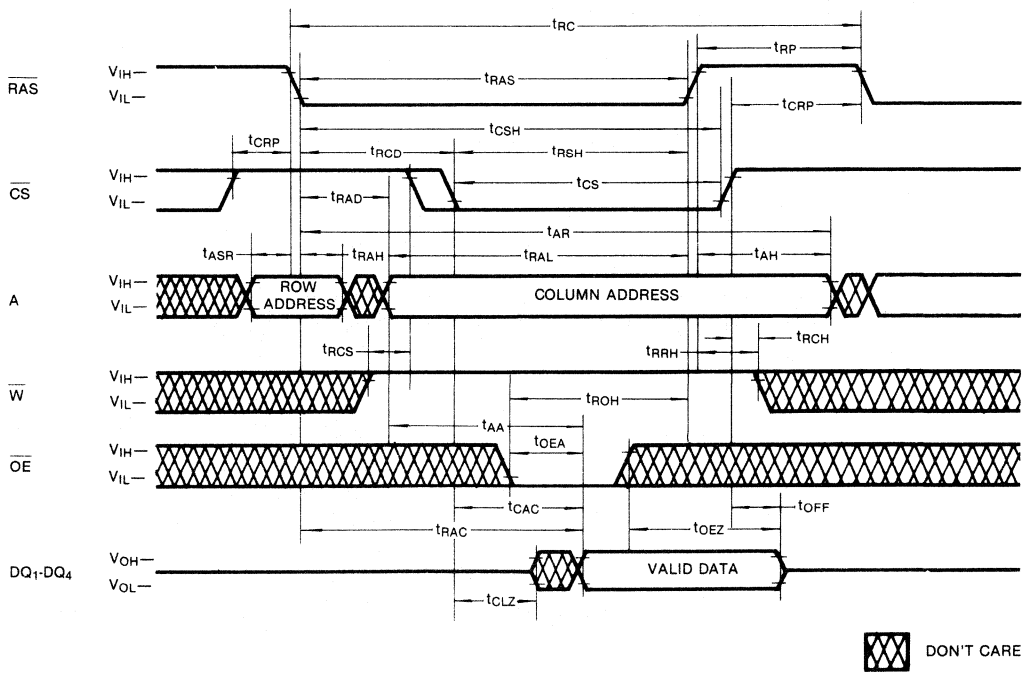
Parameter	Symbol	KM44C258C-6		KM44C258C-7		KM44C258C-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Column address hold time	t_{CAH}	15		15		15		ns	
Write address hold time referenced to $\overline{RAS}$	t_{AWR}	50		55		60		ns	6
Column address hold time referenced to $\overline{RAS}$	t_{AR}	70		80		90		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Column address hold time referenced to $\overline{RAS}$ rise	t_{AH}	5		5		5		ns	
Last write to column address delay time	t_{LWAD}	20	30	20	35	20	40	ns	12
Last write to column address hold time	t_{AHLW}	60		70		80		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	50		55		60		ns	6
Write command pulse width	t_{WP}	15		15		15		ns	
Write command inactive time	t_{WI}	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		15		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (512 cycles)	t_{REF}		8		8		8	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CS}$ to $\overline{W}$ delay time	t_{CWD}	40		45		45		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		95		105		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		60		65		ns	8
$\overline{CS}$ setup time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{SCR}	5		5		5		ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	15		15		15		ns	
$\overline{RAS}$ to $\overline{CS}$ hold time	t_{RPC}	5		5		5		ns	
$\overline{CS}$ precharge time ($\overline{CS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	20		25		30		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	15		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	15		15		15		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AWR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. Operation within the t_{LWAD}(max) limit insures that t_{ALW}(max) can be met. t_{LWAD}(max) is specified as a reference point only. If t_{LWAD} is greater than the specified t_{LWAD}(max) limit, then access time is controlled by t_{AA}.

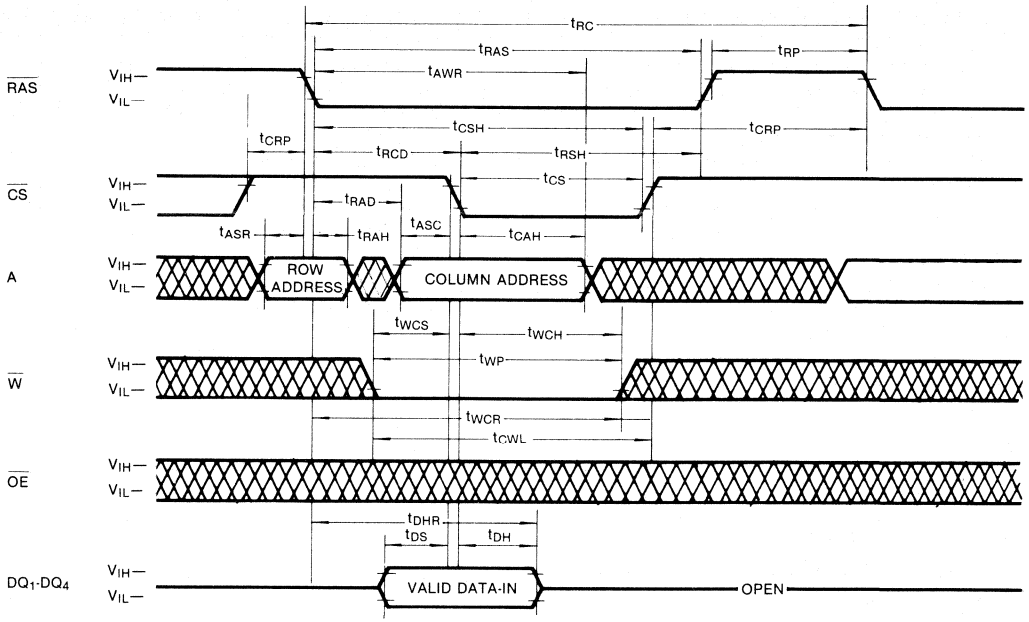
TIMING DIAGRAMS (Continued)

READ CYCLE

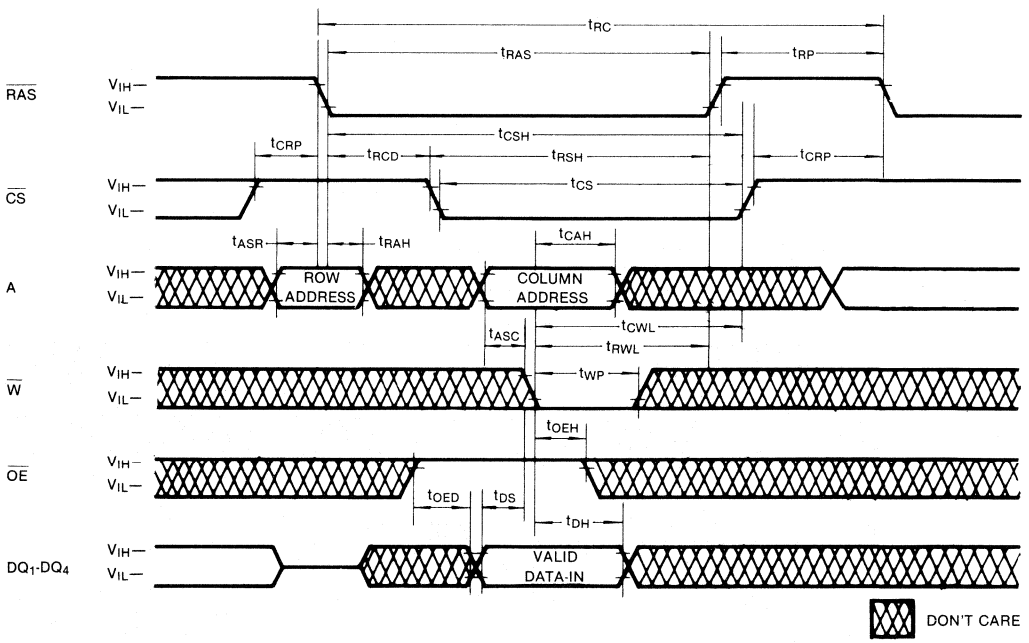


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

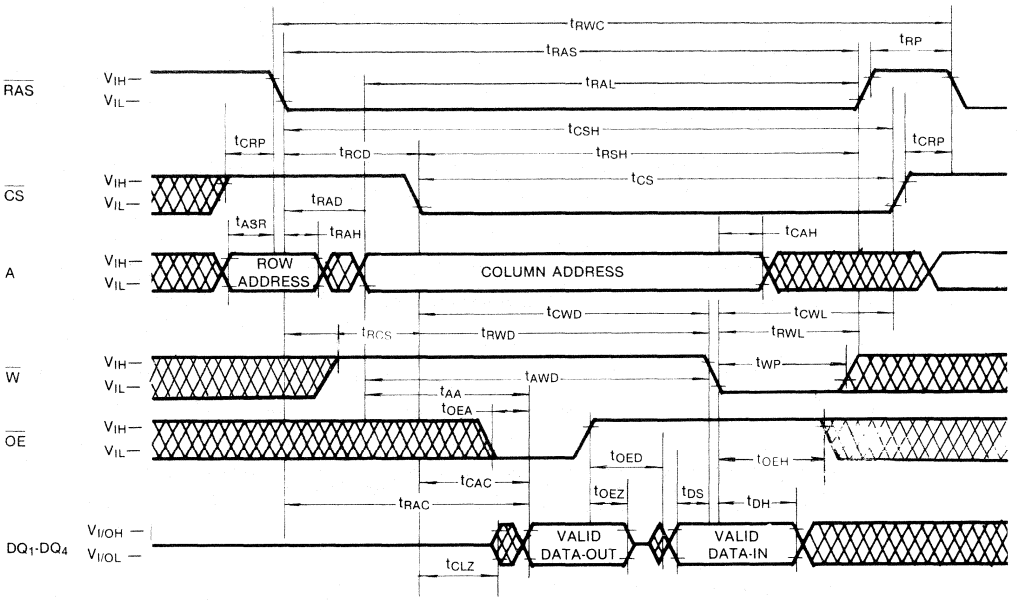


WRITE CYCLE (OE CONTROLLED WRITE)

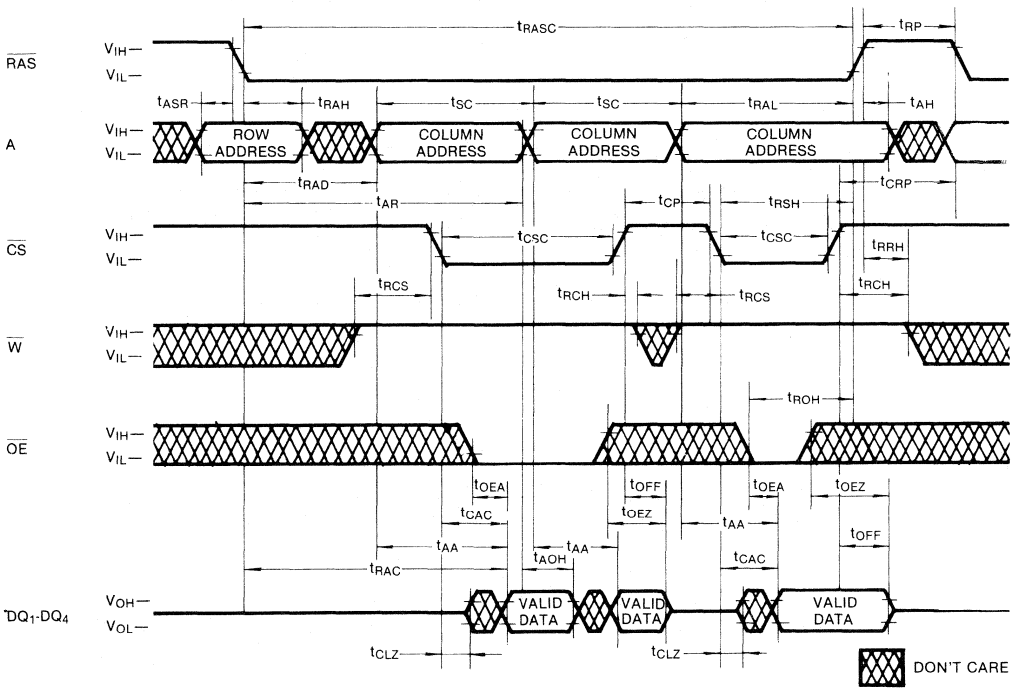


TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

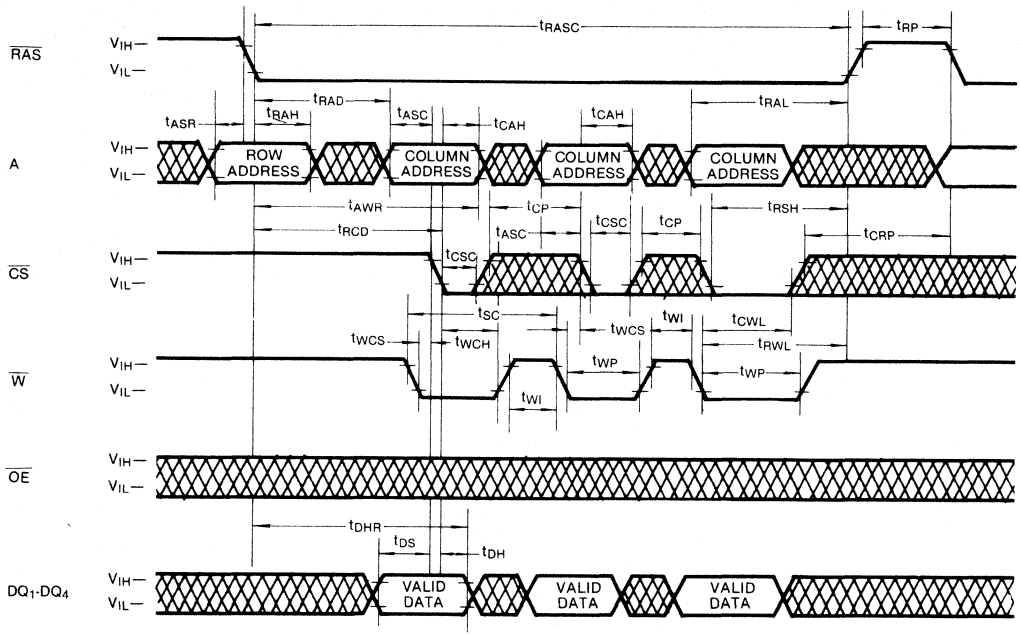


STATIC COLUMN MODE READ CYCLE

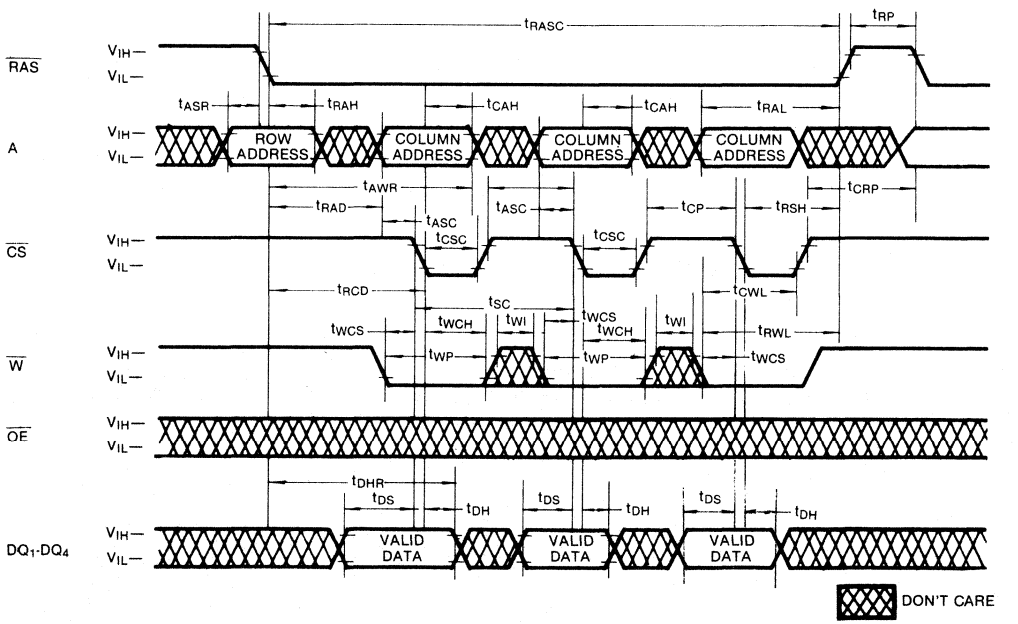


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ controlled early write)

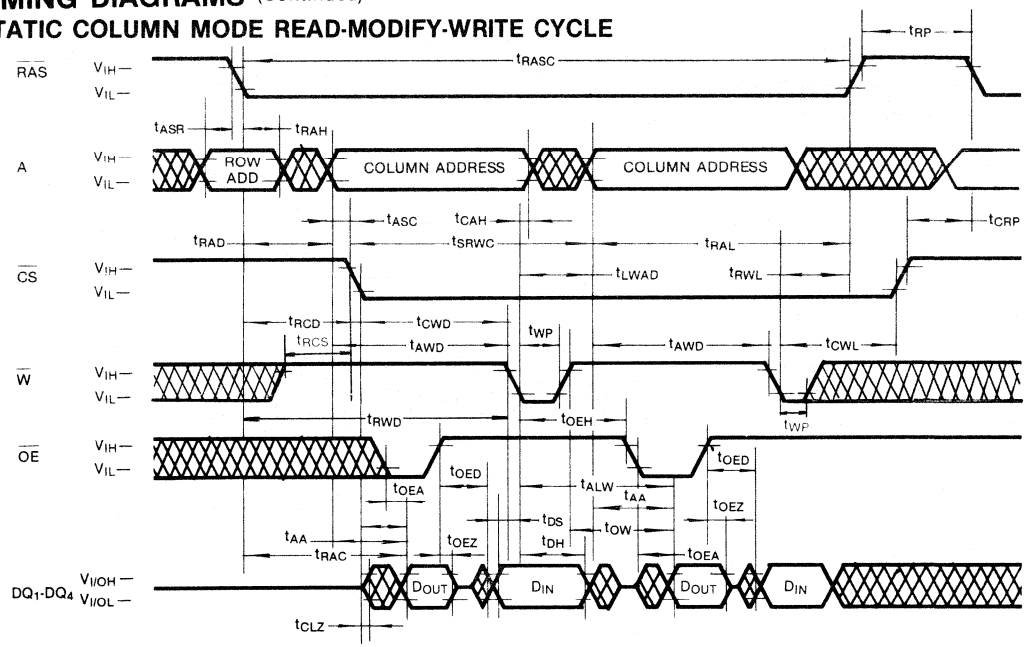


STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ controlled early write)

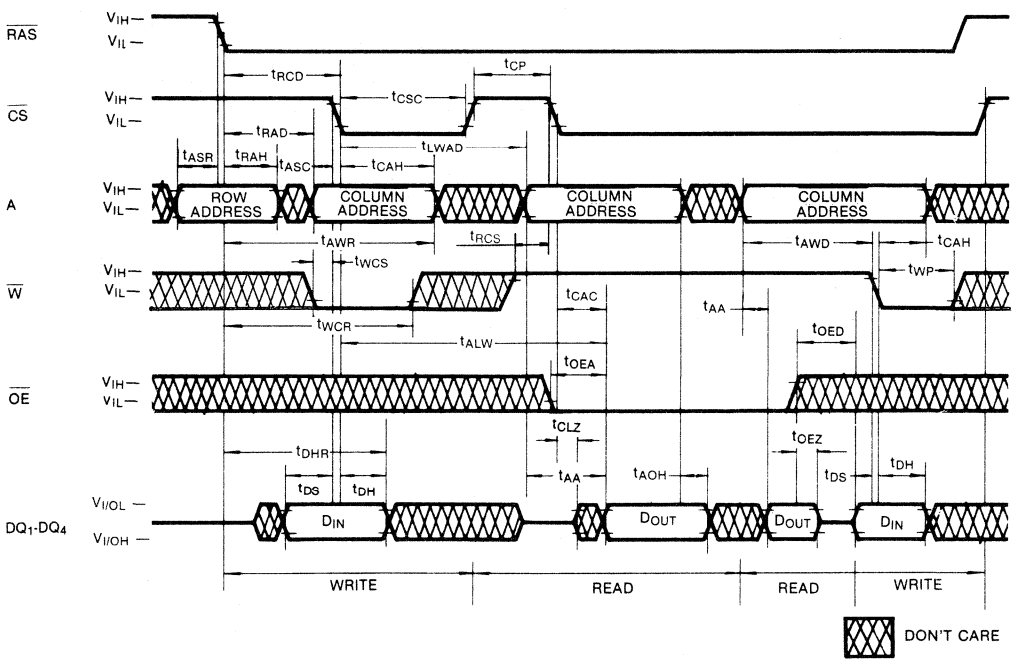


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



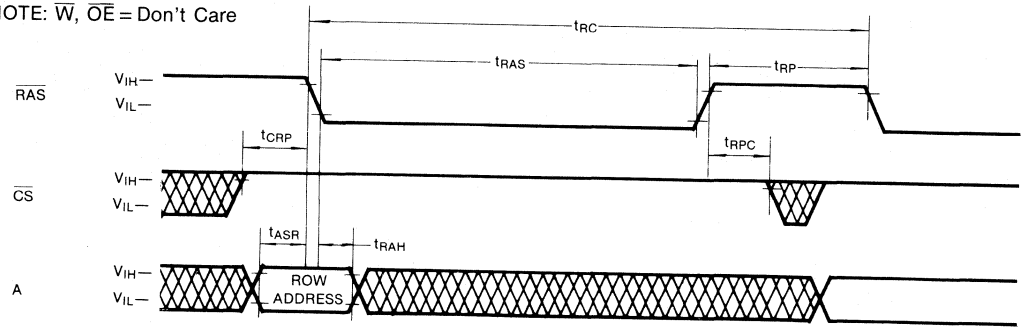
STATIC COLUMN MODE MIXED CYCLE



TIMING DIAGRAMS (Continued)

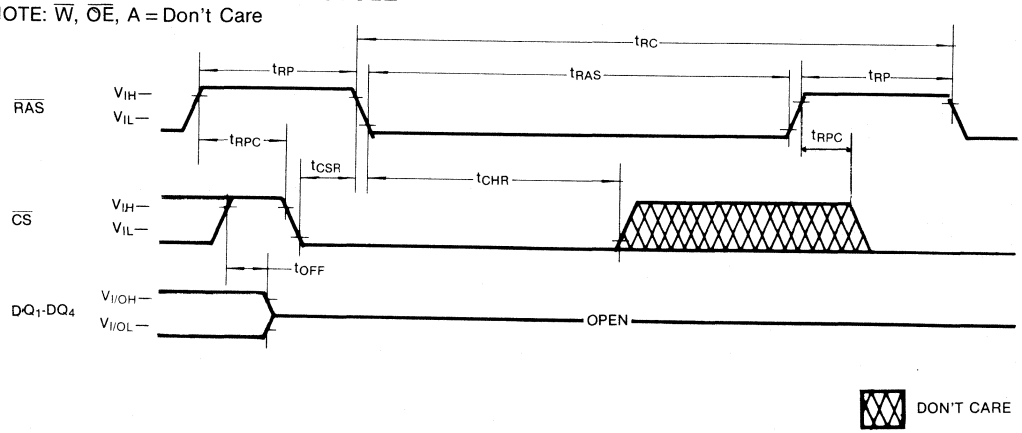
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$ = Don't Care



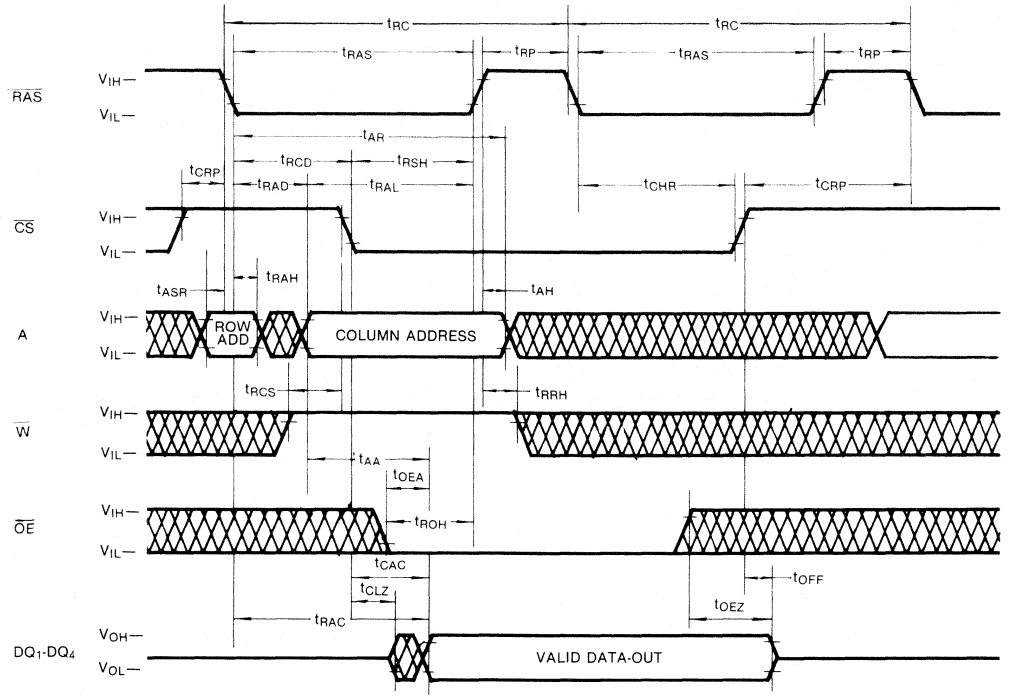
$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care

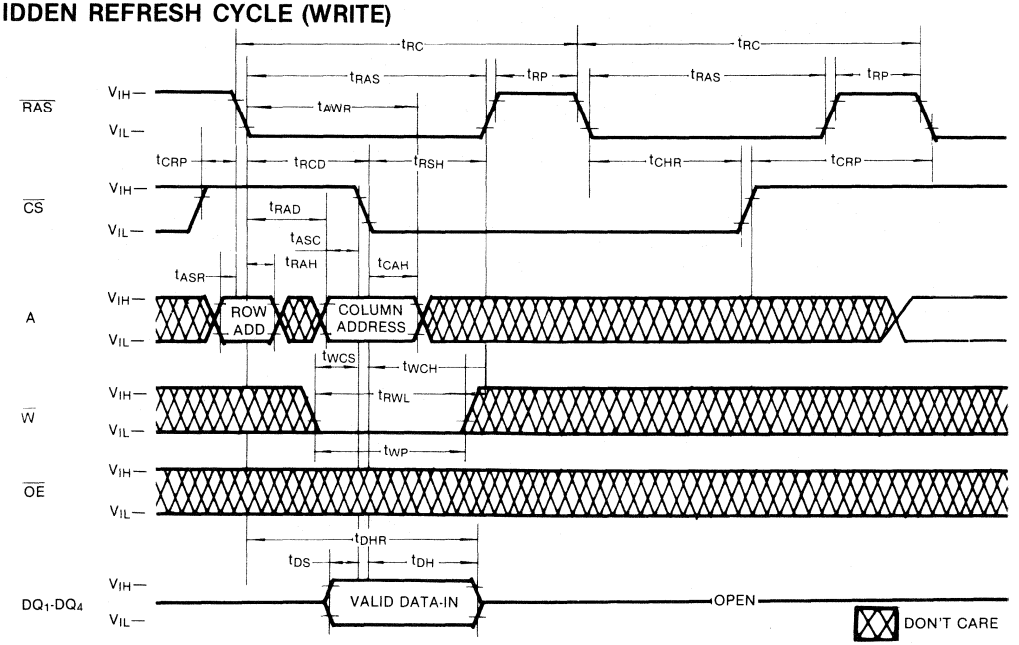


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

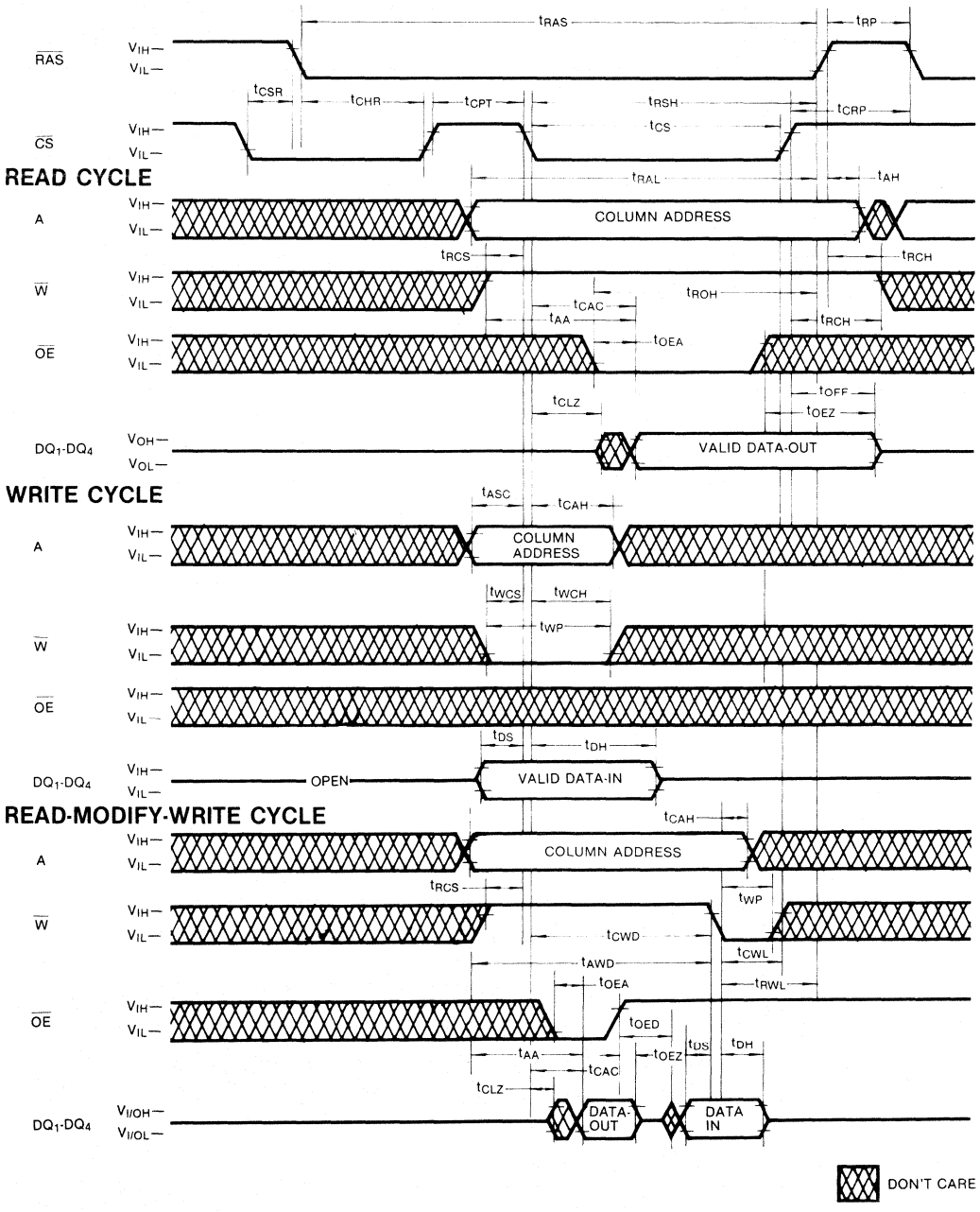


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM44C258C contains 1,048,576 memory locations organized as 262,144 four-bit words. Eighteen address bits are required to address a particular 4-bit word in the memory array. Since the KM44C258C has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CS}$) and the valid row and column address inputs.

Operation of the KM44C258C begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CS}$. This is the beginning of any KM44C258C cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths are specified by t_{RAS}(min) and t_{CS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C258C begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CS}$ and on the valid column address transition.

If $\overline{CS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

The KM44C258C has common data I/O pins. For this reason and output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44C258C can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the outputs remain in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CS}$ and meeting the data sheet read-modify-write cycle timing requirements. The output enable input ($\overline{OE}$) must be low during the time defined by t_{OEA} and t_{OEZ} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met the output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM44C258C's DQ pins.

Data Output

The KM44C258C has a three-state output buffer which is controlled by $\overline{CS}$ and $\overline{OE}$. When either $\overline{CS}$ or $\overline{OE}$ is high (V_{IH}) the output are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C258C operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Static Column Mode Read, Static Column Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Static Column Mode Write, $\overline{CS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} are not met)

Refresh

The data in the KM44C258C is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 8 ms. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A_0-A_8).

$\overline{CS}$-before-$\overline{RAS}$ Refresh: The KM44C258C has $\overline{CS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CS}$ active time and cycling $\overline{RAS}$. The KM44C258C hidden refresh cycle is actually a $\overline{CS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C258C by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CS}$ is brought high and then low again while RAS is held low, the read and write operations are enabled. In this mode, the row address bits A_0 through A_8 are supplied by the on-chip refresh counter. The A_9 bit is set low internally.

Static Column Mode

Static column mode allows high speed read, write or read-modify-write random access to all the memory cells within a selected row. Operation within a selected row is similar to a static RAM.

A static column mode read cycle starts as a normal cycle. Additional cells within the selected row are read by applying a new column address while $\overline{W} = V_{IH}$ and $\overline{RAS} = V_{IL}$.

A static column mode write cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{RAS} = V_{IL}$ and toggling either $\overline{W}$ or $\overline{CS}$. The data is written into the cell triggered by the latter falling edge of $\overline{W}$ or $\overline{CS}$.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM44C258C might begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C258C inputs act like unterminated transmission lines resulting in significant positive and negative overshoots at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C258C input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

DEVICE OPERATION (Continued)

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with may DRAMs these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on the memory boards to facilitate the shortest possible address and control lines to all the DRAMs.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

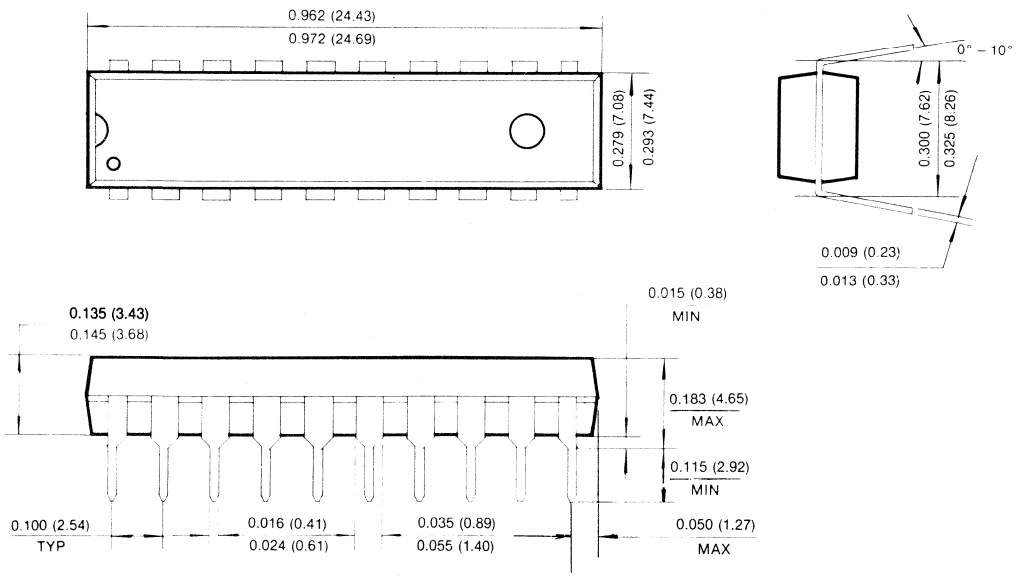
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each **KM44C258C** using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the **KM44C258C** and they supply much of the current used by the **KM44C258C** during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

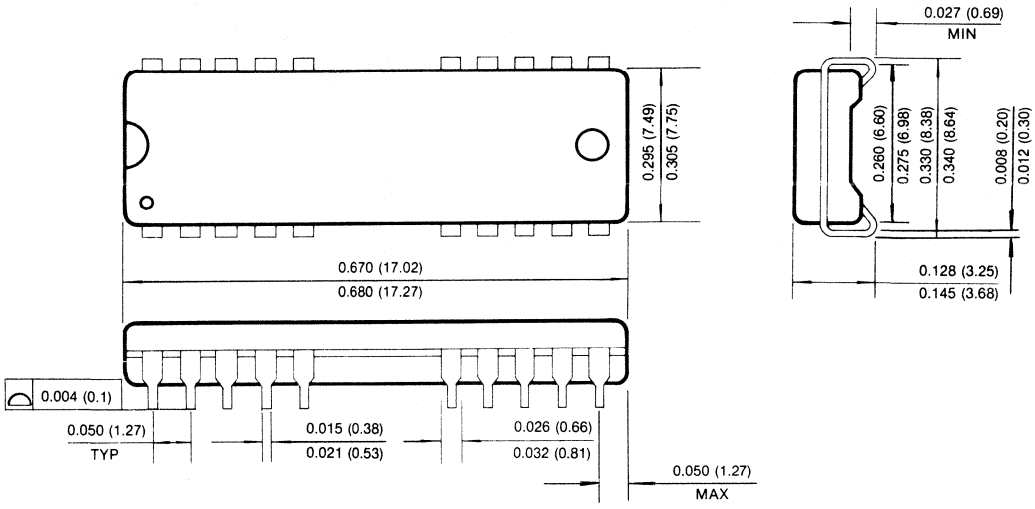
Units: Inches (millimeters)



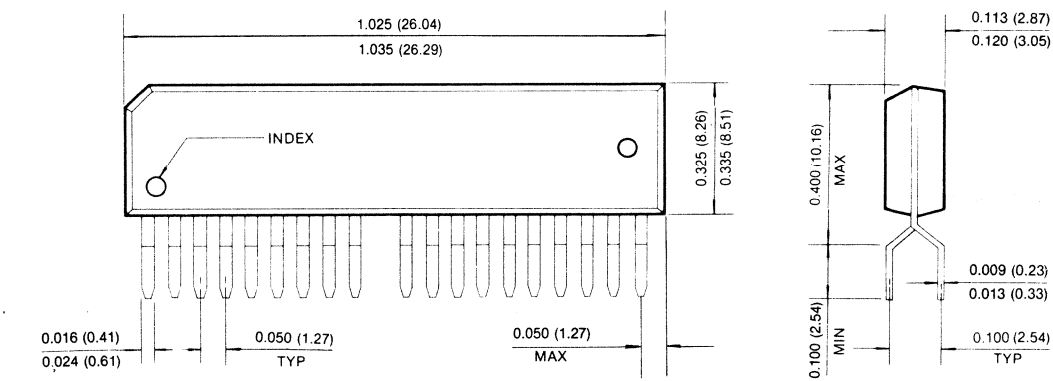
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



256K X 4 Bit CMOS Dynamic RAM with Static Column Mode (Write Per Bit Mode)

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C268C-6	60ns	15ns	110ns
KM44C268C-7	70ns	20ns	130ns
KM44C268C-8	80ns	20ns	150ns

- **Static Column Mode operation**
- **Write Per Bit Mode Capability**
- **$\overline{CS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and output**
- **Early write or Output Enable Controlled Write**
- **Single +5V±10% power supply**
- **512 cycles/8ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic DIP, SOJ and ZIP**

GENERAL DESCRIPTION

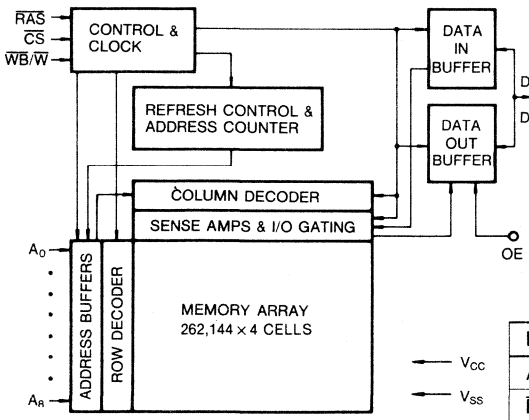
The Samsung KM44C268C is a high speed CMOS 262,144×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

Static Column Mode Operation allows high speed random or sequential access within a row. The KM44C268C offers high performance while relaxing many critical system timing requirements for fast usable speed.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

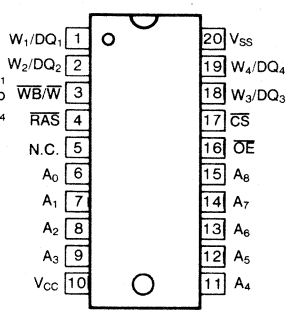
The KM44C268C is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

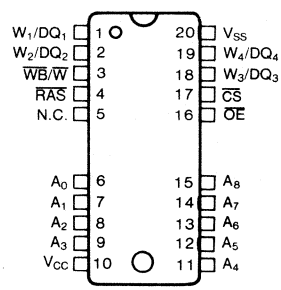


PIN CONFIGURATION (Top Views)

- **KM44C268CP**

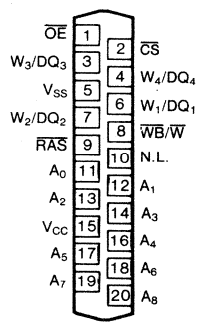


- **KM44C268CJ**



Pin Name	Pin Function
A0-A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
$\overline{WB}/\overline{W}$	Write Per Bit/Read/Write Input
$\overline{OE}$	Data Output Enable
W_1/DQ_1~ W_4/DQ_4	Write Select/Data In, Out
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection
N.L.	No Lead

- **KM44C268CZ**



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Value	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CS}$, Address Cycling @t_{RC} = min.)	KM44C268C-6	I_{CC1}	—	70	mA
	KM44C268C-7		—	65	mA
	KM44C268C-8		—	60	mA
Standby Current ($\overline{RAS}$ = $\overline{CS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CS}$ = V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM44C268C-6	I_{CC3}	—	70	mA
	KM44C268C-7		—	65	mA
	KM44C268C-8		—	60	mA
Static Column Mode Current ($\overline{RAS}$ = $\overline{CS}$ = V_{IL}, Address Cycling @t_{SC} = min.)	KM44C268C-6	I_{CC4}	—	55	mA
	KM44C268C-7		—	50	mA
	KM44C268C-8		—	45	mA
Standby Current ($\overline{RAS}$ = $\overline{CS}$ = V_{CC} − 0.2V)		I_{CC5}	—	1	mA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{RC} = min.)	KM44C268C-6	I_{CC6}	—	70	mA
	KM44C268C-7		—	65	mA
	KM44C268C-8		—	60	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test = 0V)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. I_{CC1}, I_{CC3} Address can be changed maximum two times while $\overline{RAS}$ = V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CAS}$ = V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_8, D)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	KM44C268C-6		KM44C268C-7		KM44C268C-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		175		195		ns	
Static column mode cycle time	t_{SC}	35		40		45		ns	
Static column mode read-write cycle time	t_{SRWC}	90		100		110		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
Access time from last write	t_{ALW}		60		65		75	ns	3,12
$\overline{CS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Output data hold time from column address	t_{AOH}	5		5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		25		25		25	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width (static column mode)	t_{RASC}	60	100,000	70	100,000	80	100,000	ns	
$\overline{CS}$ to $\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{RAS}$ to $\overline{CS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CS}$ pulse width	t_{CS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	15	100,000	20	100,000	20	100,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
$\overline{CS}$ precharge time (CBR mode)	t_{CPN}	10		10		10		ns	
$\overline{CS}$ precharge time (static column mode)	t_{CP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Write address hold time referenced to $\overline{RAS}$	t_{AWR}	50		55		60		ns	6
Column address hold referenced to $\overline{RAS}$	t_{AR}	70		80		90		ns	

AC CHARACTERISTICS (Continued)

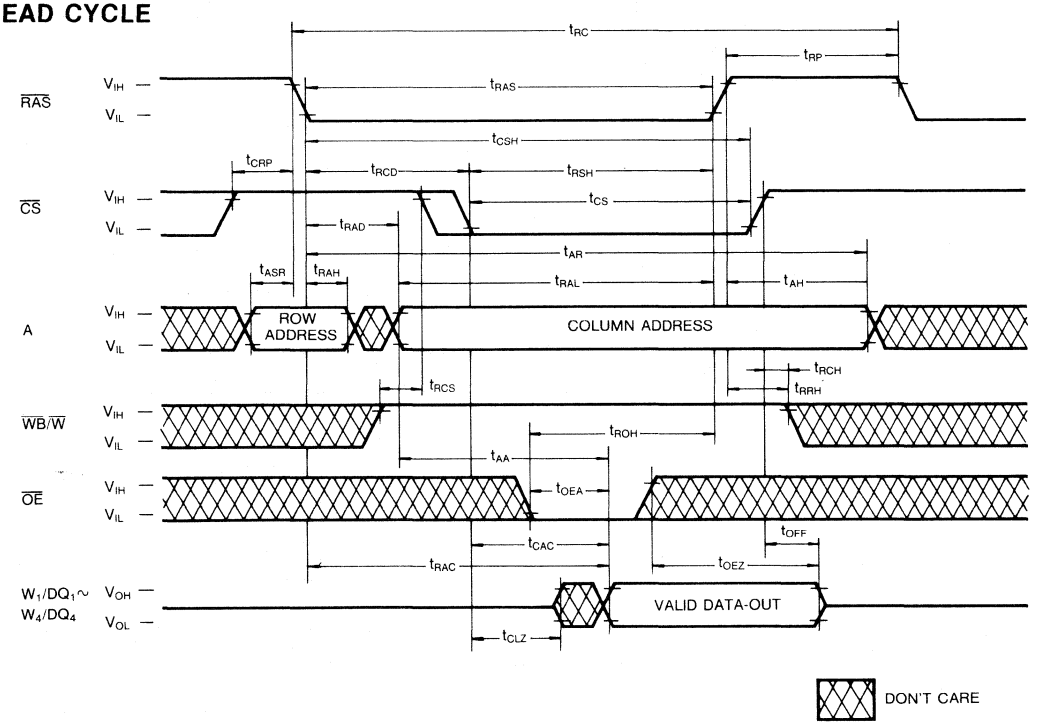
Parameter	Symbol	KM44C268C-6		KM44C268C-7		KM44C268C-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Column address hold time referenced to $\overline{RAS}$ rise	t_{AH}	5		5		5		ns	
Last write to column address delay time	t_{LWAD}	20	30	20	35	20	40	ns	12
Last write to column address hold time	t_{AHLW}	60		70		80		ns	
Read command set-up time referenced to $\overline{CS}$	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	50		55		60		ns	6
Write command pulse width	t_{WP}	15		15		15		ns	
Write command inactive time	t_{WI}	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		15		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	15		15		15		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (512 cycles)	t_{REF}		8		8		8	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CS}$ to $\overline{W}$ delay time (read modify write cycle)	t_{CWD}	40		45		45		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time (read modify write cycle)	t_{RWD}	85		95		105		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		60		65		ns	8
$\overline{CS}$ setup time ($\overline{CS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	5		5		5		ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh cycle)	t_{CHR}	15		15		15		ns	
$\overline{RAS}$ to $\overline{CS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CS}$ precharge time ($\overline{CS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	20		25		30		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	15		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	15		15		15		ns	
Write per bit set-up time	t_{WBS}	0		0		0		ns	
Write per bit hold time	t_{WBH}	10		10		15		ns	
Write per bit selection set-up time	t_{WDS}	0		0		0		ns	
Write per bit selection hold time	t_{WDH}	10		10		15		ns	

NOTES (Continued)

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. **t_{AWR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.**
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. Operation within the $t_{LWAD(max)}$ limit Insures that $t_{ALW(max)}$ can be met. $t_{LWAD(max)}$ is specified as a reference point only. If t_{LWAD} is greater than the specified $t_{LWAD(max)}$ limit, then access time is controlled by t_{AA}.

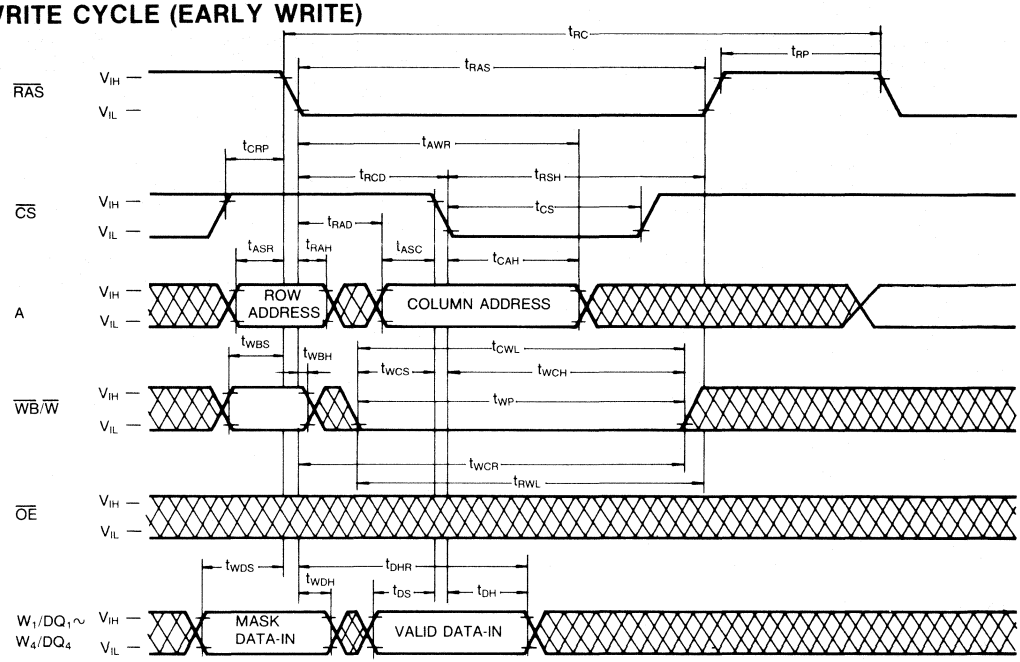
TIMING DIAGRAMS

READ CYCLE

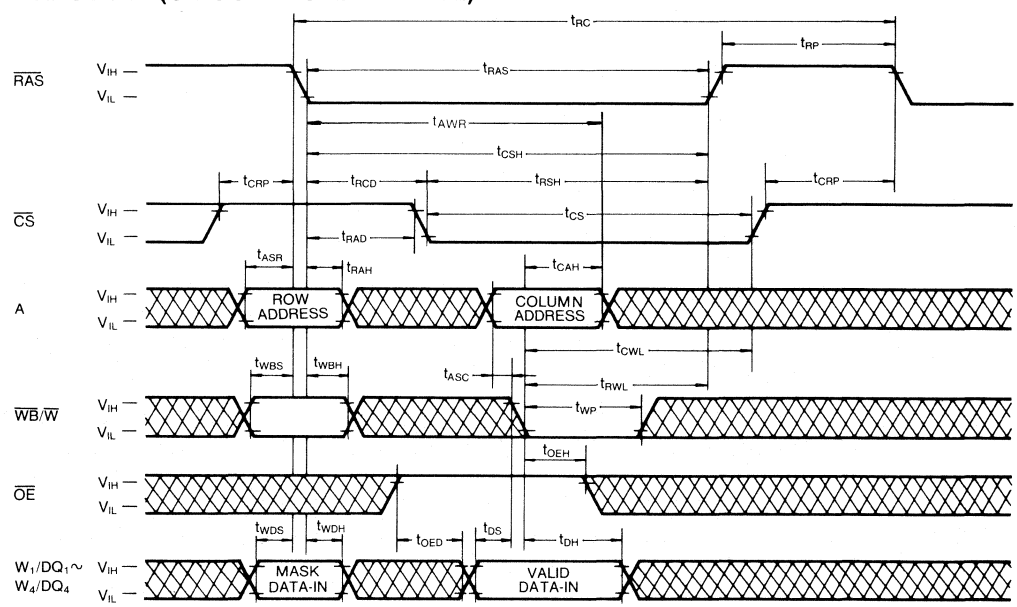


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

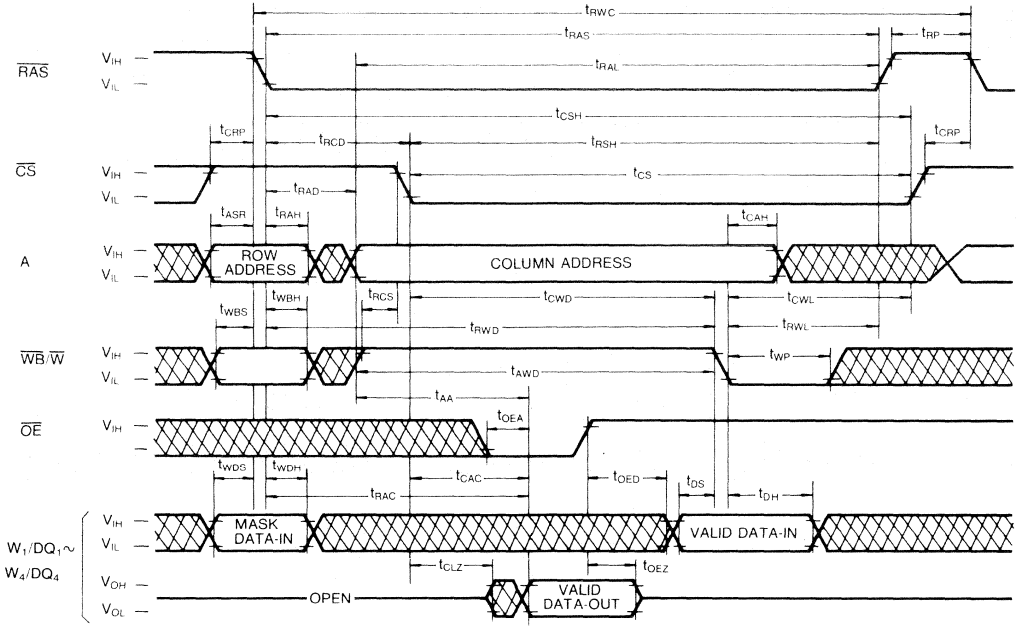


WRITE CYCLE (OE CONTROLLED WRITE)

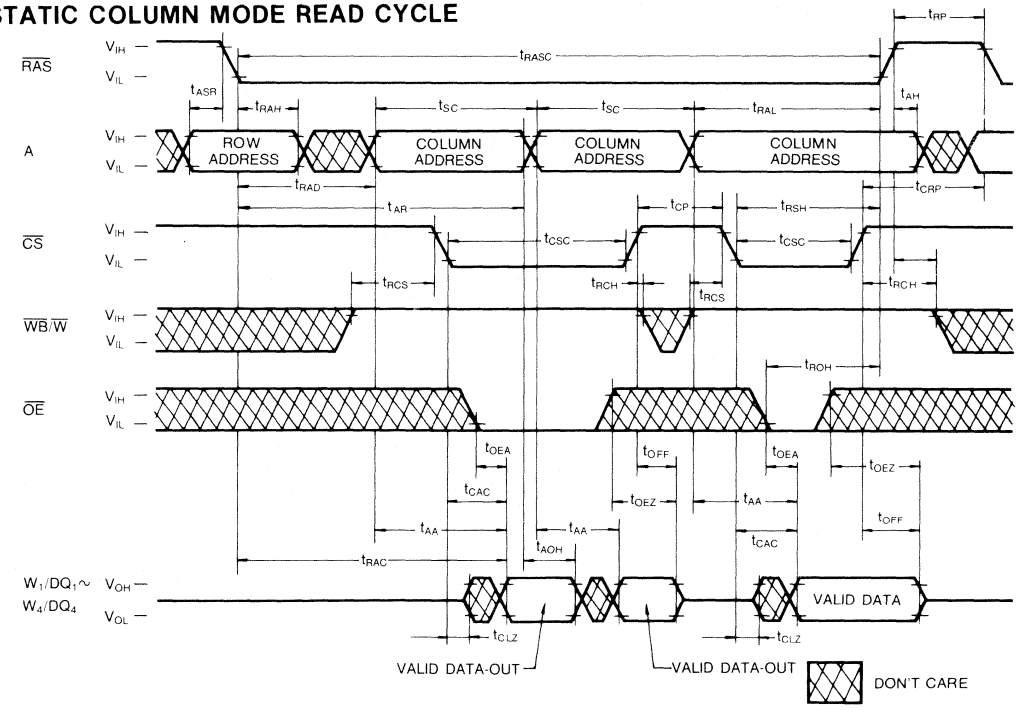


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITY CYCLE

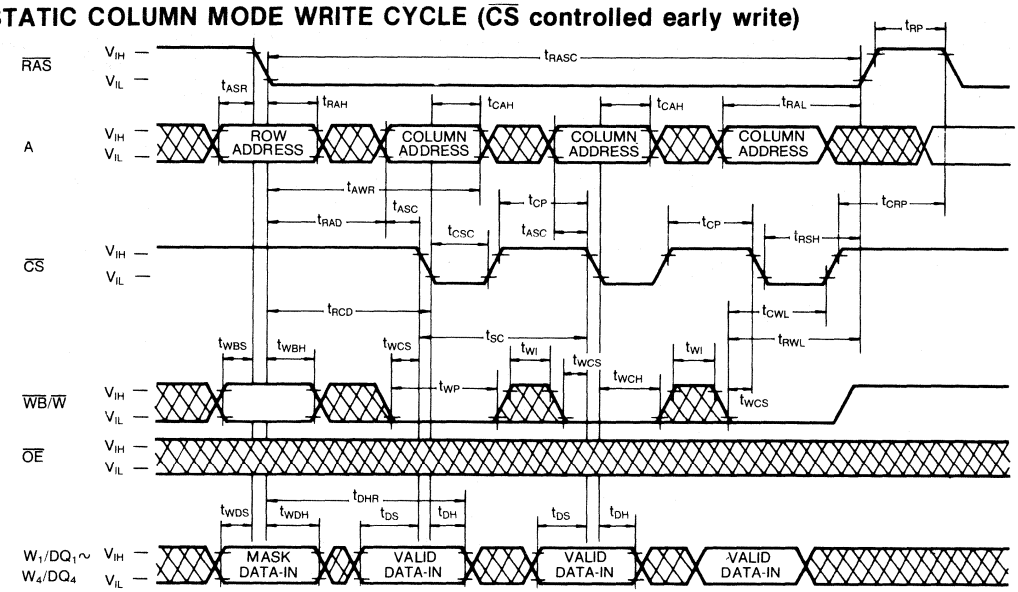


STATIC COLUMN MODE READ CYCLE

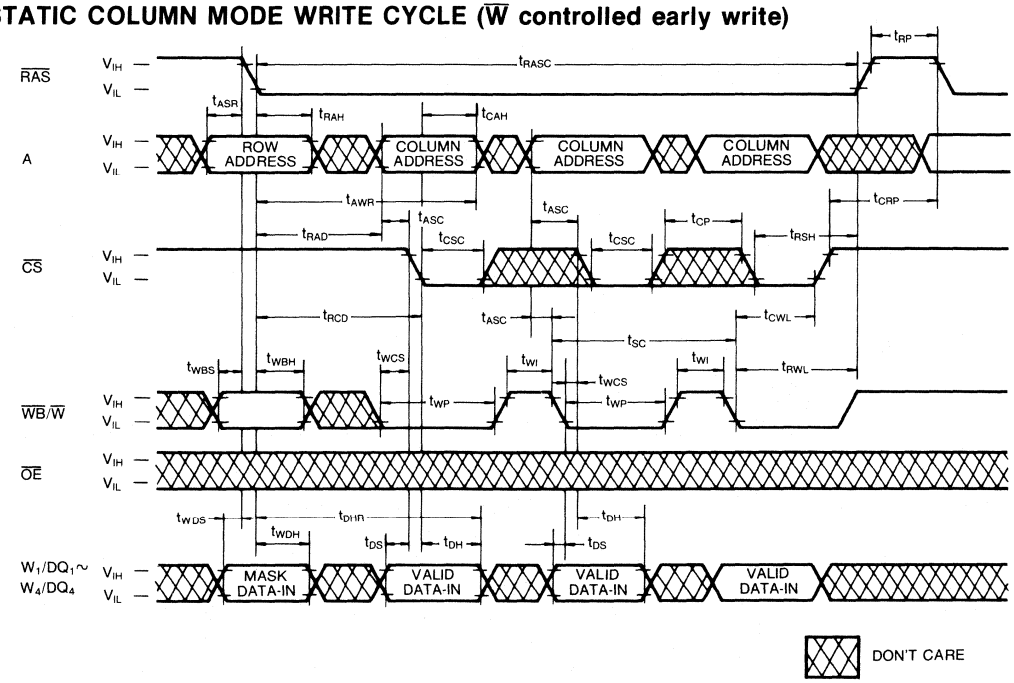


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ controlled early write)

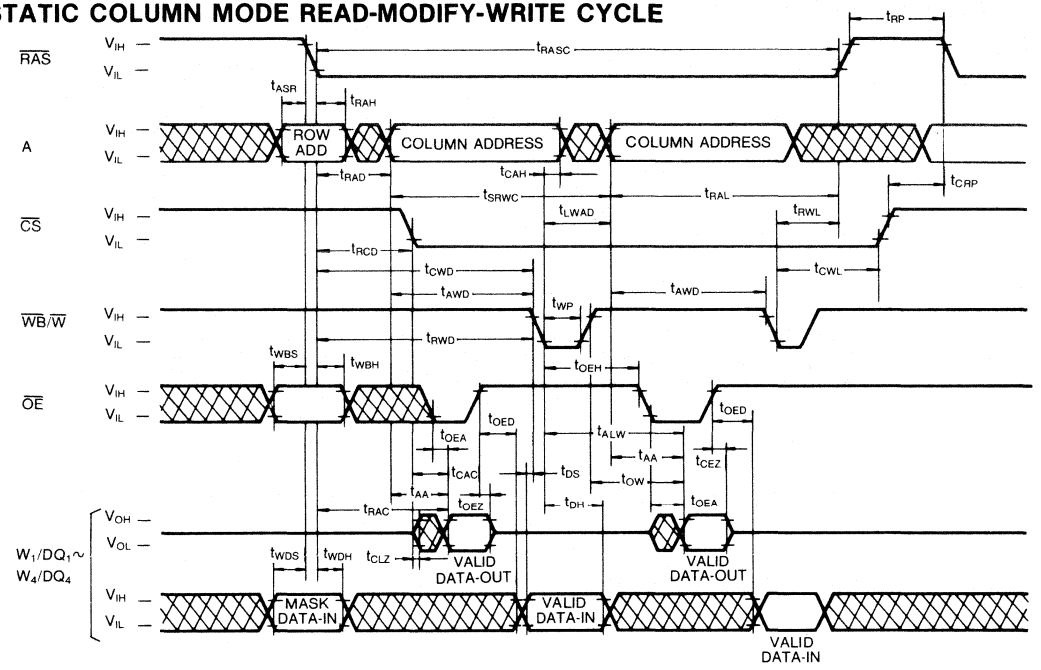


STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ controlled early write)

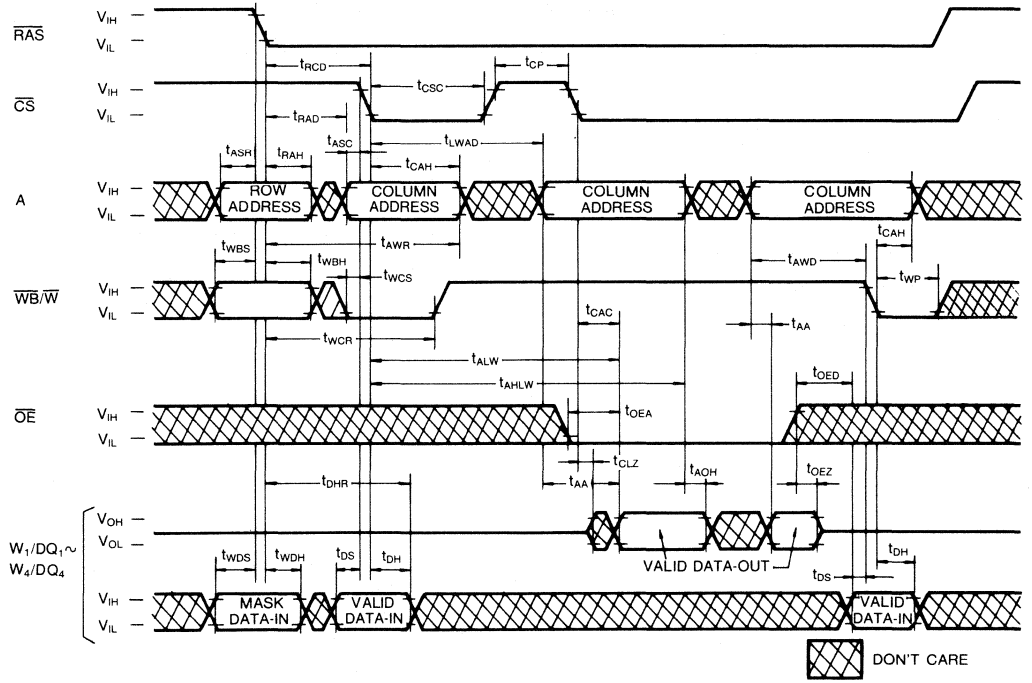


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



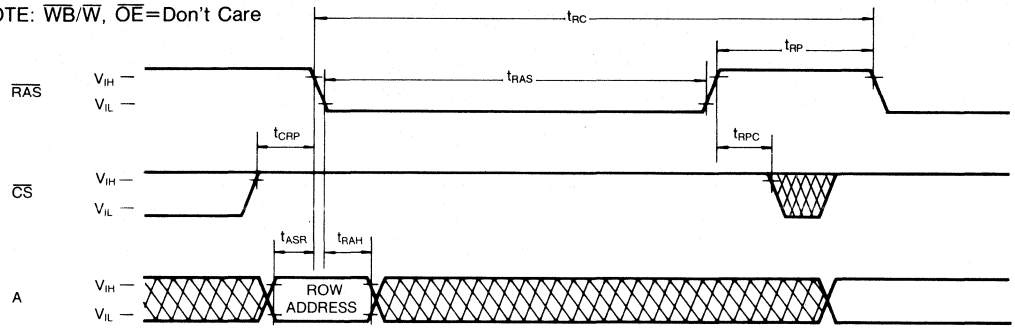
STATIC COLUMN MODE MIXED CYCLE



TIMING DIAGRAMS (Continued)

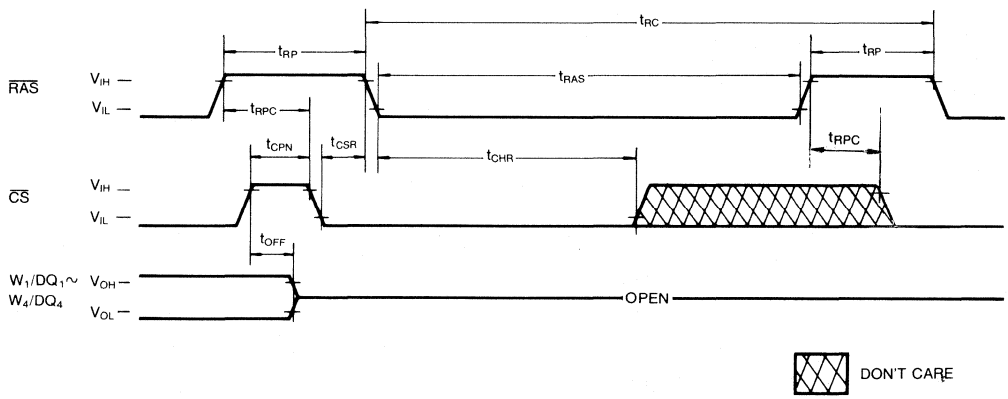
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{WB}/\overline{W}$, $\overline{OE}$=Don't Care



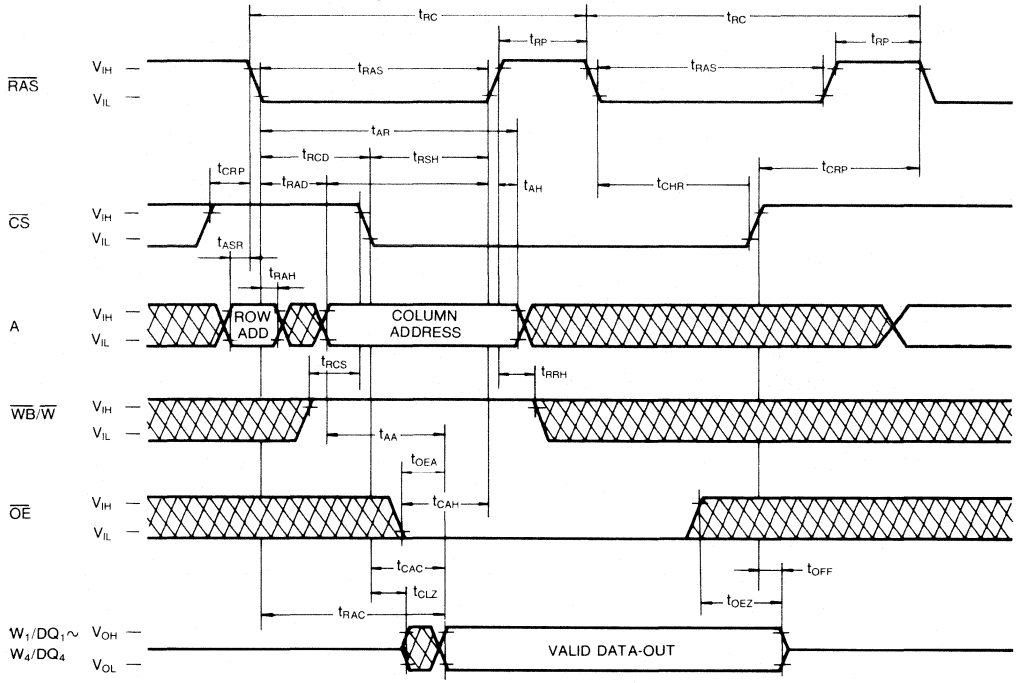
$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{WB}/\overline{W}$, $\overline{OE}$, A=Don't Care

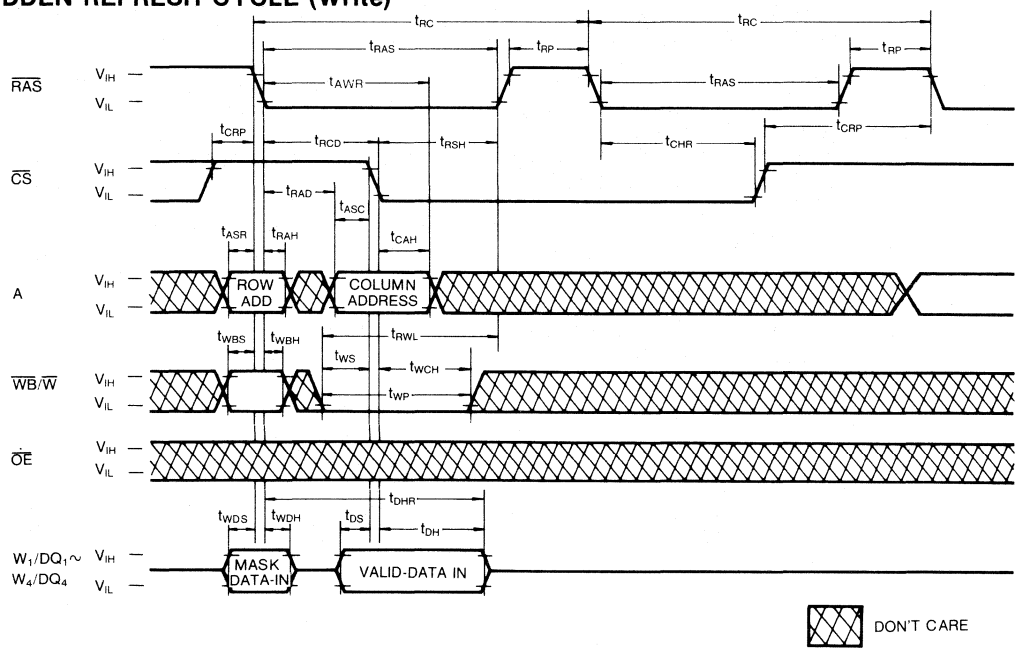


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (Read)

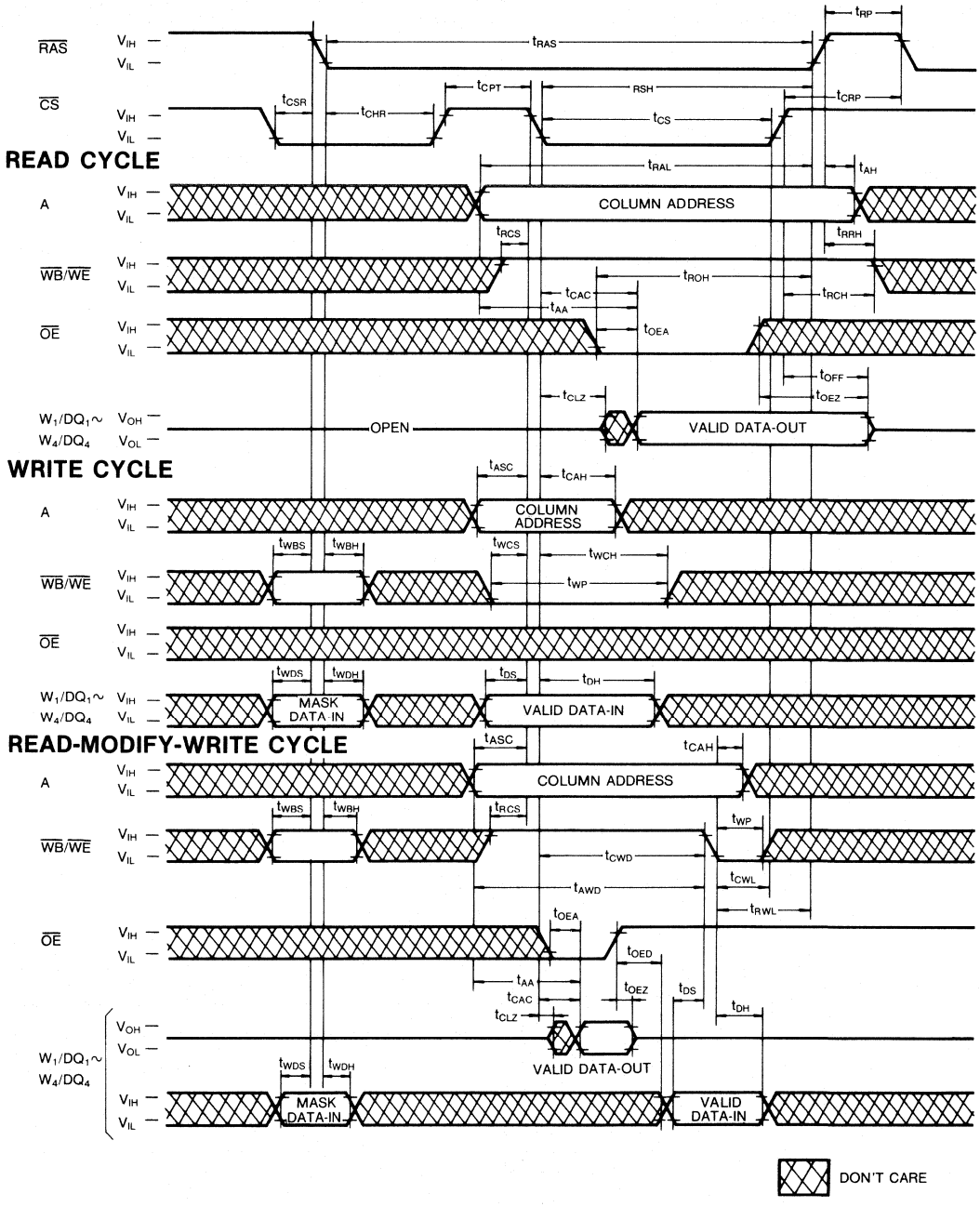


HIDDEN REFRESH CYCLE (Write)



TIMING DIAGRAMS (Continued)

$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM44C268C contains 1,048,576 memory locations organized as 262,144 four-bit words. Eighteen address bits are required to address a particular 4-bit word in the memory array. Since the KM44C268C has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CS}$) and the valid address inputs.

Operation of the KM44C268C begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CS}$. This is the beginning of any KM44C268C cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths are specified by $t_{RAS(min)}$ and $t_{CAS(min)}$ respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C268C begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CS}$ and on the valid column address transition.

If $\overline{CS}$ goes low before $t_{RCD(max)}$ and if the column address is valid before $t_{RAD(max)}$ then the access time to valid data is specified by $t_{RAC(min)}$. However, if $\overline{CS}$ goes low after $t_{RAD(max)}$, access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, $t_{RAC(min)}$, it is necessary to meet both $t_{RCD(max)}$ and $t_{RAD(max)}$.

The KM44C268C has common data I/O pins. For this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44C268C can perform early write, $\overline{OE}$ controlled write and read-modify-write cycles. Each of these write cycles is achieved by maintaing the write perbit/write enable ($\overline{WB}/\overline{W}$) input high at the falling edge of $\overline{RAS}$. If write-per-bit function is performed, $\overline{WB}/\overline{W}$ is kept low of the falling edge of $\overline{RAS}$. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of W or $\overline{CS}$ whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain the he Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CS}$ and meeting the data sheet read-modify-write timing requirements. This output enable input ($\overline{OE}$) must be low during the time defined by $t_{OEA}$and t_{OEZ} for data to appear at the outputs. If $t_{CWD}$and $t_{RWD}$are not met the output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM44C268C 's DQ pins.

Write-Per-Bit

Write-per-bit function is performed in the write cycle, that is early write, $\overline{OE}$ controlled write, read-modify-write. Write-per-bit makes it possible selectively to write one or more of the four I/O pins. To perform write-per-bit function at the falling edge of $\overline{RAS}$ the write-per-bit/write enable ($\overline{WB}/\overline{W}$) is kept low and at the same time Mask data of input pins to write among 4 I/O pins must be in high. If I/O pins that Mask data is kept low, write operation is inhibited.

Data Output

The KM44C268C has a three state output buffer which are controlled by $\overline{CS}$ and $\overline{OE}$. When either $\overline{CS}$ or $\overline{OE}$ is high (V_{IH}) the output are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} sepcify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden

DEVICE OPERATION (Continued)

refresh). Each of the KM44C268C operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast page Mode Read, Static Column Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Static Column Mode Write, $\overline{CS}$ only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} are not met)

Refresh

The data in the KM44C268C is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 8 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CS}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A_0-A_8).

$\overline{CS}$-before-$\overline{RAS}$ Refresh: The KM44C268C has $\overline{CS}$ before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh address. If $\overline{CS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CS}$ active time and cycling $\overline{RAS}$. The KM44C268C hidden refresh cycle is actually a $\overline{CS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C268C by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CS}$-before-$\overline{RAS}$ refresh is the preferred method.

$\overline{CS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CS}$-before-$\overline{RAS}$ refresh activated circuity. The cycle begins as a $\overline{CS}$ before-$\overline{RAS}$ refresh operation. Then, if $\overline{CS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A_0 through A_8 are supplied by the on-chip refresh counter. The A_9 bit is set low internally.

Static Column Mode

Static column mode allows high speed read, write or read-modify-write random access to all the memory cells within a selected row. Operation within a selected row is similar to a static RAM.

A static column mode read cycle starts as a normal cycle. Additional cells within the selected row are read by applying a new column address while $\overline{W}=V_{IH}$ and $\overline{RAS}=V_{IL}$.

A static column mode write cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{RAS}=V_{IL}$ and toggling either $\overline{W}$ or $\overline{CS}$. The data is written into teh cell triggered by the latter falling edge of $\overline{W}$ or $\overline{CS}$.

Power-up

If $\overline{RAS}=V_{SS}$ during power-up, the KM44C268C could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up courrent.
An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C268C inputs act like unterminated transmission lines resulting in significant positive and negative overshoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to

DEVICE OPERATION (Continued)

the KM44C268C input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. the recommended methods are gridded power and ground lines orseparate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with may DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM44C268C using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C268C and they supply much of the current used by the KM44C268C during cycling.

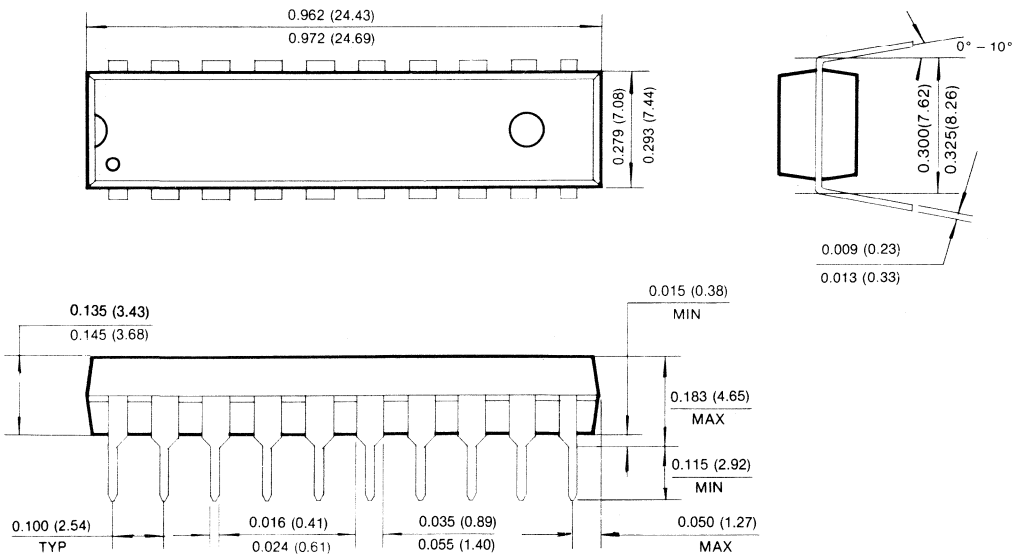
In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

2

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

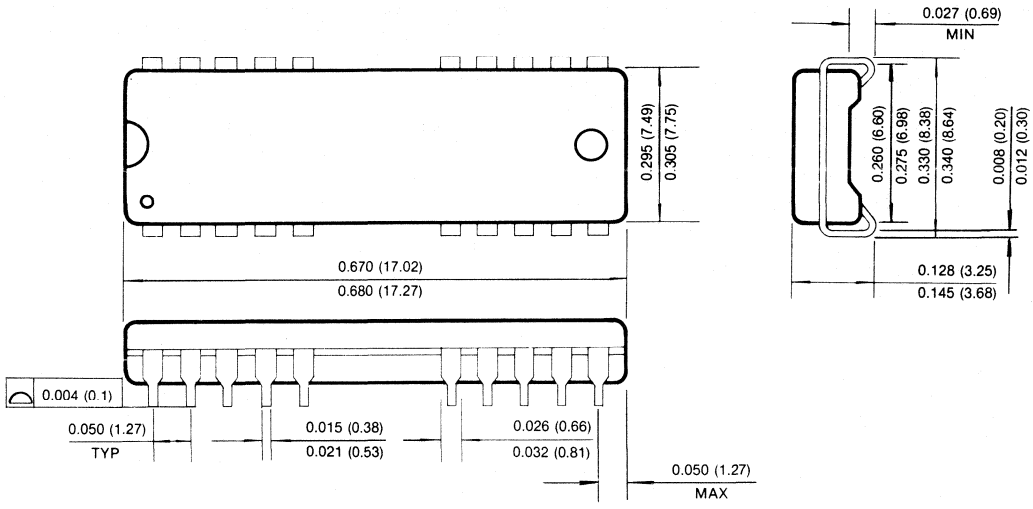
Units: Inches (Millimeters)



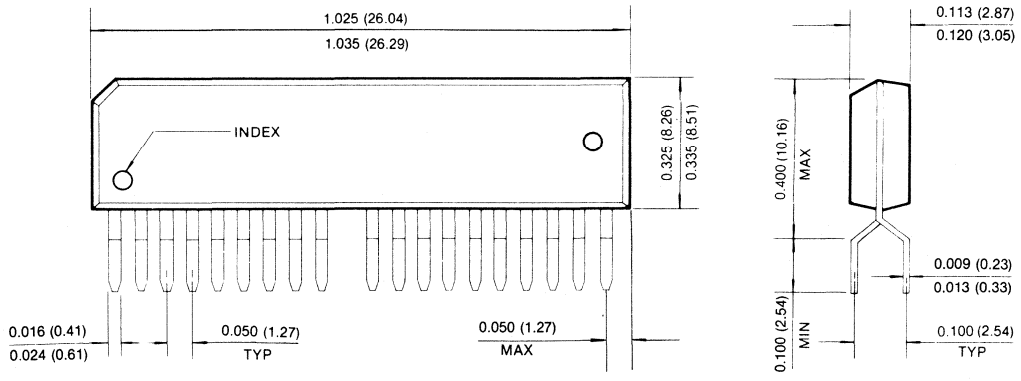
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



4MX1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C4000A- 7	70ns	20ns	130ns
KM41C4000A- 8	80ns	20ns	150ns
KM41C4000A-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8-bit fast parallel test mode capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Write**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, DIP, ZIP**

GENERAL DESCRIPTION

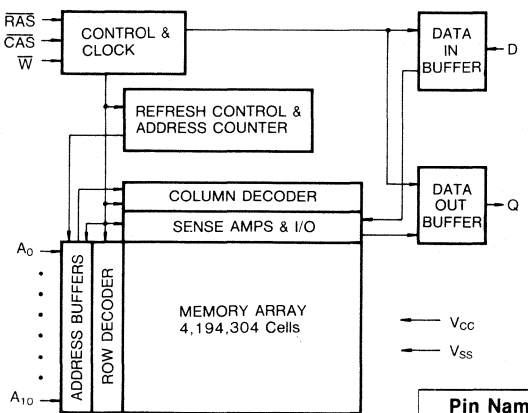
The Samsung KM41C4000A is a high speed CMOS 4,194,304 bit X 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C4000A features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

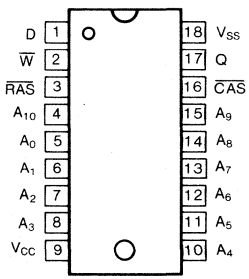
The KM41C4000A is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

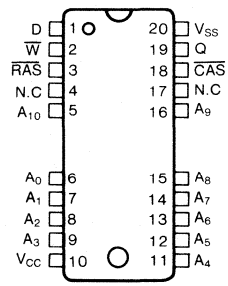


PIN CONFIGURATION (Top Views)

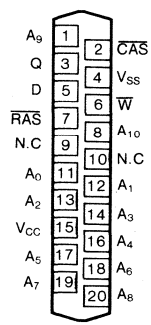
- **KM41C4000AP**



- **KM41C4000AJ**



- **KM41C4000AZ**



Pin Name	Pin Function
A0-A10	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, V_{CC}=5.0V±10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM41C4000A- 7	I_{CC1}	—	105	mA
	KM41C4000A- 8		—	95	mA
	KM41C4000A-10		—	85	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min.)	KM41C4000A- 7	I_{CC3}	—	105	mA
	KM41C4000A- 8		—	95	mA
	KM41C4000A-10		—	85	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling @ t_{PC}=min.)	KM41C4000A- 7	I_{CC4}	—	80	mA
	KM41C4000A- 8		—	70	mA
	KM41C4000A-10		—	60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$≥V_{CC}-0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM41C4000A- 7	I_{CC6}	—	105	mA
	KM41C4000A- 8		—	95	mA
	KM41C4000A-10		—	85	mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL}, Dout Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

* Note: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{10}, D)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM41C4000A-7		KM41C4000A-8		KM41C4000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	155		175		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	12
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	8
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	12
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	9

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM41C4000A-7		KM41C4000A-8		KM41C4000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		20		ns	9
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	12
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	7
$\overline{CAS}$ to write enable delay	t_{CWD}	20		20		25		ns	7
$\overline{RAS}$ to write enable delay	t_{RWD}	70		80		100		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		50		ns	7
$\overline{CAS}$ setup time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
FAst Page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	45		45		55		ns	
Fast page modered-modify-write	t_{PRWC}	75		75		90		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	

TEST MODE CYCLE

(Note. 11)

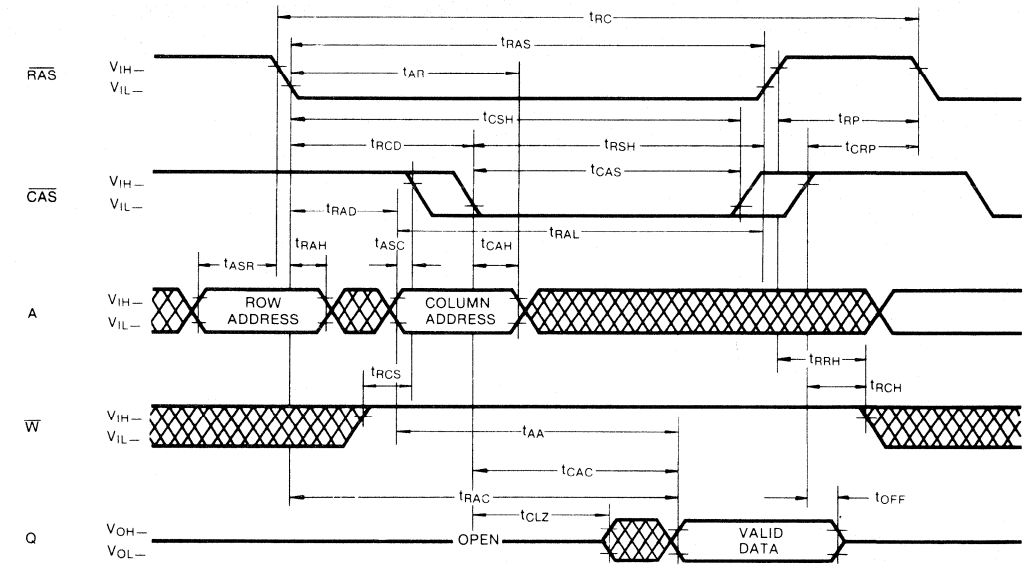
Standard Operation	Symbol	KM41C4000A-7		KM41C4000A-8		KM41C4000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	135		155		185		ns	
Read-modify-write cycle time	t_{RWC}	160		180		215		ns	
Access time from $\overline{RAS}$	t_{RAC}		75		85		105	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		25		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		45		55	ns	3,10
$\overline{RAS}$ pulse width	t_{RAS}	75	10,000	85	10,000	105	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{CAS}$ hold time	t_{CSH}	75		85		105		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		45		55		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	25		25		30		ns	7
$\overline{RAS}$ to write enable delay	t_{RWD}	75		85		105		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	40		45		55		ns	7
Fast mode cycle time	t_{PC}	55		55		65		ns	
Fast page mode read-modefy-write	t_{PRWC}	80		80		95		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	75	200,000	85	200,000	105	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		50		60	ns	3

NOTES

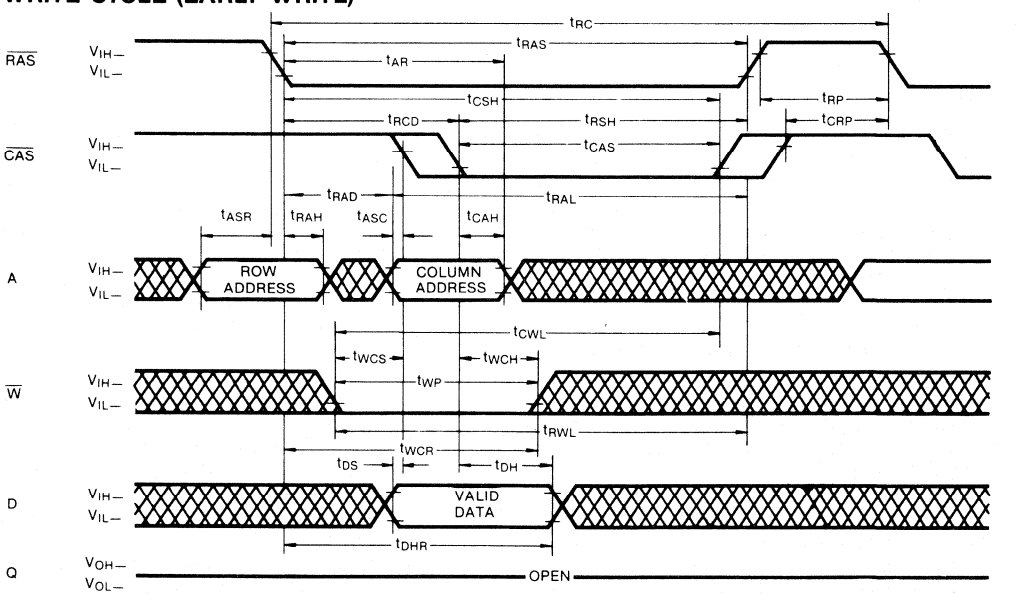
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
10. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
11. These specifications are applied in the test mode.
12. t_{AR}, t_{WCR}, t_{DHR} are refrerenced to $t_{RAD(max)}$.

TIMING DIAGRAMS

READ CYCLE



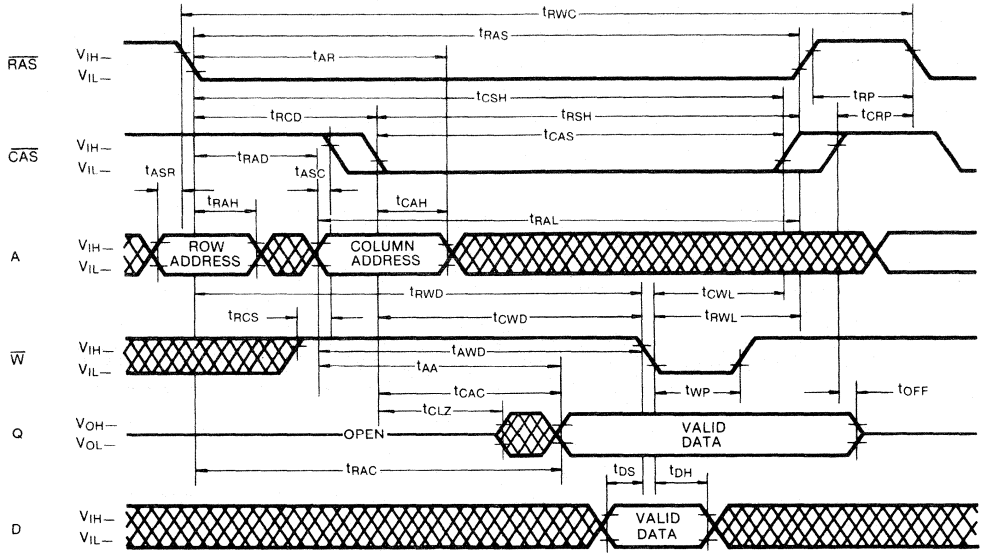
WRITE CYCLE (EARLY WRITE)



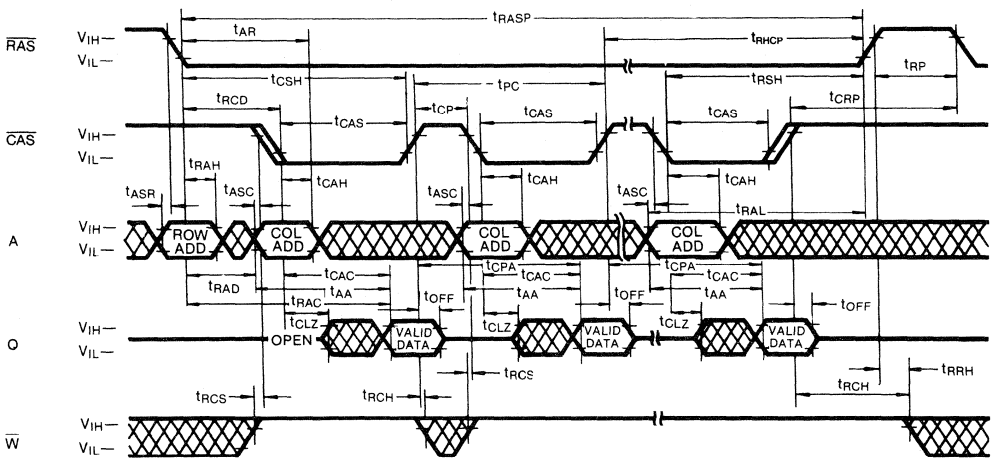
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



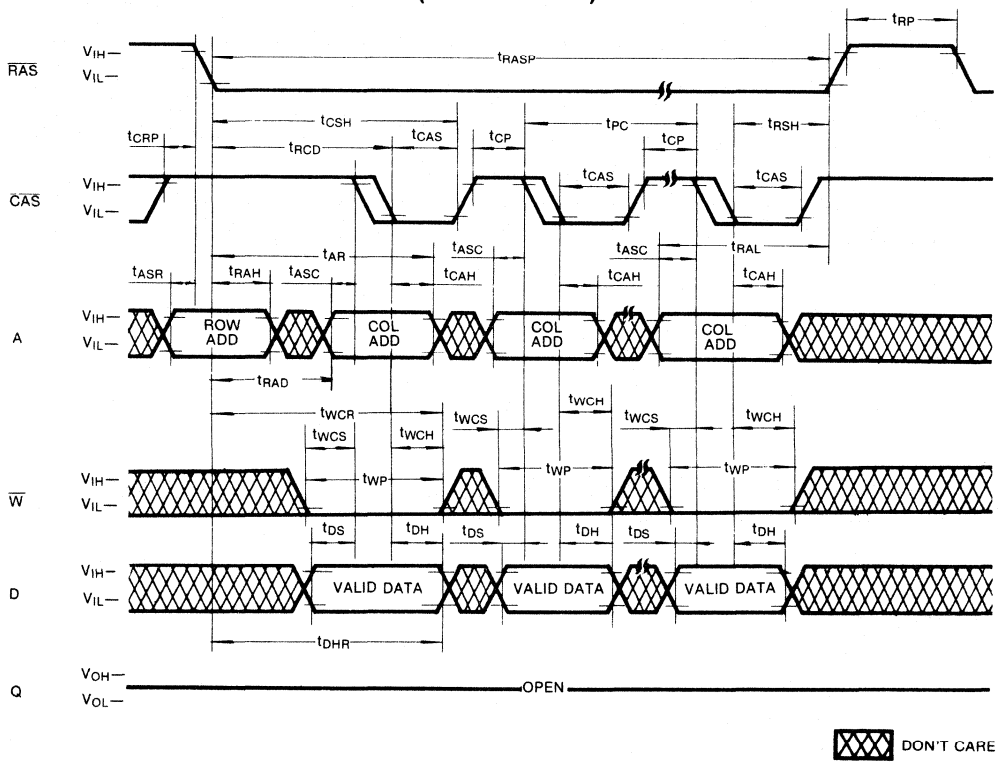
FAST PAGE MODE READ CYCLE



DON'T CARE

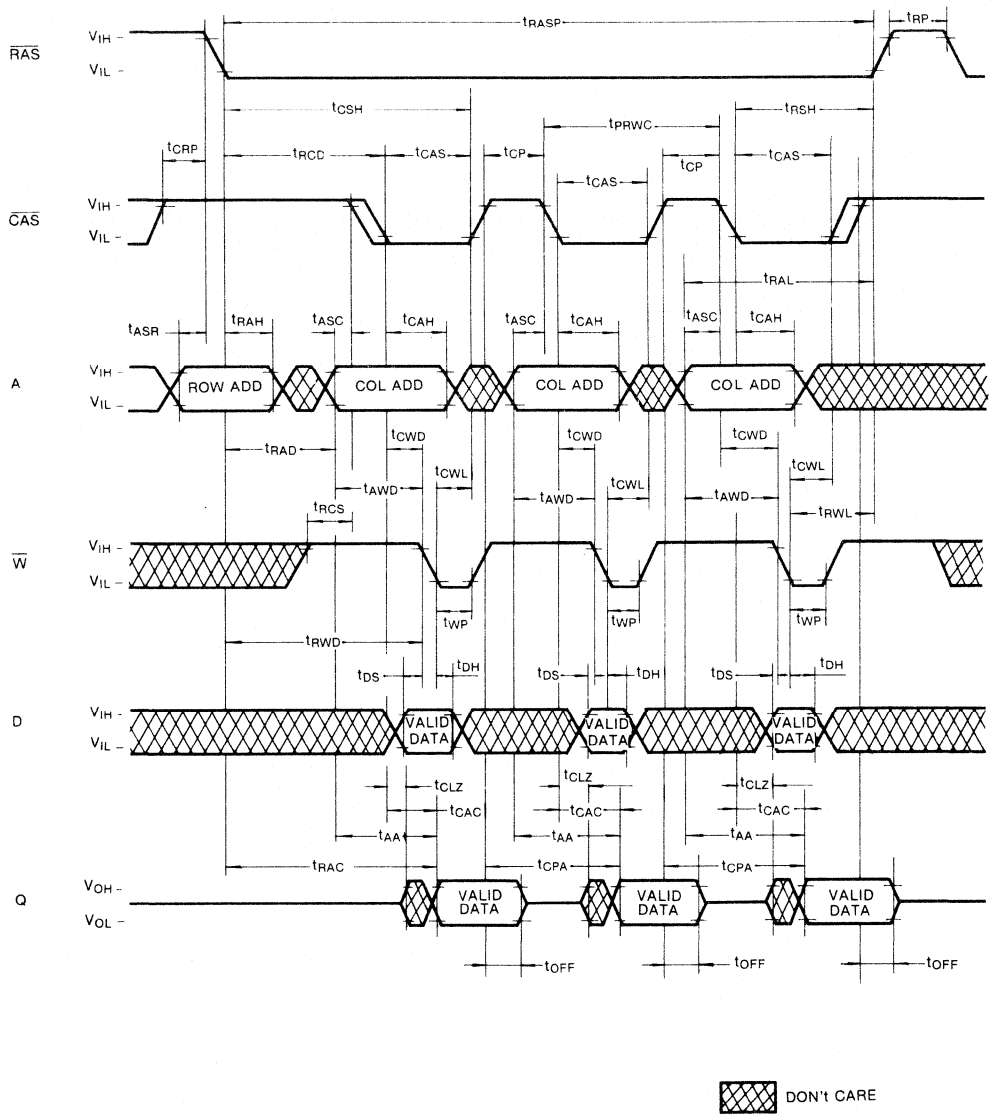
TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

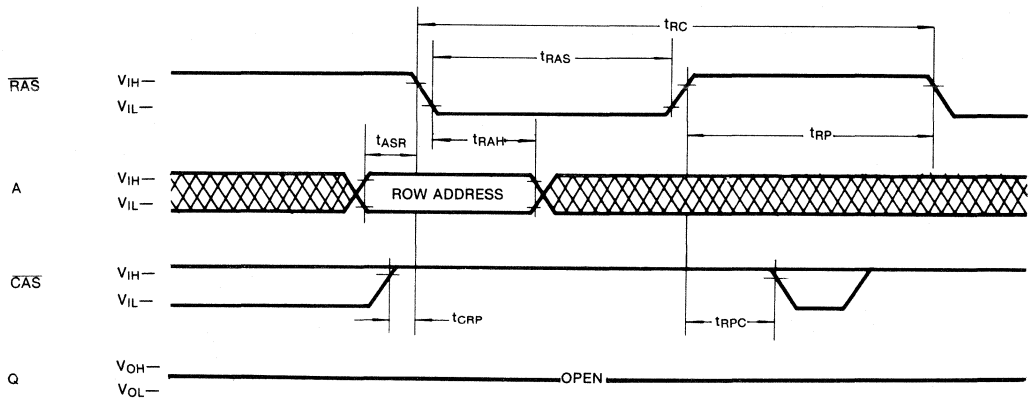
FAST PAGE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

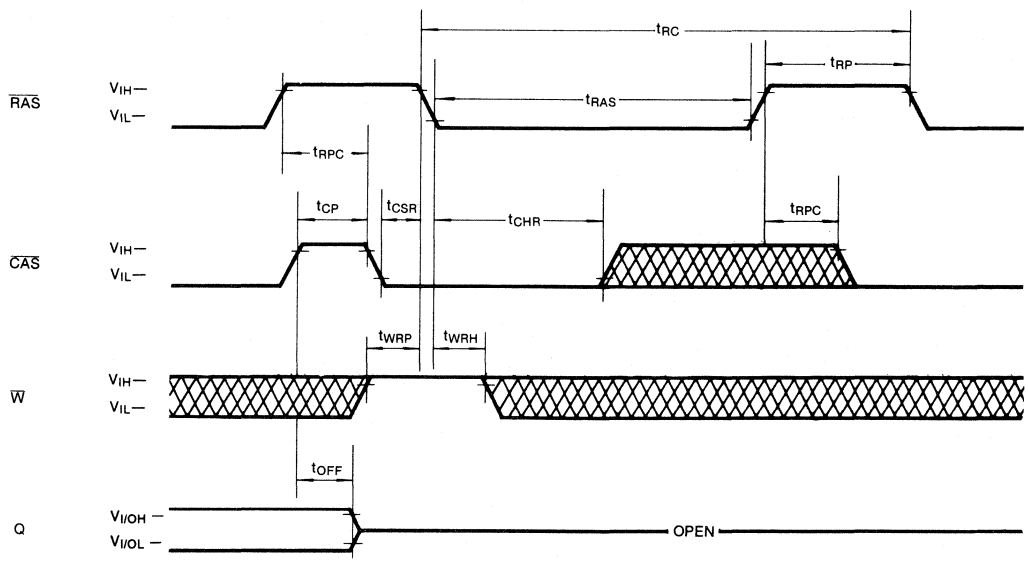
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, D, A_{10} = Don't Care



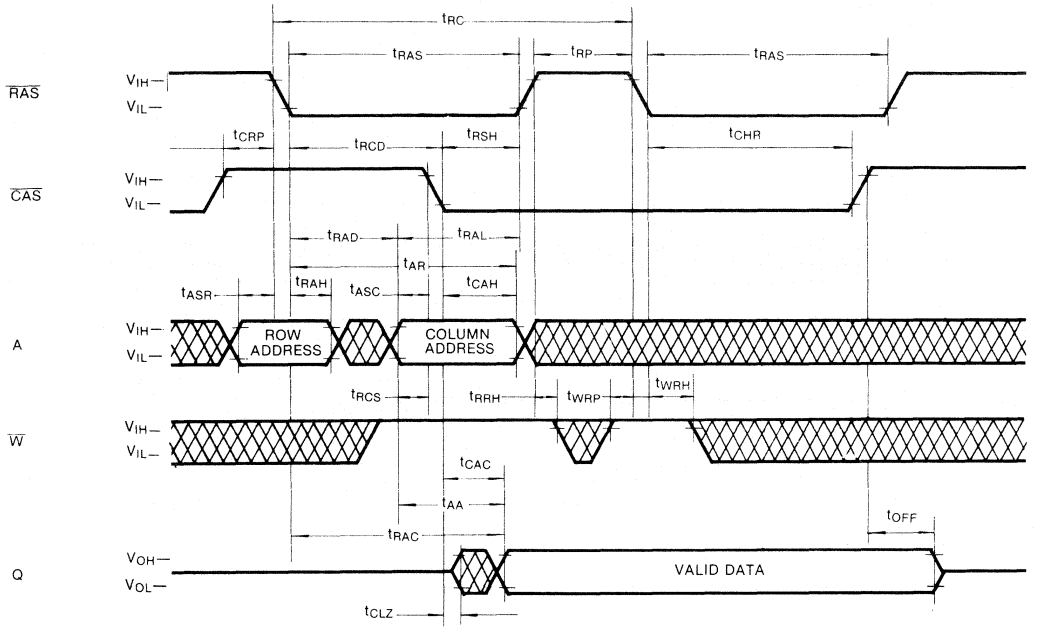
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address = Don't Care

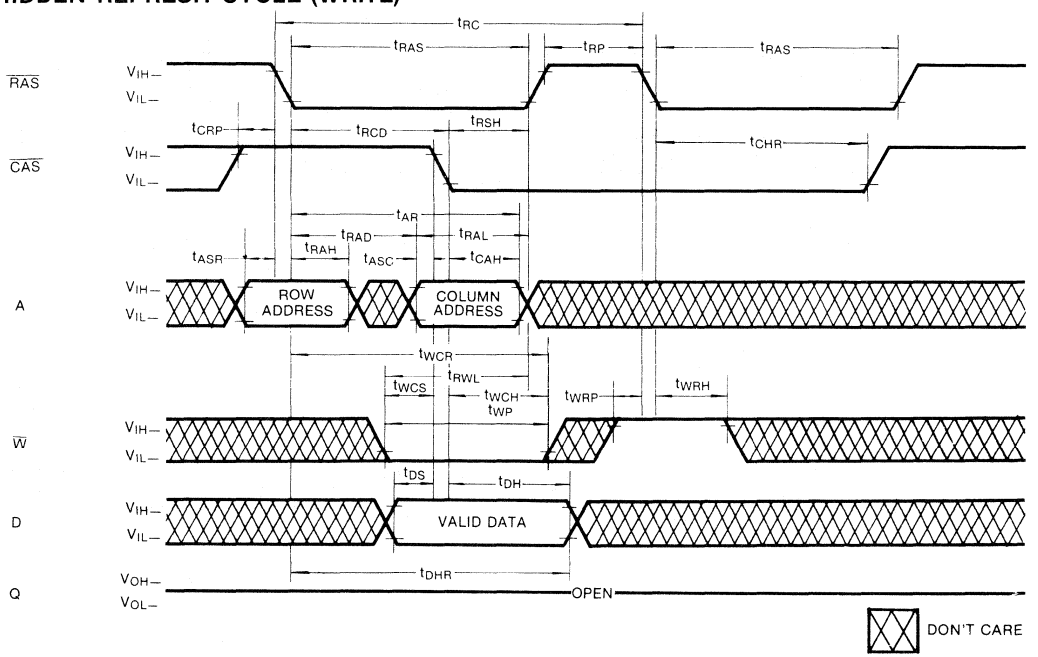


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

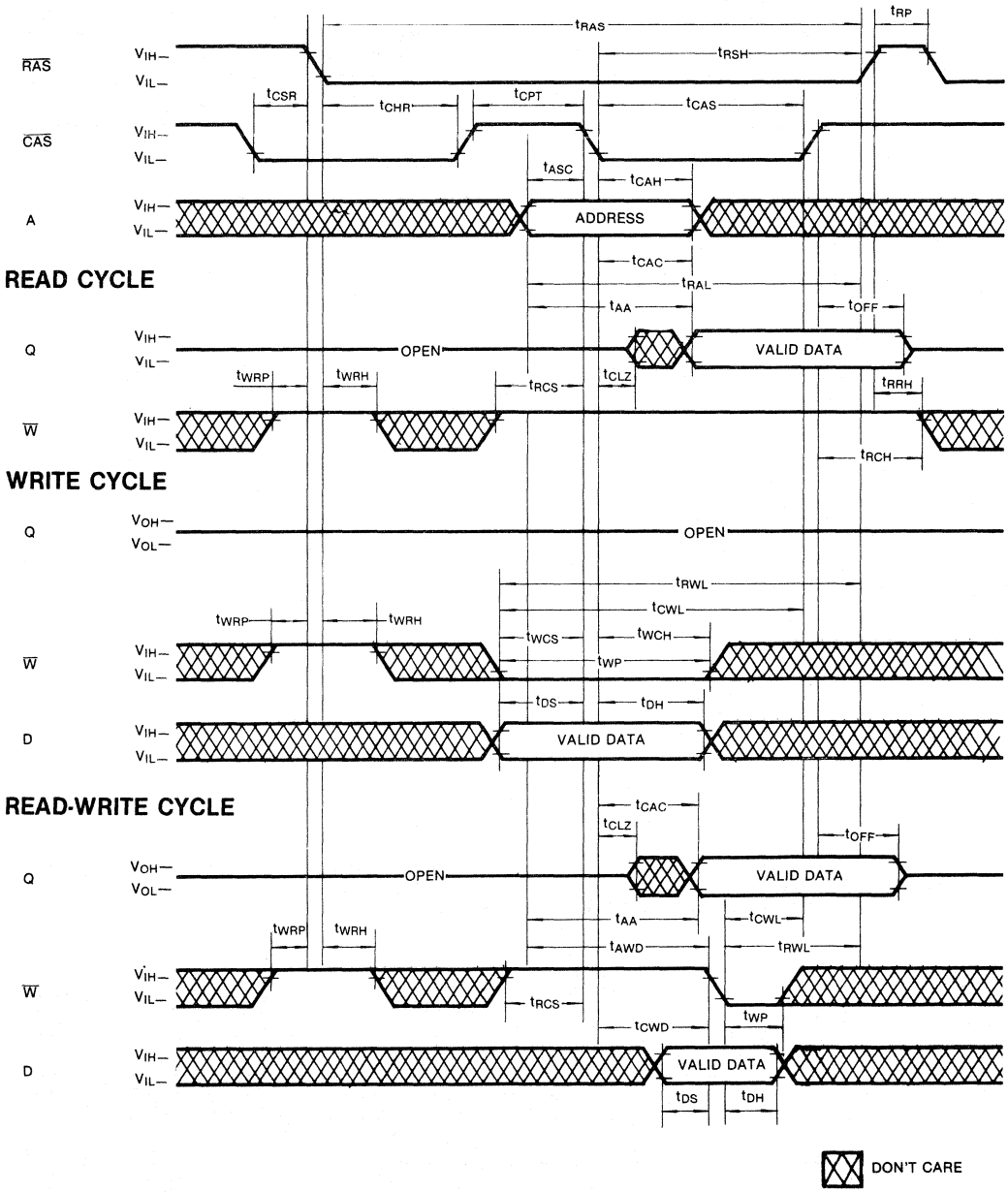


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

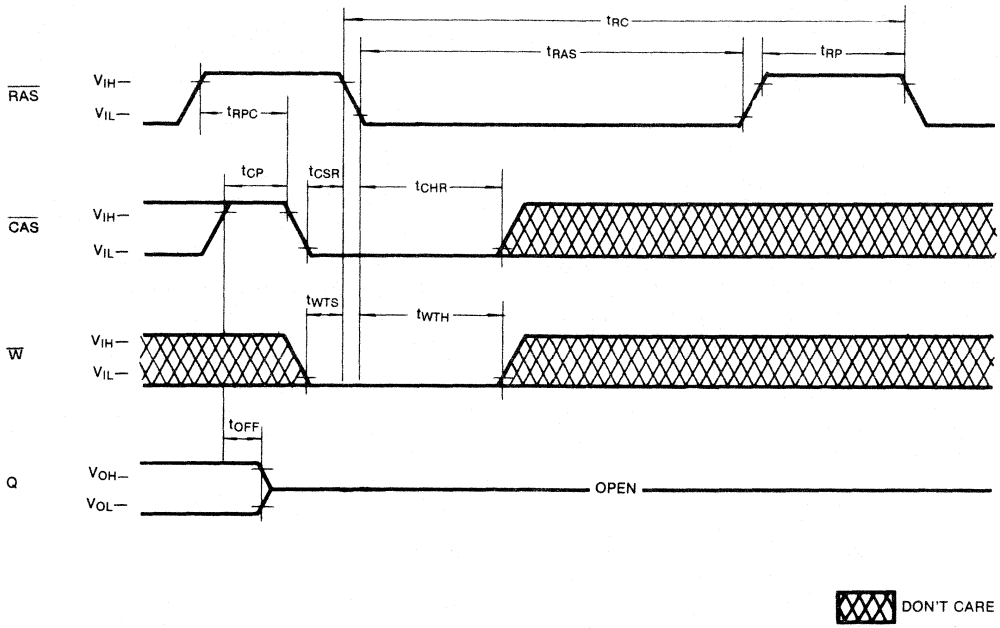
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address = Don't Care



TEST MODE DESCRIPTION

The KM41C4000A is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}. A_{10C} and A_{OC} are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0" In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM. $\overline{W}$, $\overline{CAS}$ Before $\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/8 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM41C4000A contains 4,194,304 memory locations. Twenty-two address bits are required to address a particular memory location. Since the KM41C4000A has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM41C4000A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C4000A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C4000A begin a complex sequence of events. If the sequence if broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41C4000A can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C4000A has a three-state output buffer which which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C4000A operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

DEVICE OPERATION (Continued)

Refresh

The data in the KM41C4000A is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C4000A has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuity is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C4000A hidden refresh cycle is actually a $\overline{CAS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C4000A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM41C4000A has Fast Page mode capability. Fast Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In Fast Page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A Fast Page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row address for the same page. Up to 2048 memory cells can be accessed with the same row address.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter. This A_{10} bit is set high internally.

Column Address—Bits A_0 through A_{10} are strobedin by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

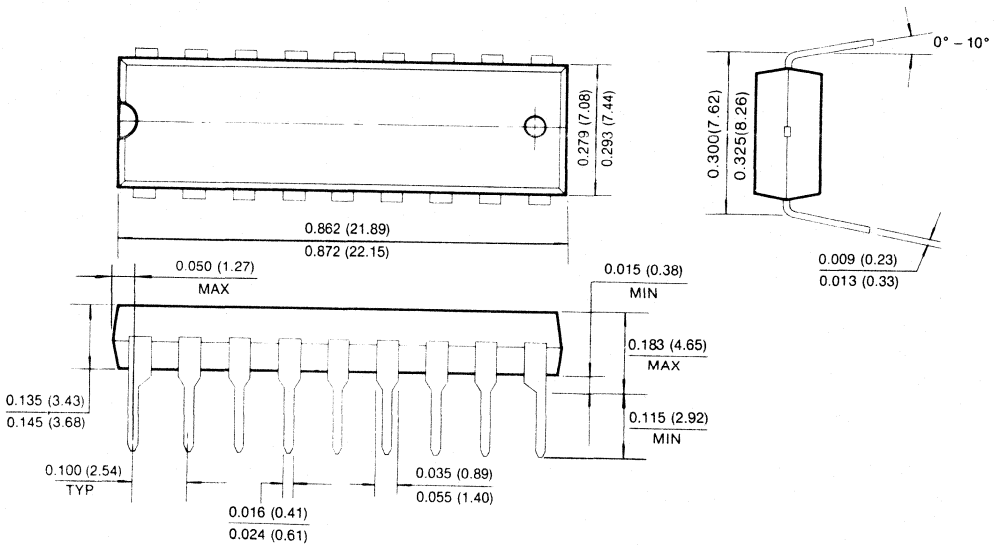
If $\overline{RAS}=V_{SS}$ during power-up, the KM41C4000A could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200μs is required after power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.

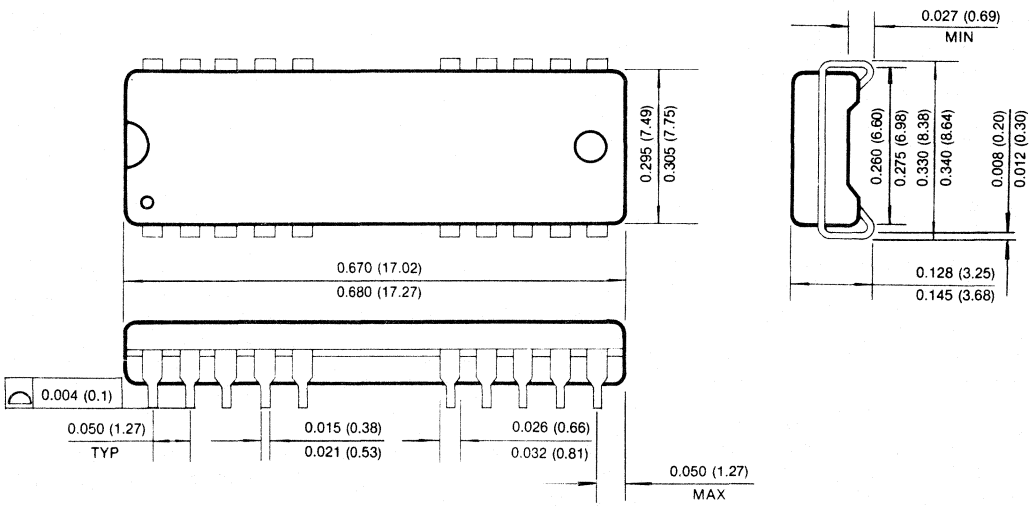
PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (Millimeters)



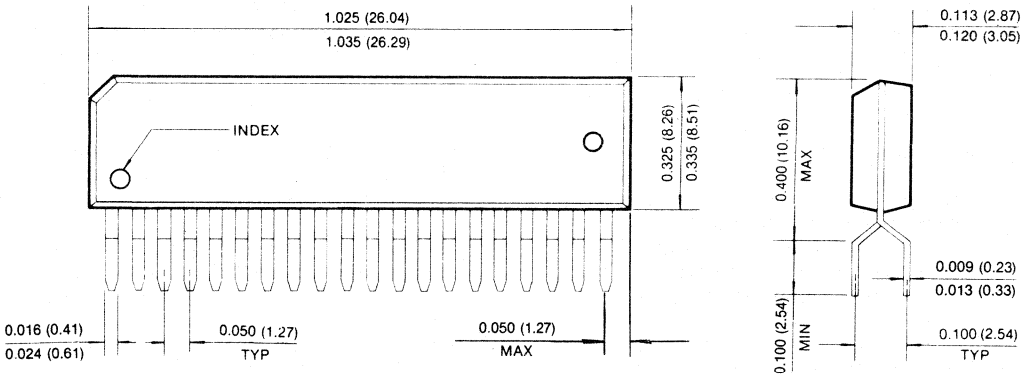
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)



4MX1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C4000AL- 7	70ns	20ns	130ns
KM41C4000AL- 8	80ns	20ns	150ns
KM41C4000AL-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8-bit fast parallel test mode capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Write**
- **Single +5V±10% power supply**
- **1024 cycles/128ms refresh**
- **Low power dissipation**
  - **—Standby: 1.1mW**
  - **—Active (70/80/100ns): 578/523/468mW**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, DIP, ZIP**

GENERAL DESCRIPTION

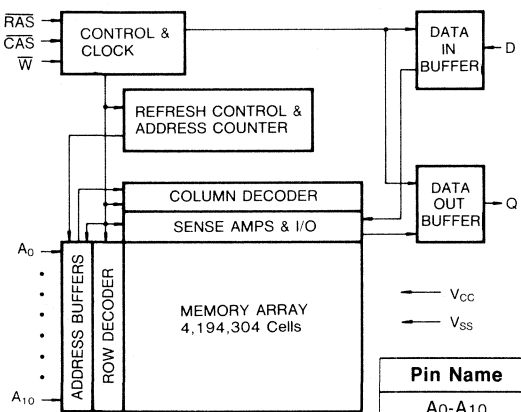
The Samsung KM41C4000AL is a high speed CMOS 4,194,304 bit X 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C4000AL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

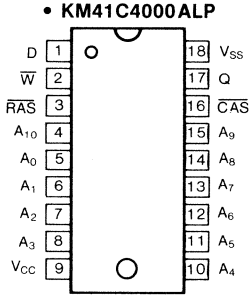
The KM41C4000AL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

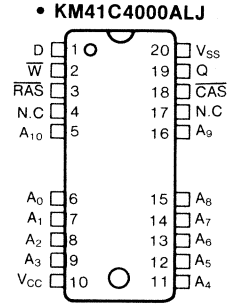


PIN CONFIGURATION (Top Views)

- **KM41C4000ALP**

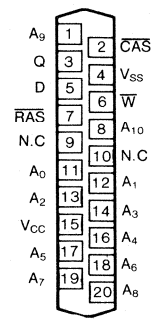


- **KM41C4000ALJ**



Pin Name	Pin Function
A0-A10	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

- **KM41C4000ALZ**



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, V_{CC}=5.0V±10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM41C4000AL- 7	I_{CC1}	—	105	mA
	KM41C4000AL- 8		—	95	mA
	KM41C4000AL-10		—	85	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min.)	KM41C4000AL- 7	I_{CC3}	—	105	mA
	KM41C4000AL- 8		—	95	mA
	KM41C4000AL-10		—	85	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling @ t_{PC}=min.)	KM41C4000AL- 7	I_{CC4}	—	80	mA
	KM41C4000AL- 8		—	70	mA
	KM41C4000AL-10		—	60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$≥V_{CC}−0.2V)		I_{CC5}	—	200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM41C4000AL- 7	I_{CC6}	—	105	mA
	KM41C4000AL- 8		—	95	mA
	KM41C4000AL-10		—	85	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{CC}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=125μS, T_{RAS}=t_{RAS} min.~1μS		I_{CC7}	—	300	μA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL}, Dout Enable)		I_{CC8}	—	5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*Note: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{10}, D)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM41C4000AL-7		KM41C4000AL-8		KM41C4000AL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	155		175		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	12
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	8
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	12
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	9

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM41C4000AL-7		KM41C4000AL-8		KM41C4000AL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		20		ns	9
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	12
Refresh period (1024 cycles)	t_{REF}		128		128		128	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	7
$\overline{CAS}$ to write enable delay	t_{CWD}	20		20		25		ns	7
$\overline{RAS}$ to write enable delay	t_{RWD}	70		80		100		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		50		ns	7
$\overline{CAS}$ setup time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
Fast Page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	45		45		55		ns	
Fast page modered-modify-write	t_{PRWC}	75		75		90		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	

TEST MODE CYCLE

(Note. 11)

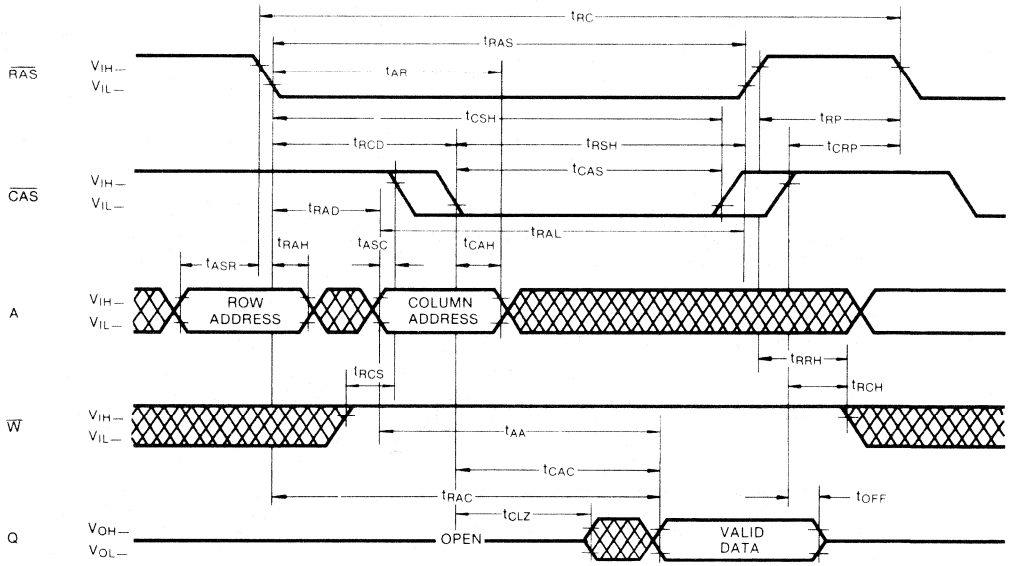
Standard Operation	Symbol	KM41C4000AL-7		KM41C4000AL-8		KM41C4000AL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	135		155		185		ns	
Read-modify-write cycle time	t_{RWC}	160		180		215		ns	
Access time from $\overline{RAS}$	t_{RAC}		75		85		105	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		25		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		45		55	ns	3,10
$\overline{RAS}$ pulse width	t_{RAS}	75	10,000	85	10,000	105	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{CAS}$ hold time	t_{CSH}	75		85		105		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		45		55		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	25		25		30		ns	7
$\overline{RAS}$ to write enable delay	$_{RWD}$	75		85		105		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	40		45		55		ns	7
Fast mode cycle time	t_{PC}	55		55		65		ns	
Fast page mode read-modefy-write	t_{PRWC}	80		80		95		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	75	200,000	85	200,000	105	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		50		60	ns	3

NOTES

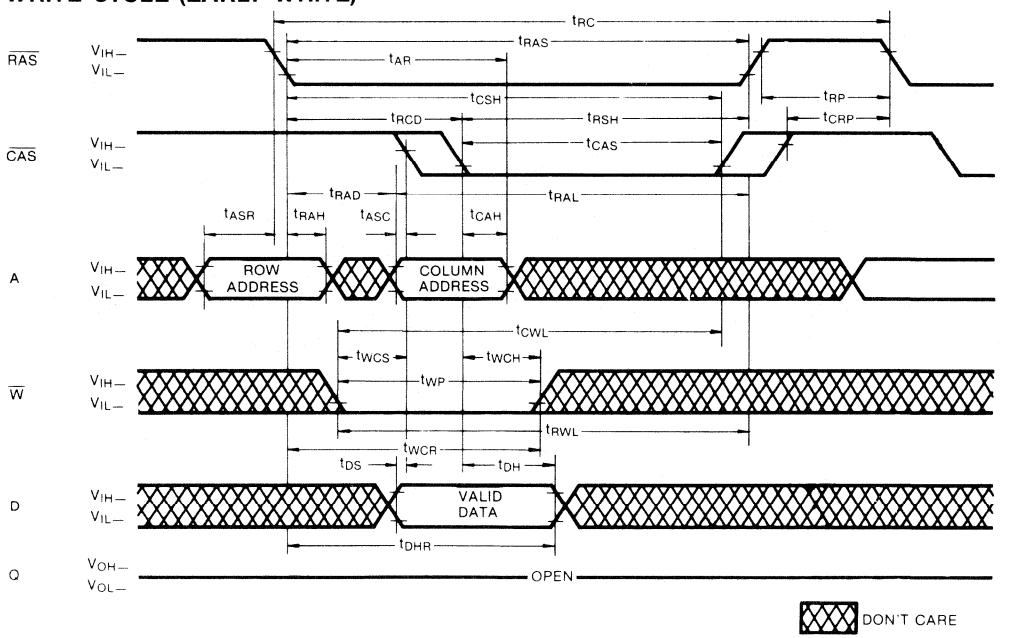
1. An initial pause of 200μs is required after power-up followed by and 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
10. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
11. These specifications are applied in the test mode.
12. t_{AR}, t_{WCR}, t_{DHR} are refrerenced to $t_{RAD(max)}$.

TIMING DIAGRAMS

READ CYCLE

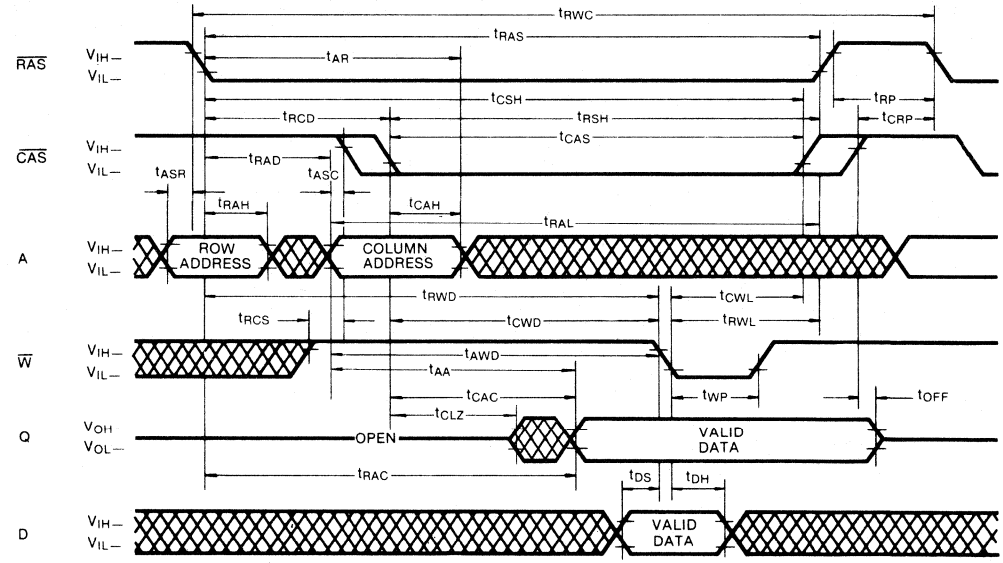


WRITE CYCLE (EARLY WRITE)

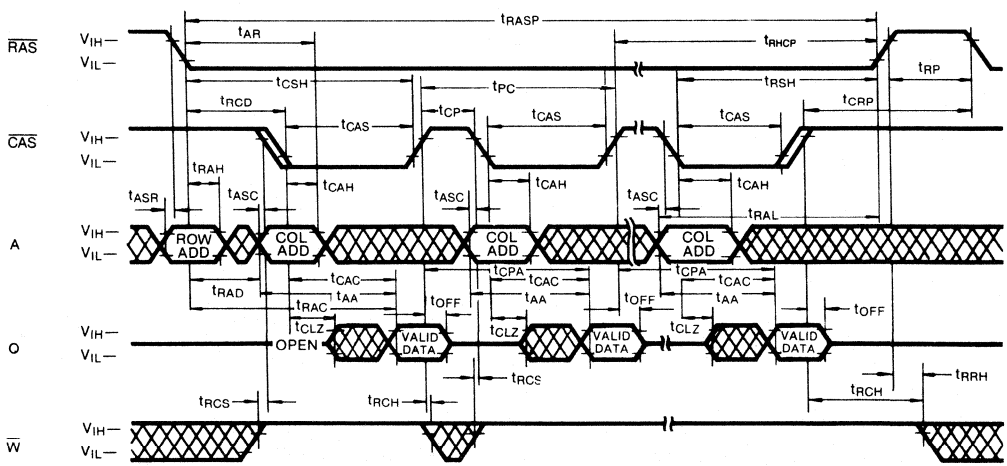


TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



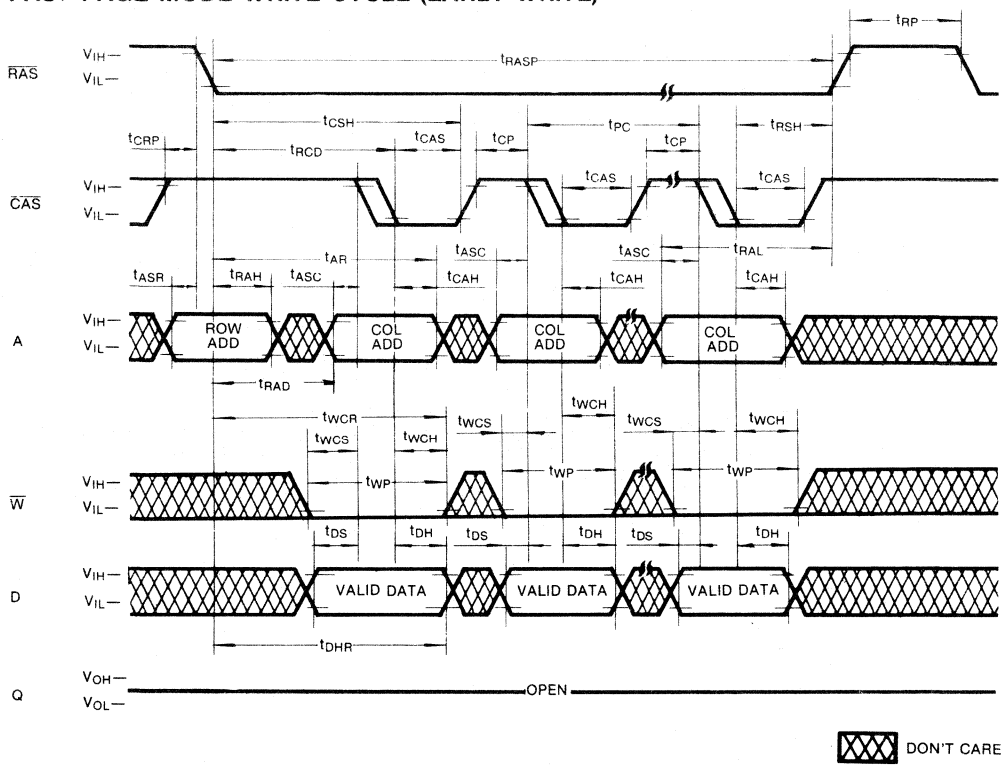
FAST PAGE MODE READ CYCLE



DON'T CARE

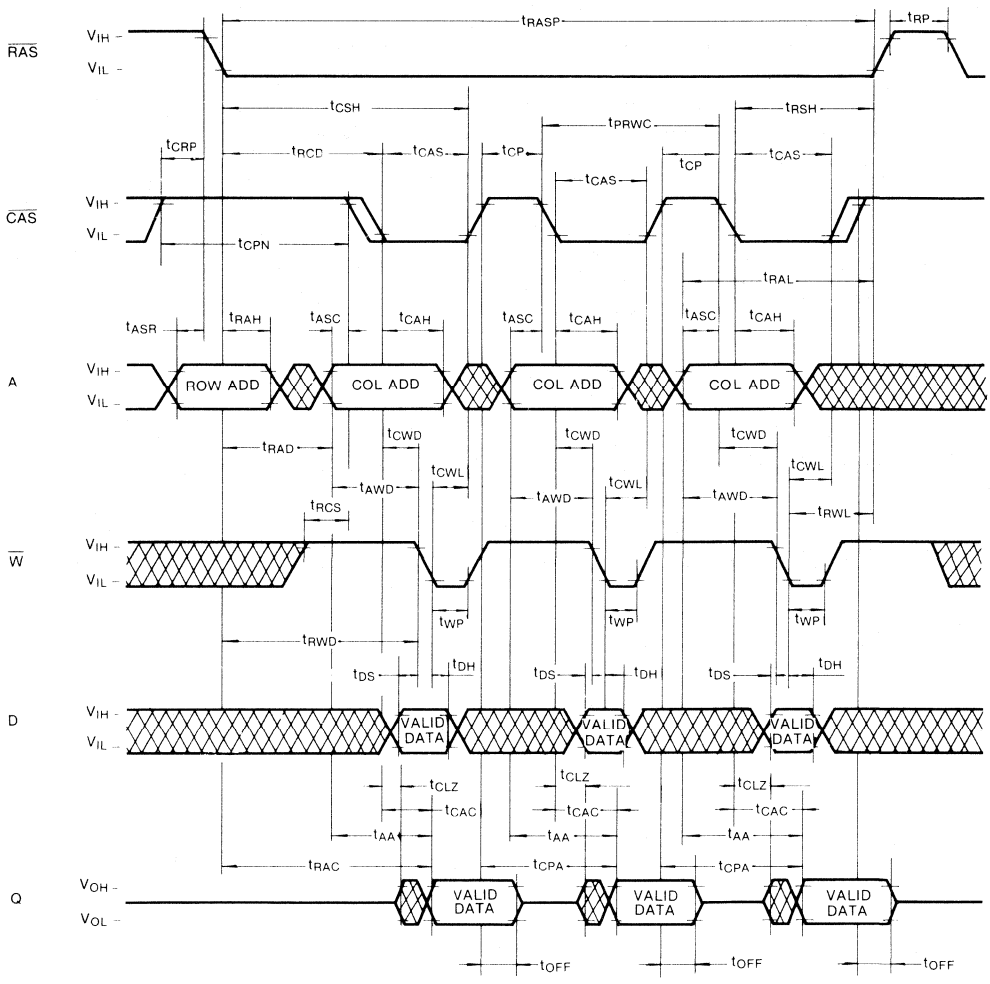
TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

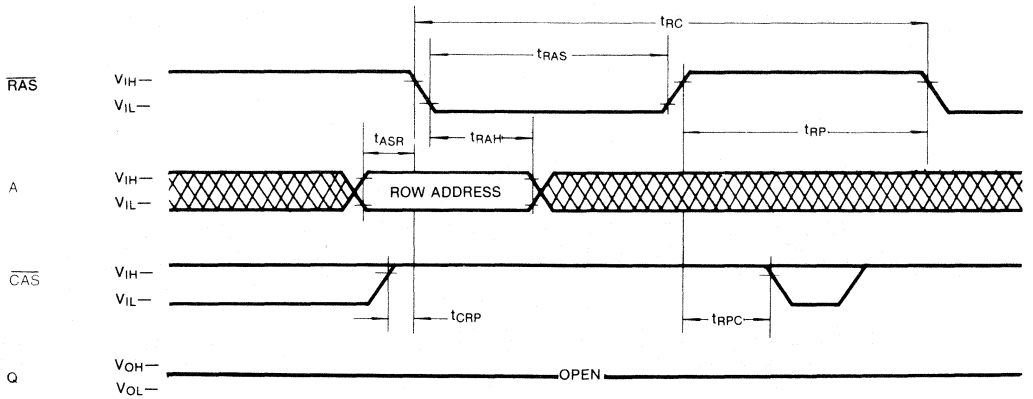
FAST PAGE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

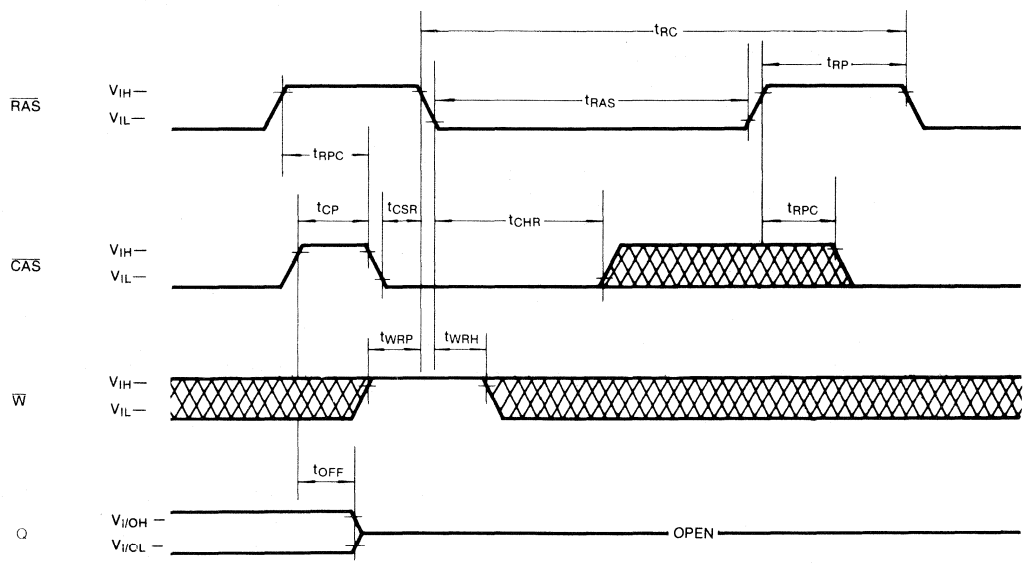
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, D, A_{10} = Don't Care



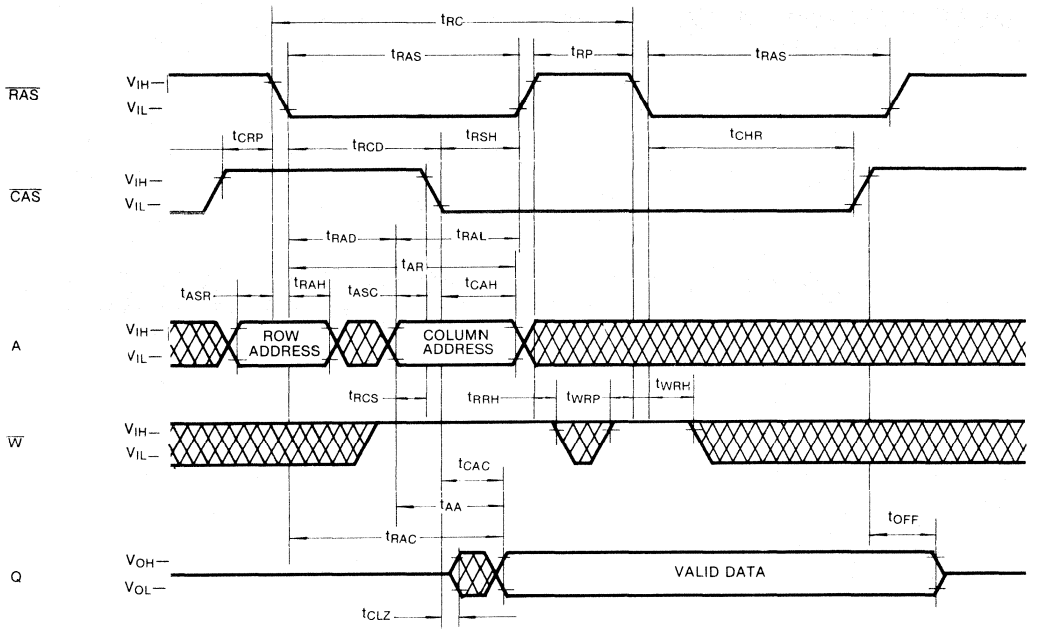
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address = Don't Care

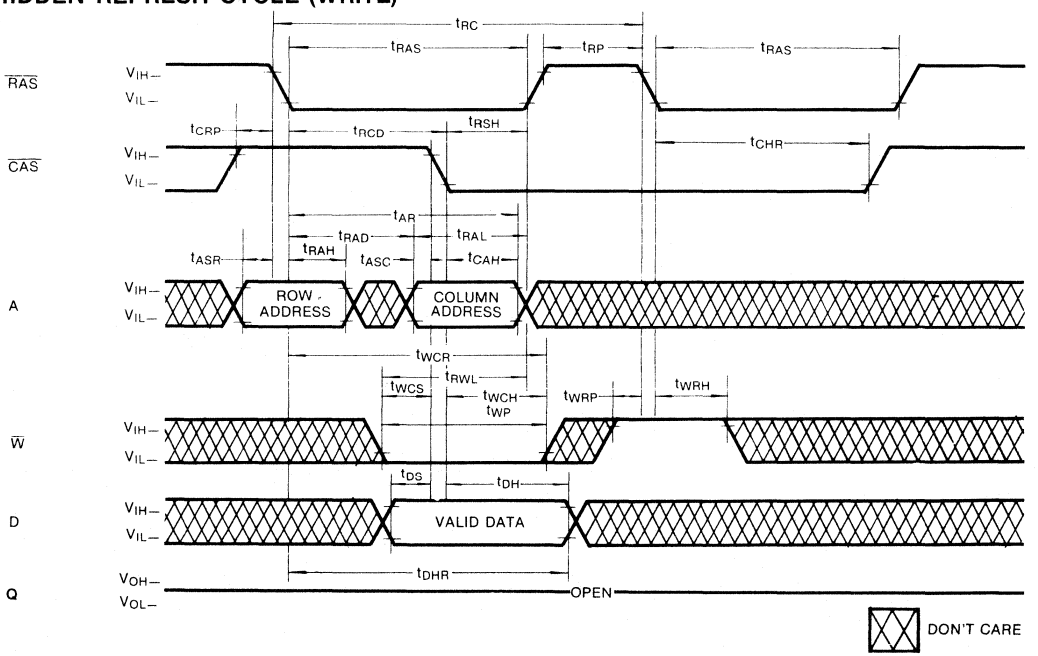


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

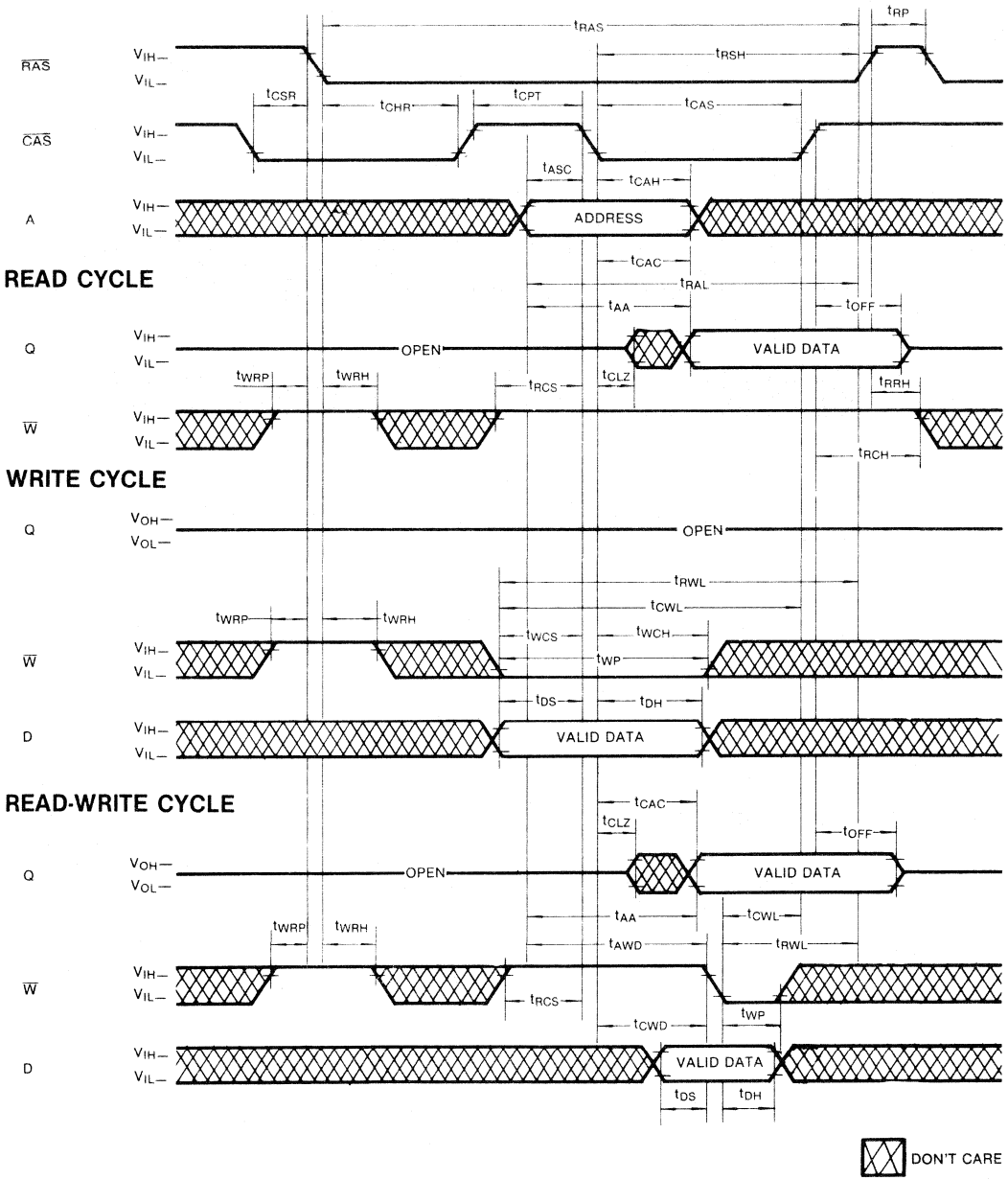


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

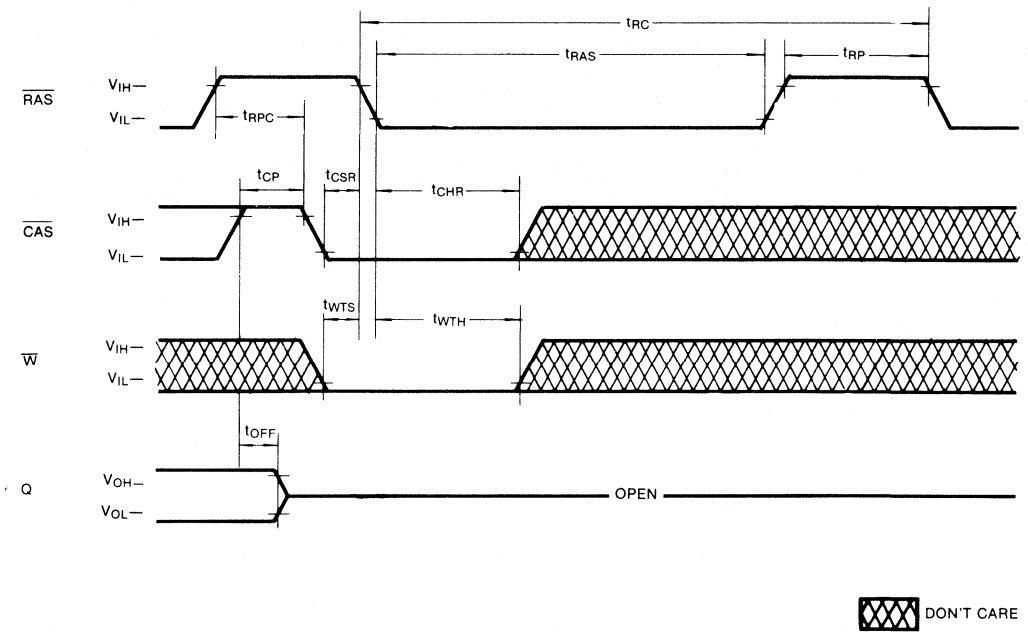
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address= Don't care



TEST MODE DESCRIPTION

The KM41C4000AL is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}, A_{10C} and A_{0C} are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed the data output pin would indicate a "0" In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM. $\overline{W}$, $\overline{CAS}$-Before $\overline{RAS}$-Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/8 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM41C4000AL contains 4,194,304 memory locations. Twenty-two address bits are required to address a particular memory location. Since the KM41C4000AL has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM41C4000AL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C4000AL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C4000AL begin a complex sequence of events. If the sequence if broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41C4000AL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C4000AL has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C4000AL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C4000AL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every

DEVICE OPERATION (Continued)

128 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C4000AL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuity is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C4000AL hidden refresh cycle is actually a $\overline{CAS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C4000AL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM41C4000AL has Fast Page mode capability. Fast Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In Fast Page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A Fast Page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row address for the same page. Up to 2048 memory cells can be accessed with the same row address.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter. This A_{10} bit is set high internally.

Column Address—Bits A_0 through A_{10} are strobedin by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

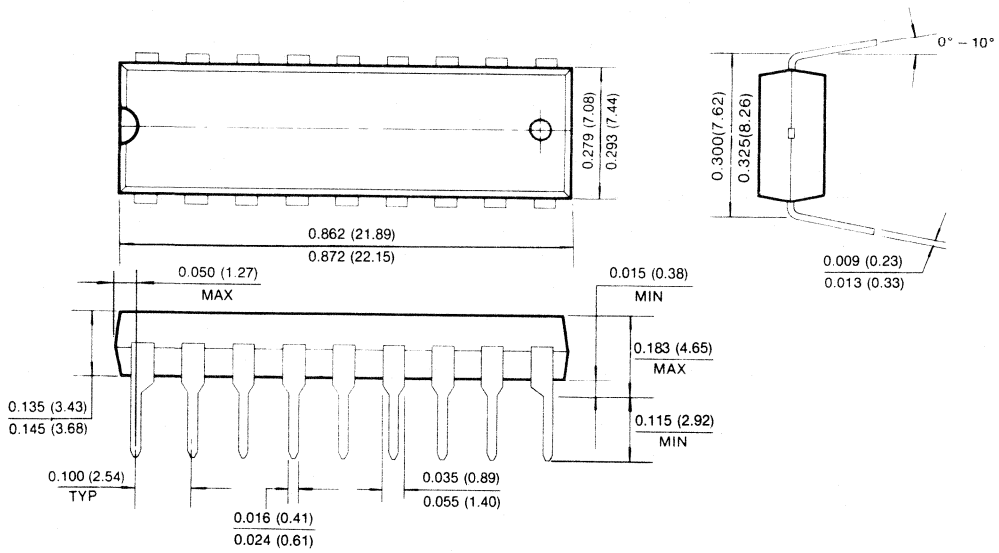
If $\overline{RAS}=V_{SS}$ during power-up, the KM41C4000AL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200μs is required after power-up followed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$ only refresh cycles before proper device operation is achieved.

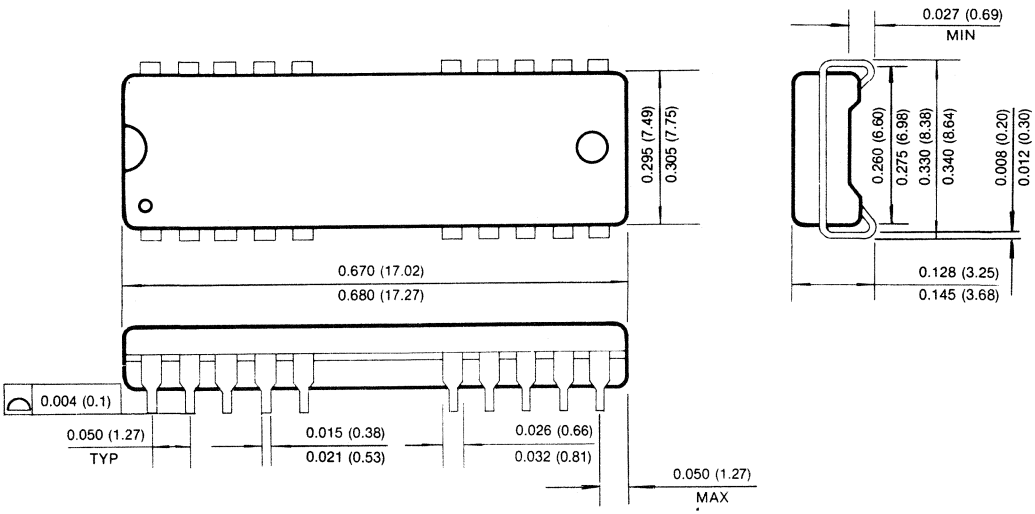
PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (Millimeters)



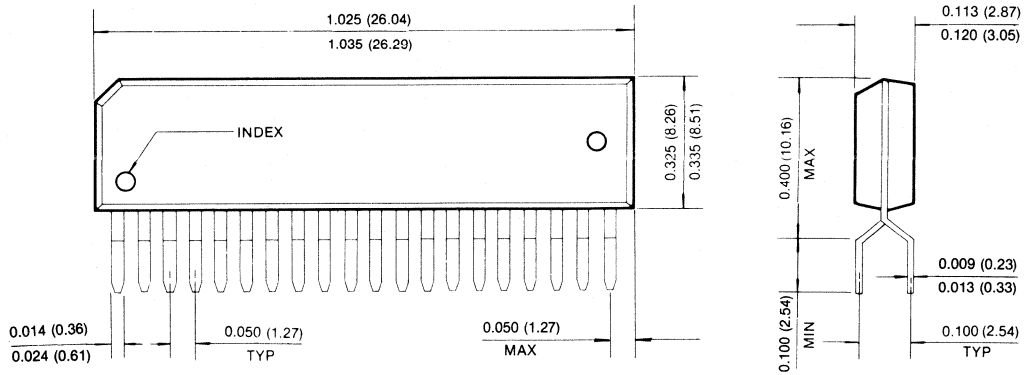
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)



4M×1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C4000ASL- 7	70ns	20ns	130ns
KM41C4000ASL- 8	80ns	20ns	150ns
KM41C4000ASL-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8-bit fast parallel test mode capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Write**
- **Single +5V±10% power supply**
- **1024 cycles/256ms refresh**
- **Low power dissipation**
  - **—Standby: 0.6mW**
  - **—Active (70/80/100ns): 578/523/468mW**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, DIP, ZIP**

GENERAL DESCRIPTION

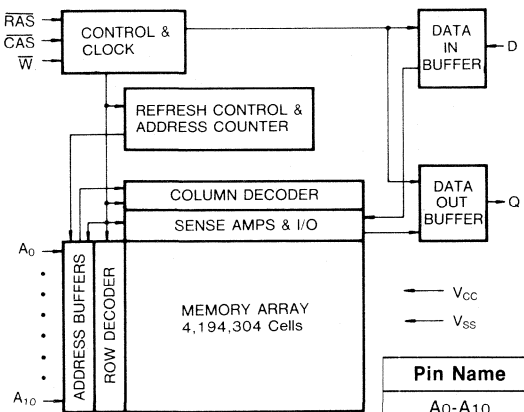
The Samsung KM41C4000ASL is a high speed CMOS 4,194,304 bit × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C4000ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

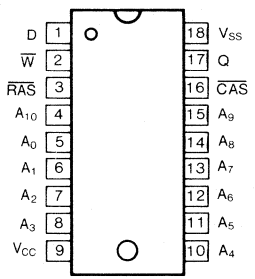
The KM41C4000ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

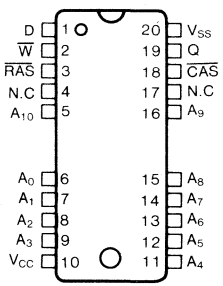


PIN CONFIGURATION (Top Views)

- **KM41C4000ASLP**

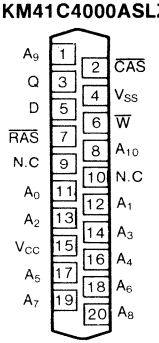


- **KM41C4000ASLJ**



Pin Name	Pin Function
A0-A10	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

- **KM41C4000ASLZ**



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC}=5.0V \pm 10\%$)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM41C4000ASL- 7	I_{CC1}	—	105	mA
	KM41C4000ASL- 8		—	95	mA
	KM41C4000ASL-10		—	85	mA
Standby Current ($\overline{RAS}=\overline{CAS}=V_{IH}$)		I_{CC2}	—	2	mA
RAS-Only Refresh Current* ($\overline{CAS}=V_{IH}$, $\overline{RAS}$ Cycling @ t_{RC}=min.)	KM41C4000ASL- 7	I_{CC3}	—	105	mA
	KM41C4000ASL- 8		—	95	mA
	KM41C4000ASL-10		—	85	mA
Fast Page Mode Current* ($\overline{RAS}=V_{IL}$, $\overline{CAS}$ Cycling @ t_{PC}=min.)	KM41C4000ASL- 7	I_{CC4}	—	80	mA
	KM41C4000ASL- 8		—	70	mA
	KM41C4000ASL-10		—	60	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W} \geq V_{CC}-0.2V$)		I_{CC5}	—	100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM41C4000ASL- 7	I_{CC6}	—	105	mA
	KM41C4000ASL- 8		—	95	mA
	KM41C4000ASL-10		—	85	mA
Battery Back Up CurrentAverage Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{CC}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}=\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V D_{IN}=Don't Care T_{RC}=250μS, $T_{RAS}=t_{RAS}$ min.~1μS		I_{CC7}	—	150	μA
Standby Current ($\overline{RAS}=V_{IH}$, $\overline{CAS}=V_{IL}$, Dout Enable)		I_{CC8}	—	5	mA
Input Leakage Current (Any input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test=0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0 \leq V_{OUT} \leq 5.5V$)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*Note: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}=V_{IL}$. I_{CC4}, Address can be changed maximum once while $\overline{CAS}=V_{IH}$.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{10}, D)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM41C4000ASL-7		KM41C4000ASL-8		KM41C4000ASL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	155		175		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	12
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	8
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	12
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	9

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM41C4000ASL-7		KM41C4000ASL-8		KM41C4000ASL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		20		ns	9
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	12
Refresh period (1024 cycles)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	7
$\overline{CAS}$ to write enable delay	t_{CWD}	20		20		25		ns	7
$\overline{RAS}$ to write enable delay	t_{RWD}	70		80		100		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		50		ns	7
$\overline{CAS}$ setup time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
FAst Page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	45		45		55		ns	
Fast page mode read-modify-write	t_{PRWC}	75		75		90		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	

TEST MODE CYCLE

(Note. 11)

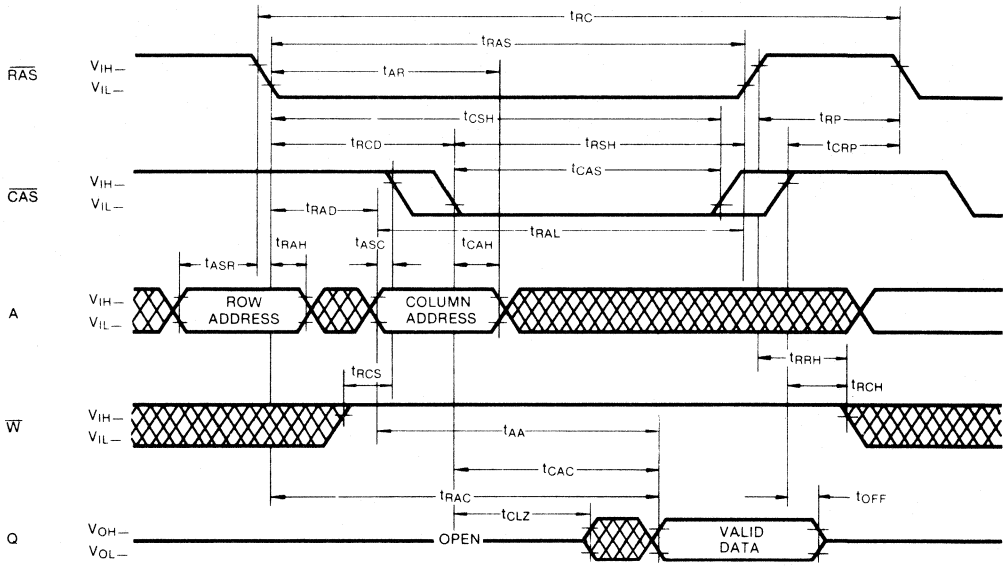
Standard Operation	Symbol	KM41C4000ASL-7		KM41C4000ASL-8		KM41C4000ASL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	135		155		185		ns	
Read-modify-write cycle time	t_{RWC}	160		180		215		ns	
Access time from $\overline{RAS}$	t_{RAC}		75		85		105	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		25		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		45		55	ns	3,10
$\overline{RAS}$ pulse width	t_{RAS}	75	10,000	85	10,000	105	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{CAS}$ hold time	t_{CSH}	75		85		105		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		45		55		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	25		25		30		ns	7
$\overline{RAS}$ to write enable delay	$_{RWD}$	75		85		105		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	40		45		55		ns	7
Fast mode cycle time	t_{PC}	55		55		65		ns	
Fast page mode read-modefy-write	t_{PRWC}	80		80		95		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	75	200,000	85	200,000	105	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		50		60	ns	3

NOTES

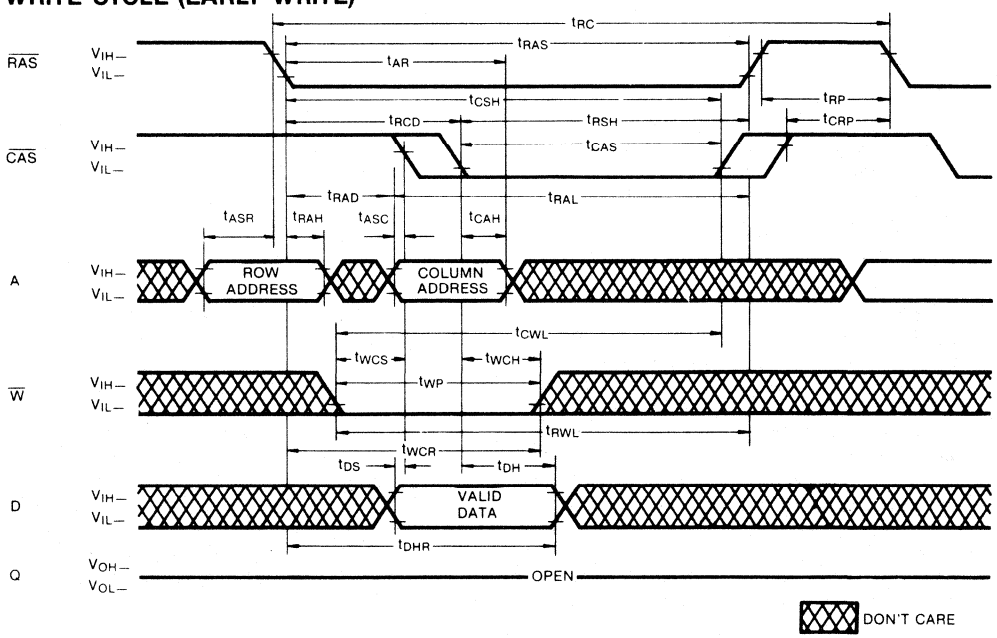
1. An initial pause of 200μs is required after power-up followed by and 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
10. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
11. These specifications are applied in the test mode.
12. t_{AR}, t_{WCR}, t_{DHR} are refrerenced to $t_{RAD(max)}$.

TIMING DIAGRAMS

READ CYCLE

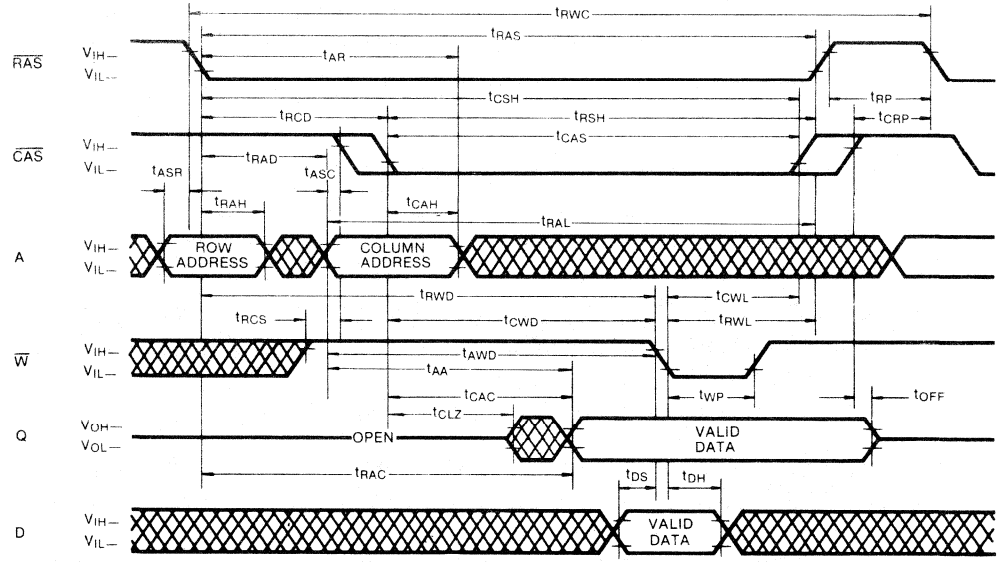


WRITE CYCLE (EARLY WRITE)

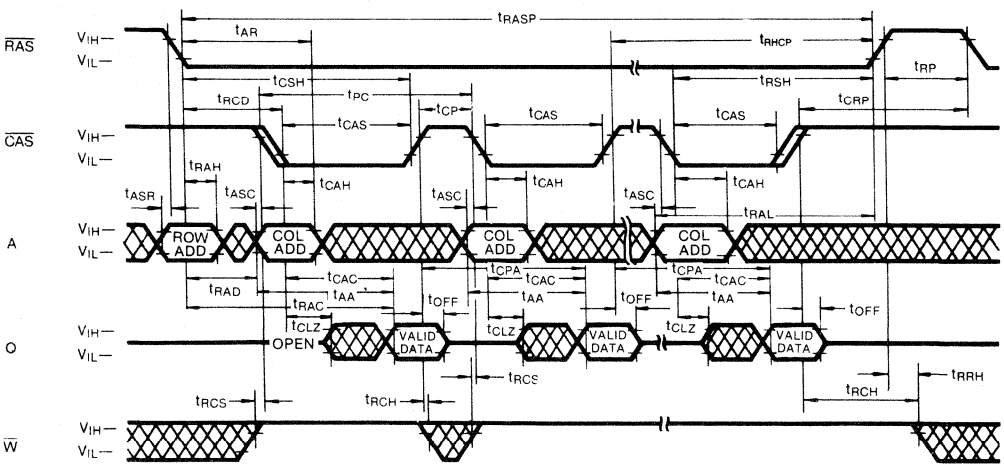


TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



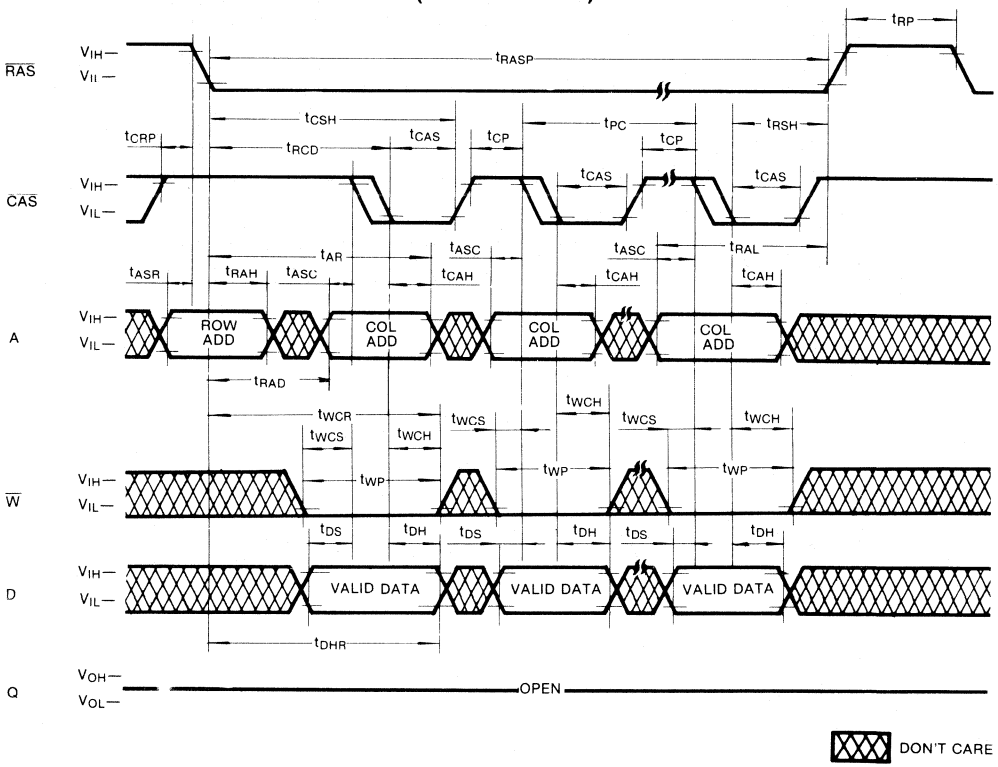
FAST PAGE MODE READ CYCLE



DON'T CARE

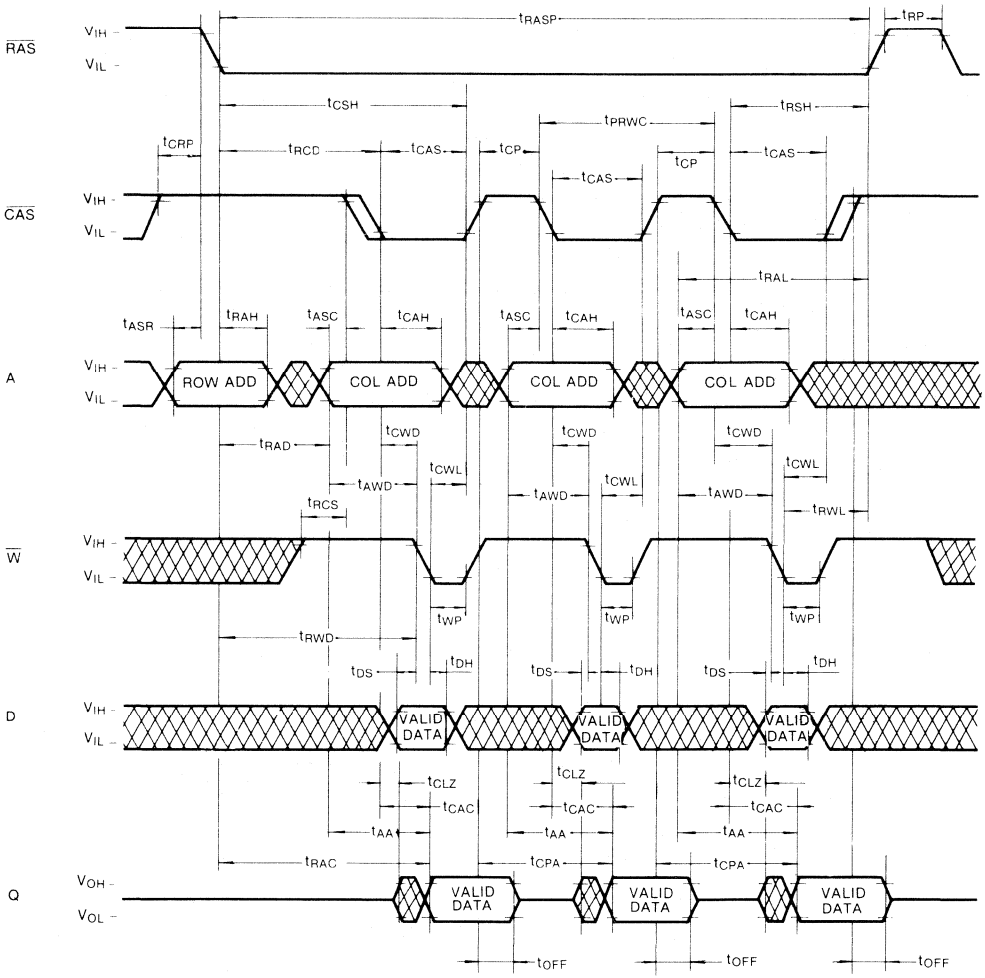
TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

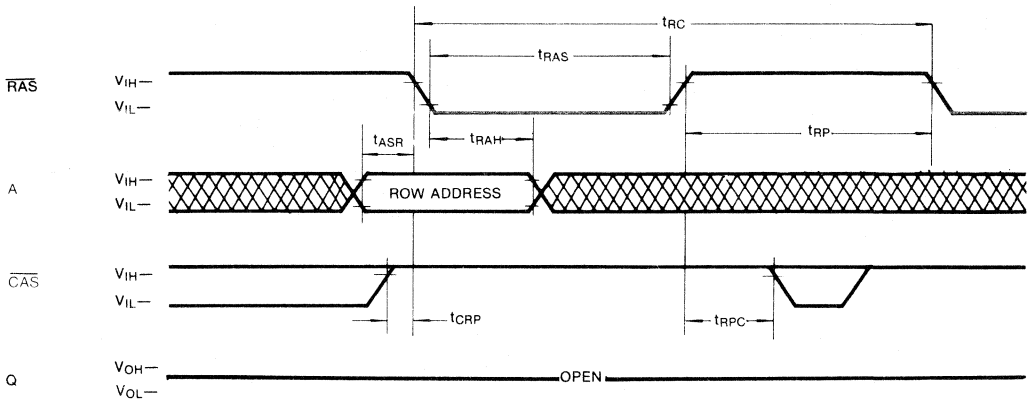
FAST PAGE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

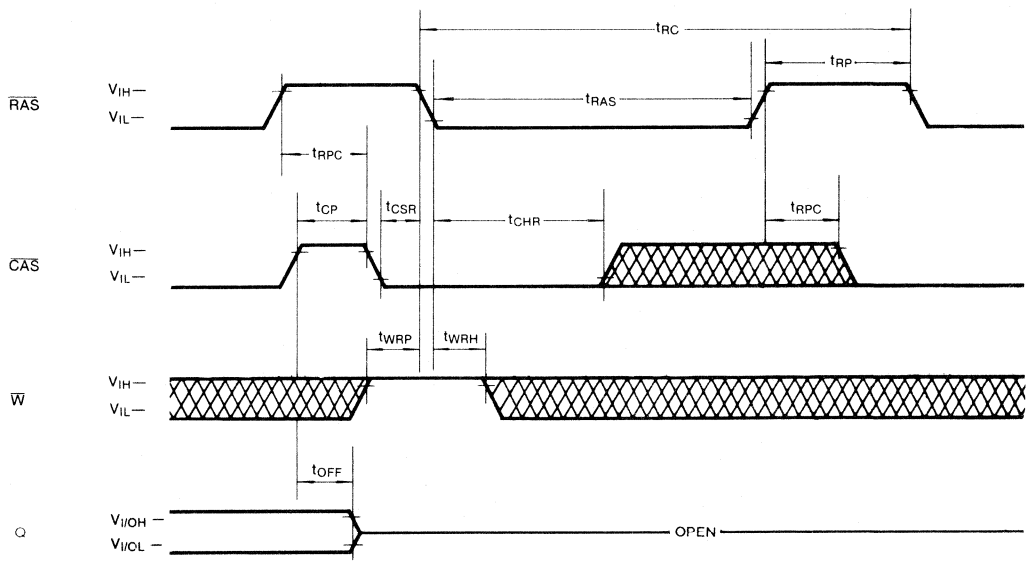
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, D, A_{10} = Don't Care



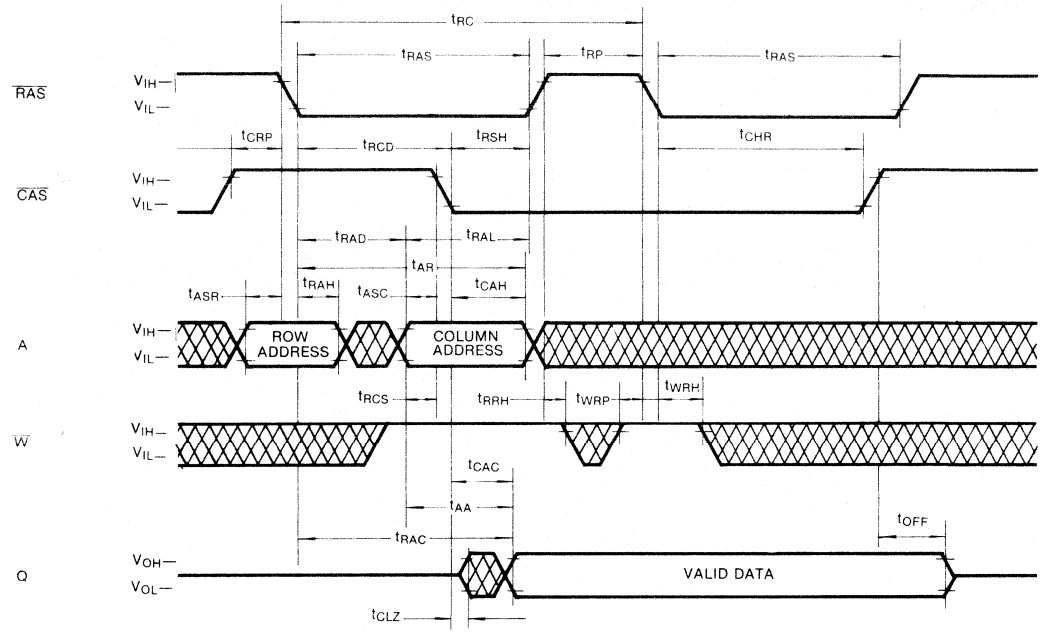
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address = Don't Care

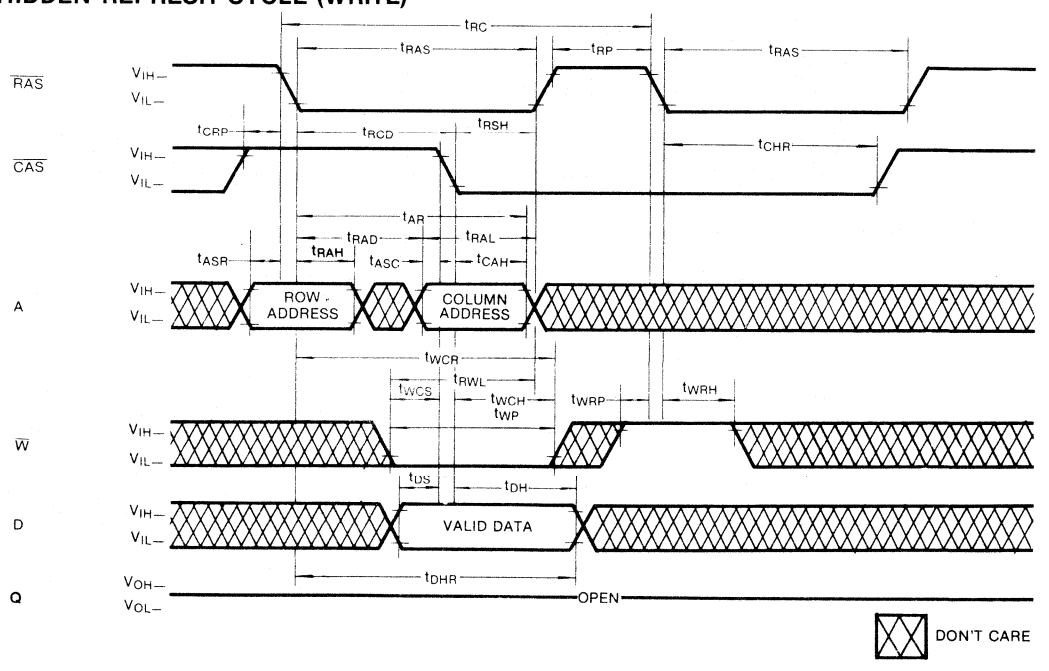


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

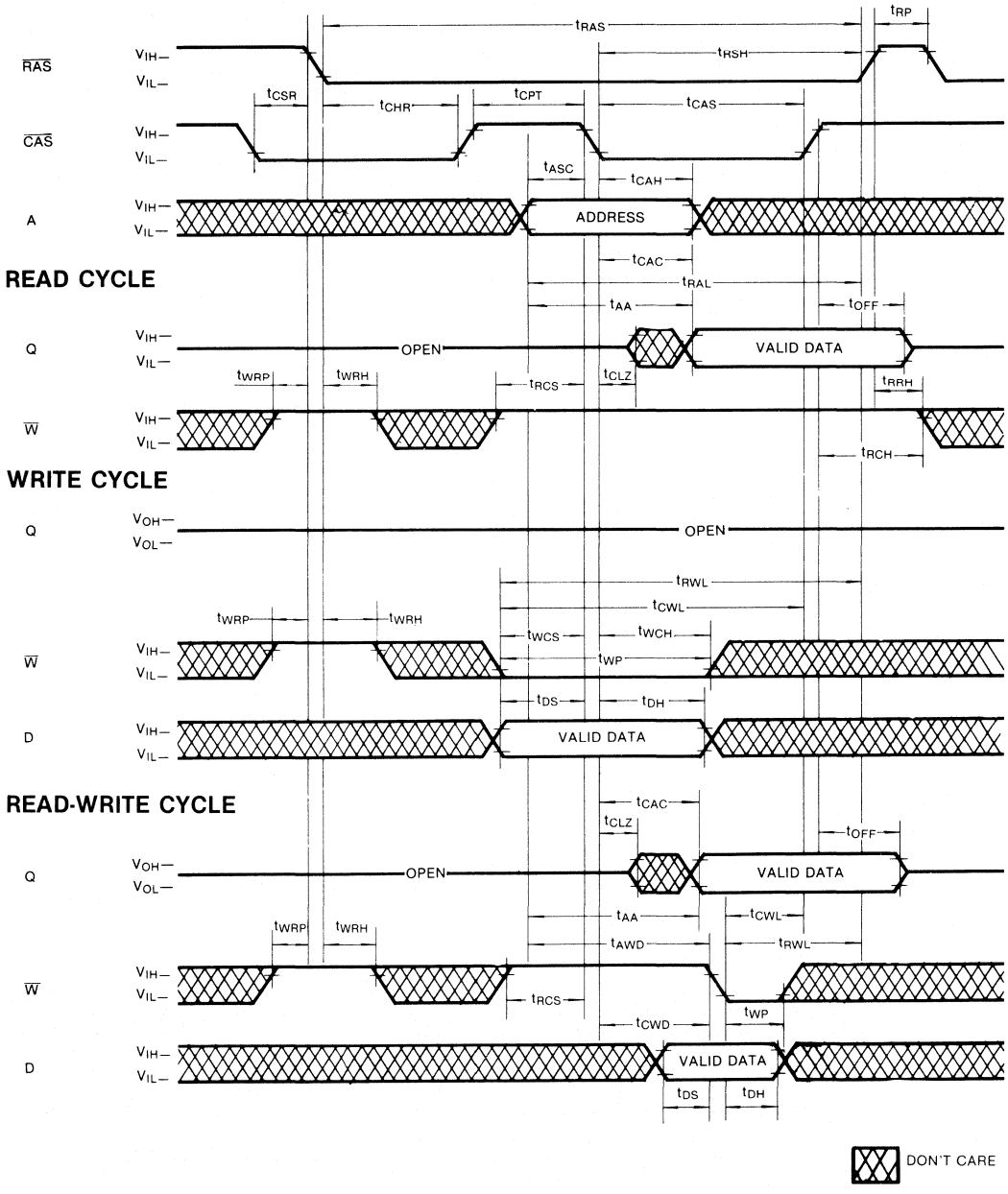


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

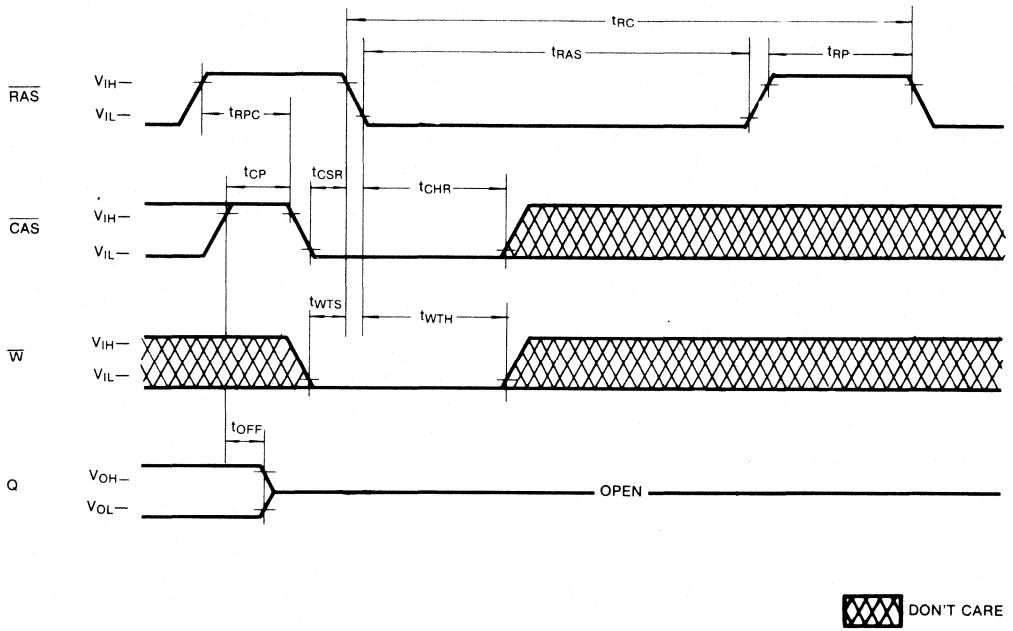
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address=Don't Care



TEST MODE DESCRIPTION

The KM41C4000ASL is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}, A_{10C} and A_{0C} are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed the data output pin would indicate a "0" In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM. $\overline{W}$, $\overline{CAS}$-Before-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/8 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM41C4000ASL contains 4,194,304 memory locations. Twenty-two address bits are required to address a particular memory location. Since the KM41C4000ASL has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM41C4000ASL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C4000ASL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C4000ASL begin a complex sequence of events. If the sequence if broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41C4000ASL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C4000ASL has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C4000ASL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C4000ASL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every

DEVICE OPERATION (Continued)

256 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C4000ASL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuity is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C4000ASL hidden refresh cycle is actually a $\overline{CAS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C4000ASL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM41C4000ASL has Fast Page mode capability. Fast Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In Fast Page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A Fast Page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row address for the same page. Up to 2048 memory cells can be accessed with the same row address.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter. This A_{10} bit is set high internally.

Column Address—Bits A_0 through A_{10} are strobedin by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

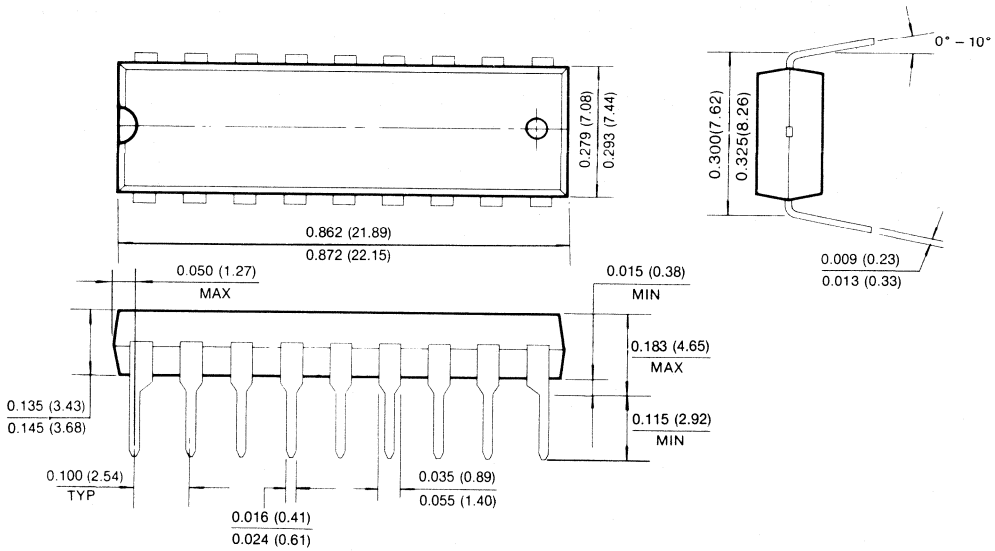
If $\overline{RAS}$=V_{SS} during power-up, the KM41C4000ASL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200μs is required after power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.

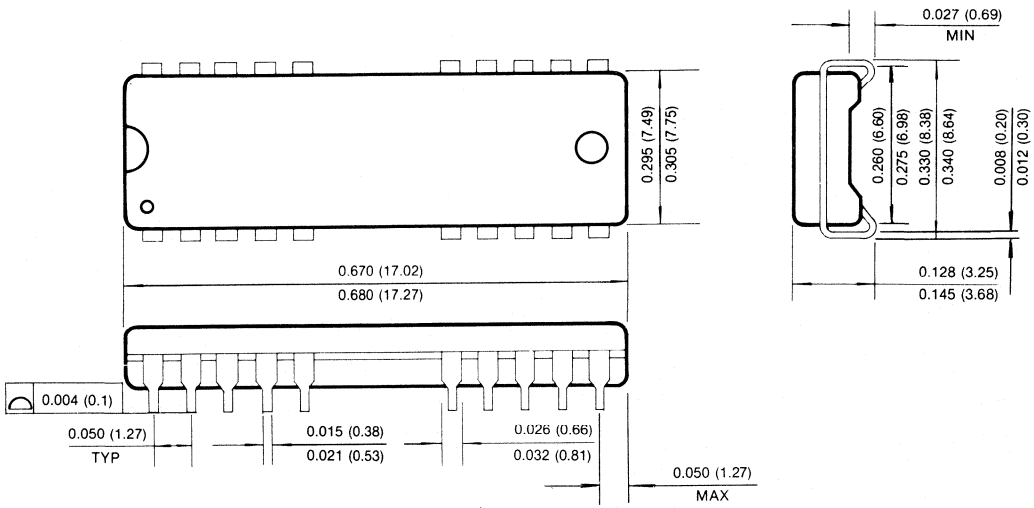
PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (Millimeters)



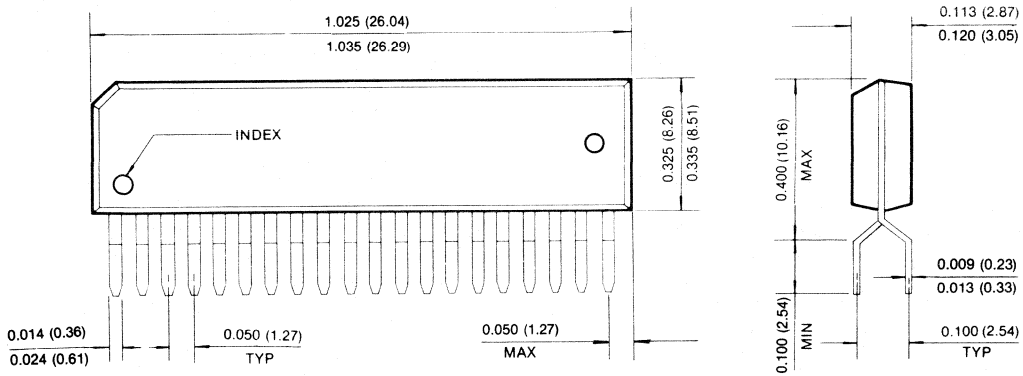
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)



4MX1 Bit CMOS Dynamic RAM with Nibble Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C4001A- 7	70ns	20ns	130ns
KM41C4001A- 8	80ns	20ns	150ns
KM41C4001A-10	100ns	25ns	180ns

- **Nibble Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh Capability**
- **$\overline{RAS}$-only and Hidden Refresh Capability**
- **8-bit fast parallel test mode Capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Write**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, DIP, ZIP**

GENERAL DESCRIPTION

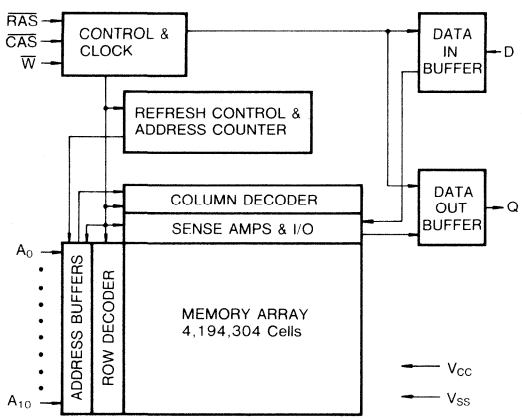
The Samsung KM41C4001A is a CMOS high speed 4,194,304 bit × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C4001A features Nibble Mode operation which allows high speed serial access of up to 4 bits of data.

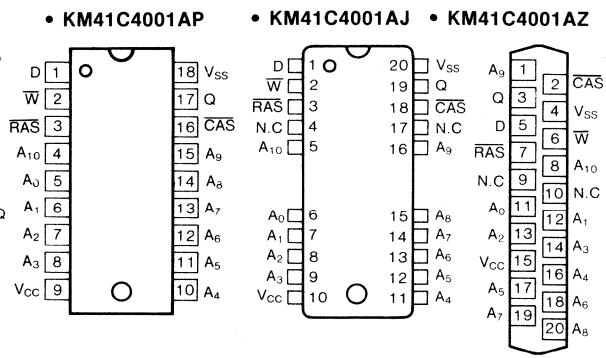
$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM41C4001A is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A_0-A_{10}	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, Ta=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC}=5.0V \pm 10\%$)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM41C4001A- 7	I_{CC1}	—	105	mA
	KM41C4001A- 8		—	95	mA
	KM41C4001A-10		—	85	mA
Standby Current ($\overline{RAS}=\overline{CAS}=V_{IH}$)		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}=V_{IH}$, $\overline{RAS}$ Cycling @ t_{RC}=min.)	KM41C4001A- 7	I_{CC3}	—	105	mA
	KM41C4001A- 8		—	95	mA
	KM41C4001A-10		—	85	mA
Nibble Mode Current* ($\overline{RAS}=V_{IL}$, $\overline{CAS}$, Address Cycling: t_{NC}=min.)	KM41C4001A- 7	I_{CC4}	—	80	mA
	KM41C4001A- 8		—	70	mA
	KM41C4001A-10		—	60	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W} \geq V_{CC}-0.2V$)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM41C4001A- 7	I_{CC6}	—	105	mA
	KM41C4001A- 8		—	95	mA
	KM41C4001A-10		—	85	mA
Standby Current ($\overline{RAS}=V_{IH}$, $\overline{CAS}=V_{IL}$, Dout Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test=0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0 \leq V_{OUT} \leq 5.5V$)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}=V_{IL}$. I_{CC4}, Address can be changed maximum once while $\overline{CAS}=V_{IH}$.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{10}, D)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM41C4001A-7		KM41C4001A-8		KM41C4001A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	155		175		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	12
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	8
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	12
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	9

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM41C4001A-7		KM41C4001A-8		KM41C4001A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		20		ns	9
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	12
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	7
$\overline{CAS}$ to write enable delay	t_{CWD}	20		20		25		ns	7
$\overline{RAS}$ to write enable delay	t_{RWD}	70		80		100		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		50		ns	7
$\overline{CAS}$ setup time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	
Nibble mode cycle time	t_{NC}	40		40		45		ns	
Nibble mode read-write cycle time	t_{NRWC}	65		65		70		ns	
Nibble mode access time	t_{NCAC}		20		20		25	ns	
Nibble mode $\overline{CAS}$ pulse width	t_{NCAS}	20		20		25		ns	
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	10		10		10		ns	
Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	20		20		25		ns	
Nibble mode $\overline{CAS}$ to $\overline{W}$ delay time	t_{NCWD}	20		20		25		ns	
Nibble mode $\overline{W}$ to $\overline{RAS}$ lead time	t_{NRWL}	20		20		25		ns	
Nibble mode $\overline{W}$ to $\overline{CAS}$ lead time	t_{NCWL}	20		20		25		ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	

TEST MODE CYCLE

(Note. 11)

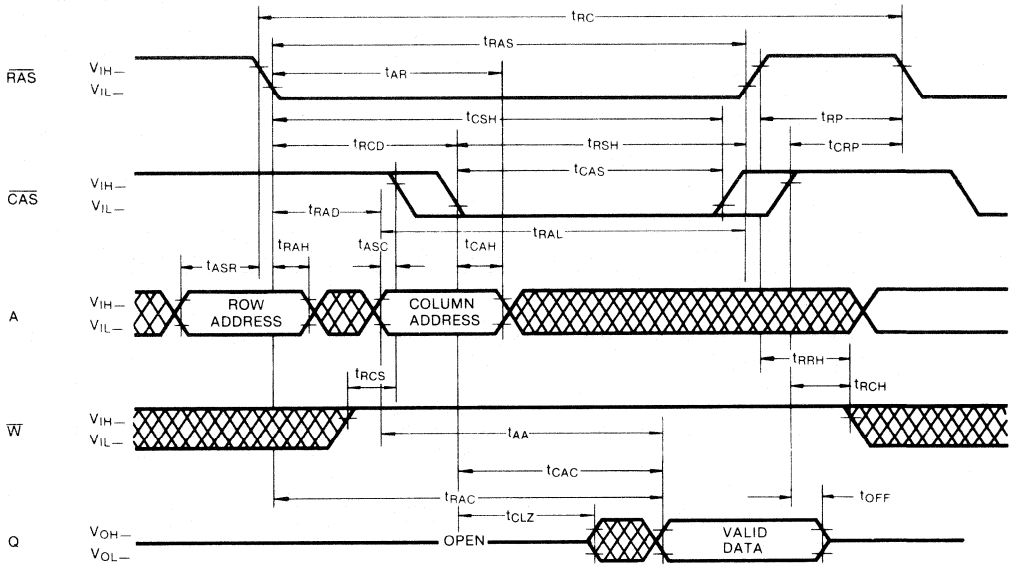
Standard Operation	Symbol	KM41C4001A-7		KM41C4001A-8		KM41C4001A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	135		155		185		ns	
Read-modify-write cycle time	t_{RWC}	160		180		215		ns	
Access time from $\overline{RAS}$	t_{RAC}		75		85		105	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		25		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		45		55	ns	3,10
$\overline{RAS}$ pulse width	t_{RAS}	75	10,000	85	10,000	105	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{CAS}$ hold time	t_{CSH}	75		85		105		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		45		55		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	25		25		30		ns	7
$\overline{RAS}$ to write enable delay	t_{RWD}	75		85		105		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	40		45		55		ns	7

NOTES

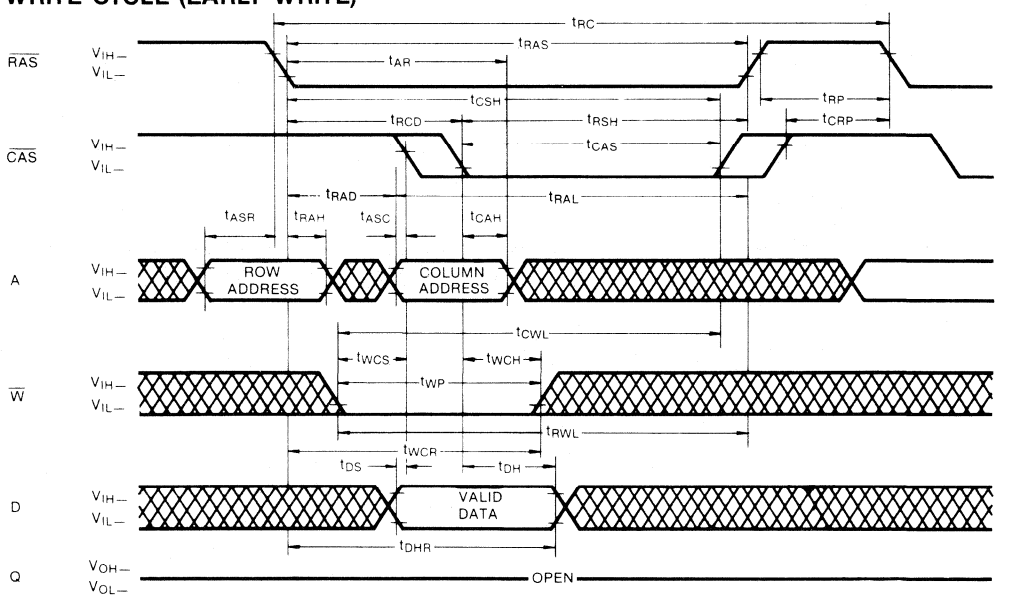
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
10. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
11. These specifications are applied in the test mode.
12. t_{AR}, t_{WCR}, t_{DHR} are refrerenced to $t_{RAD(max)}$.

TIMING DIAGRAMS

READ CYCLE



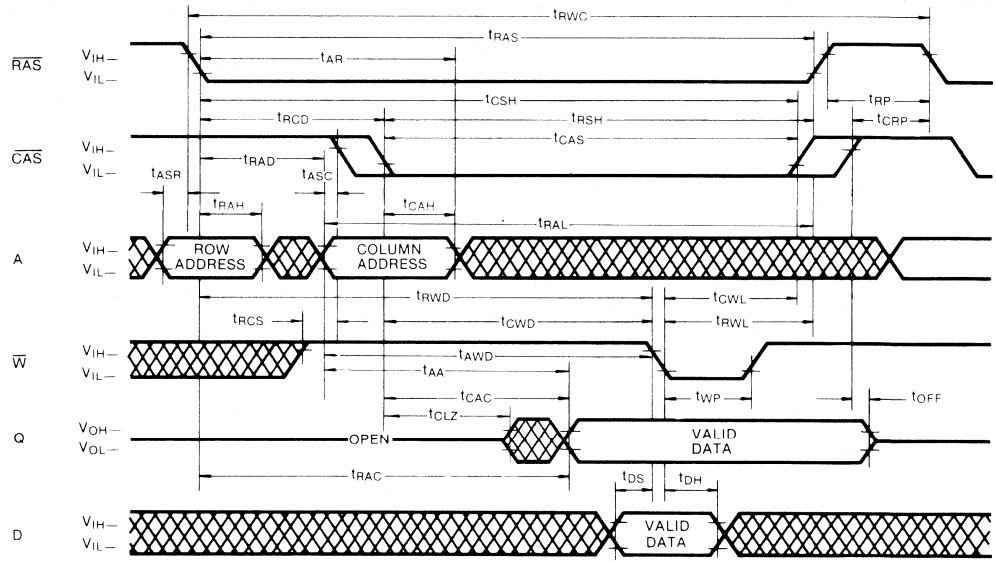
WRITE CYCLE (EARLY WRITE)



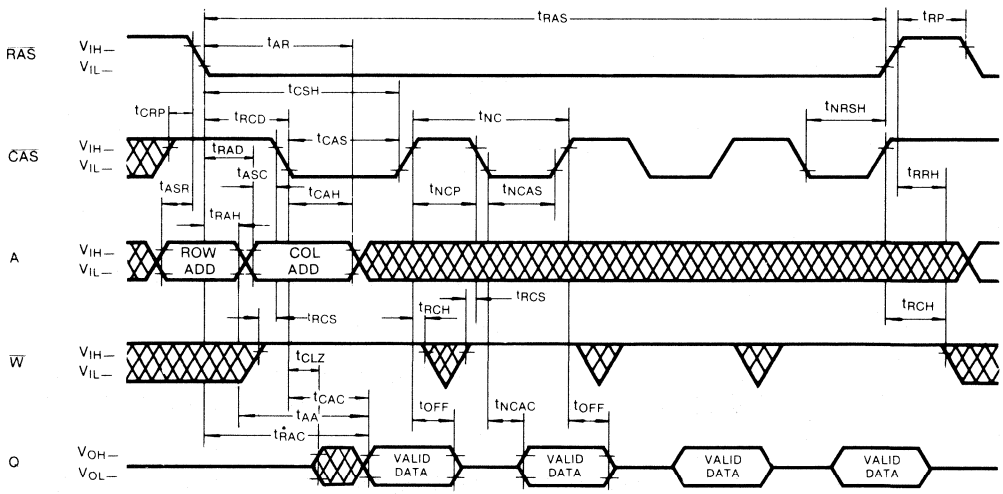
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



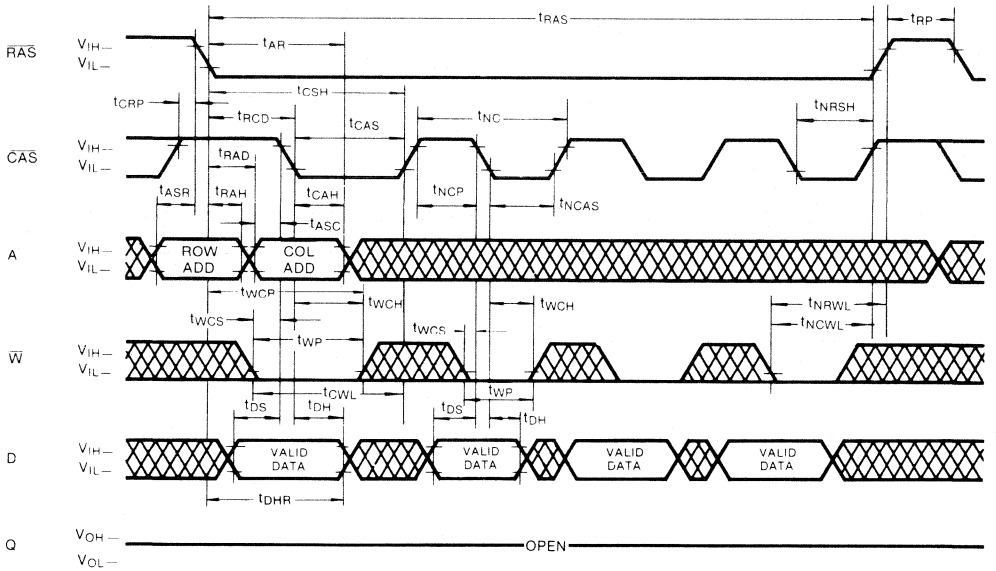
NIBBLE MODE READ CYCLE



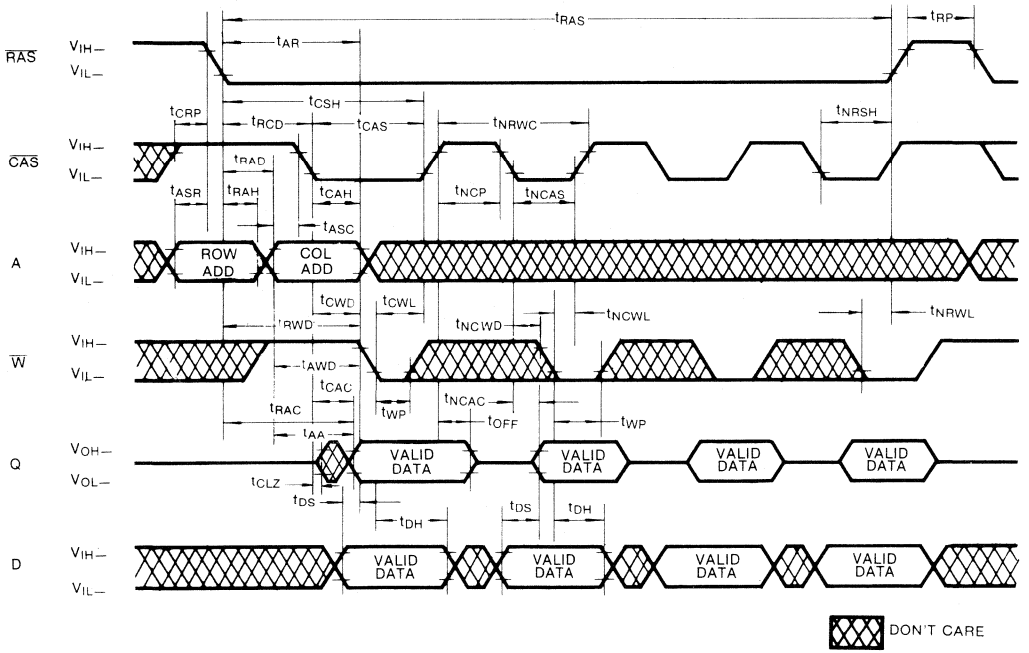
DON'T CARE

TIMING DIAGRAMS (Continued)

NIBBLE MODE WRITE CYCLE (EARLY WRITE)



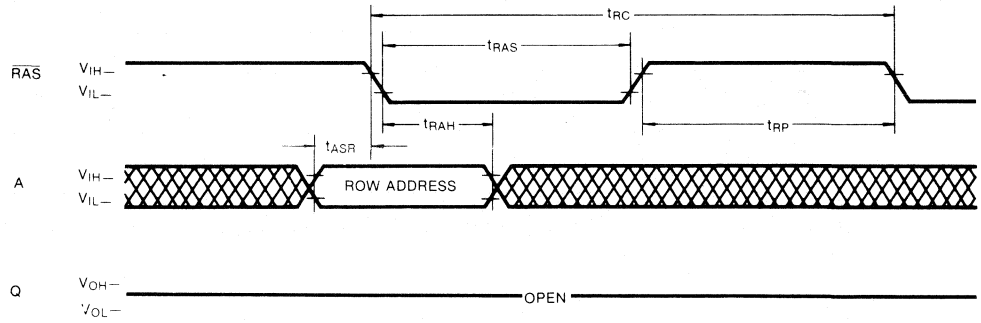
NIBBLE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

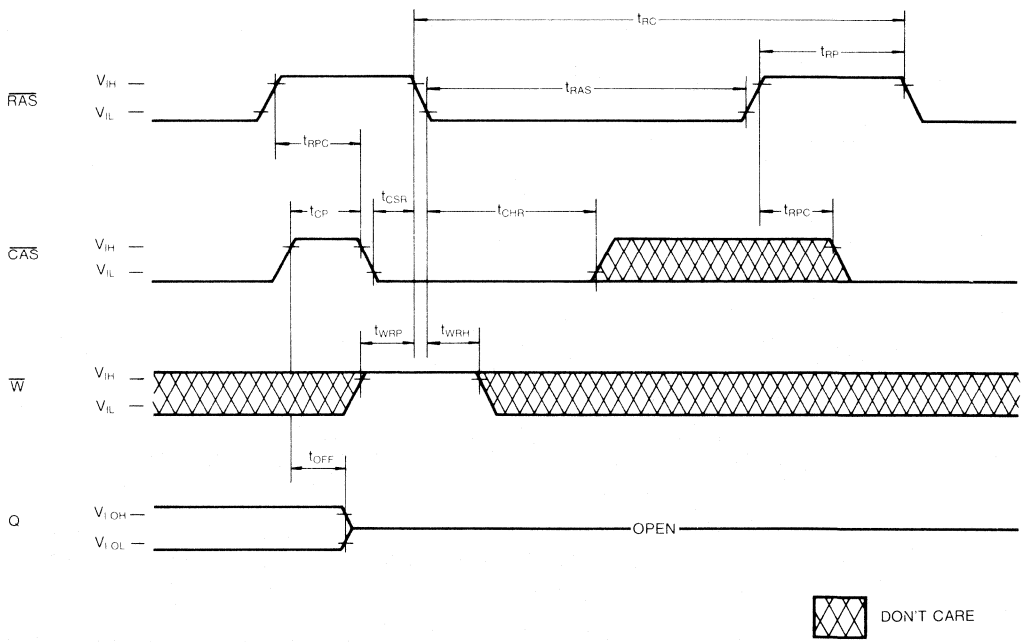
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{CAS}$=V_{IH}, $\overline{W}$,D, A_{10}=Don't Care



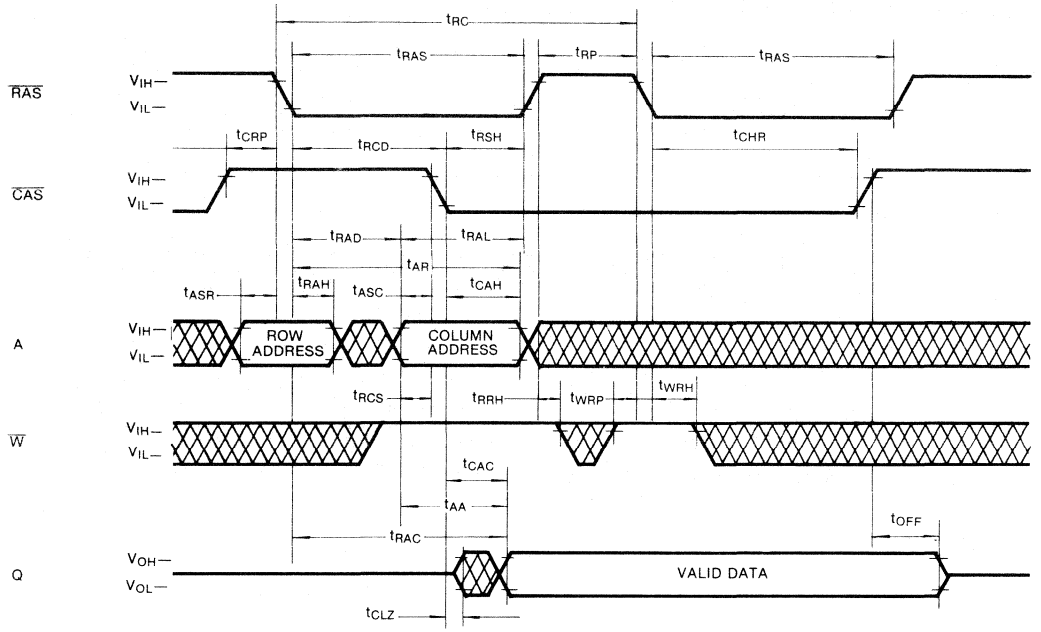
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: Address=Don't Care

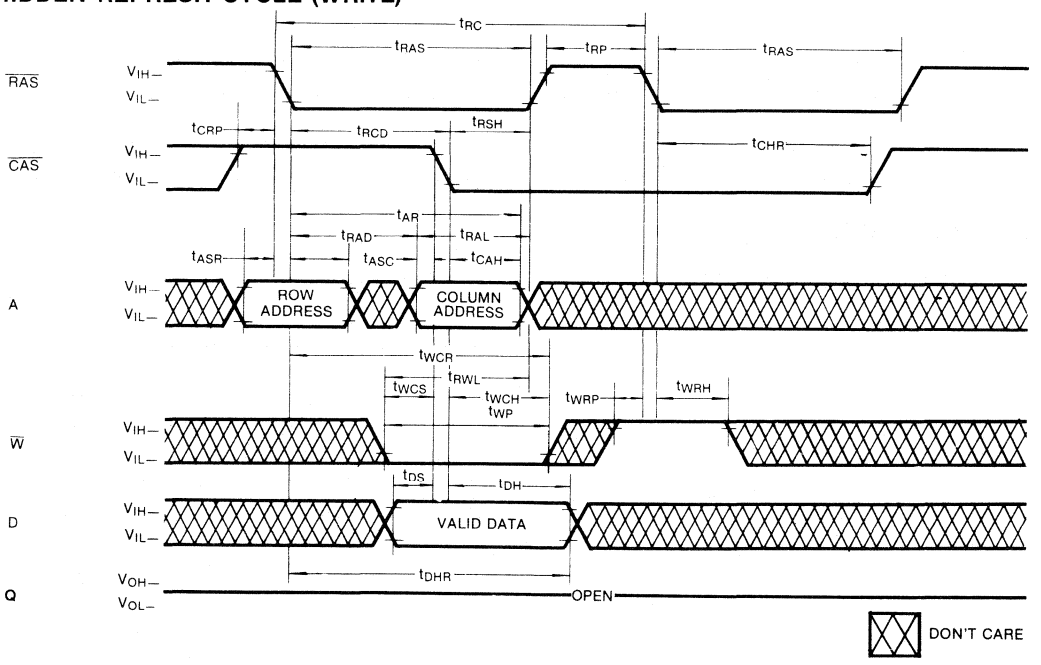


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

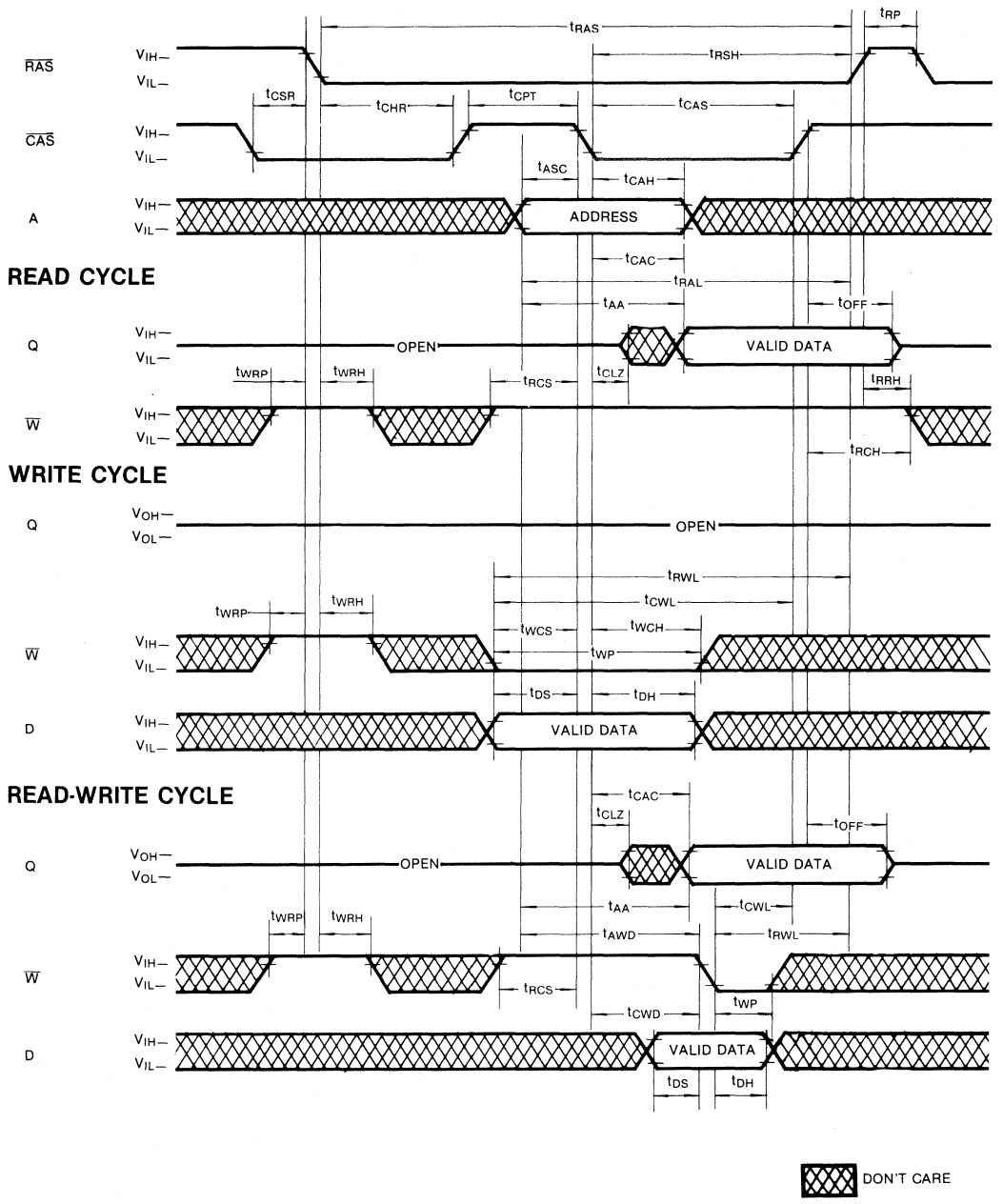


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

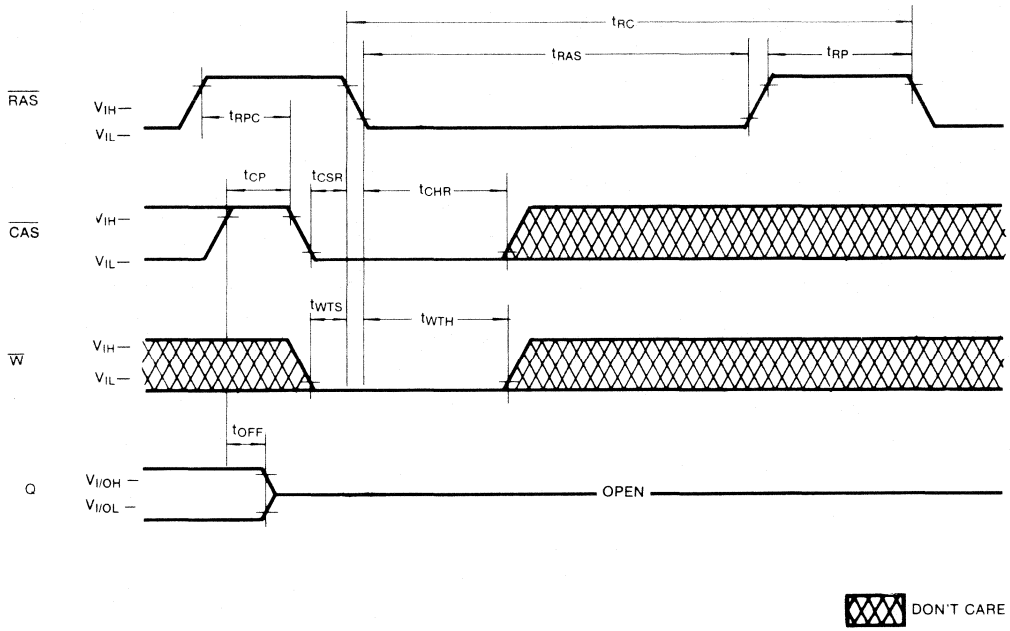
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address=Don't Care



TEST MODE DESCRIPTION

The KM41C4001A is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}. A_{10C} and A_{OC} are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0" In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM. $\overline{W}$, $\overline{CAS}$-Before-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/8 in cases of N test pattern).

DEVICE OPERATIONS

The KM41C4001A contains 4,194,304 memory locations. Twenty-two address bits are required to address a particular memory location. Since the KM41C4001A has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM41C4001A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C4001A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for porper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP} has been satisfied. Once a cycle begins internal clocks and other circuits within the KM41C4001A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41C4001A can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C4001A has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C4001A operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Nibble Mode Read, Nibble Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Nibble Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C4001A is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

DEVICE OPERATIONS (Continued)

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C4001A has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuity is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

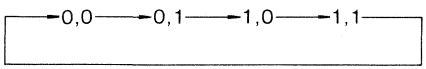
Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C4001A hidden refresh cycle is actually a $\overline{CAS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C4001A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Nibble Mode

The KM41C4001A has Nibble mode capability. Nibble mode operation allows high speed serial read, write or read-modify-write access of 4 consecutive bits. The first of 4 bits is accessed in the usual manner. The remaining nibble bits are accessed by toggling $\overline{CAS}$ high then low while $\overline{RAS}$ remains low.

The 4 bits of data that may be accessed during Nibble mode are determined by the lower 10 row address bits (R_{A0}-R_{A9}) and 10 column address bits (C_{A0}-C_{A9}). The two address bits, C_{A10} and R_{A10} are used to select 1 of the 4 nibble bits for initial access. The remaining nibble bits are accessed by toggling $\overline{CAS}$ with $\overline{RAS}$ held low. Each high-low $\overline{CAS}$ transition will internally increment the nibble address (C_{A10}, R_{A10}) as shown in the following diagram with R_{A10} being the least significant bit.



If more than 4 bits are accessed during Nibble mode, the address sequence will wrap around and repeat. If any bit is written during Nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on a subsequent access, the new data will be written into the selected cell location.

A nibble mode cycle can be a read, write or read-modify-write cycle. Any combinations of reads and writes or read-modify-write be allowed.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter. This A_{10} bit is set high internally.

Column Address—Bits A_0 through A_{10} are strobedin by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

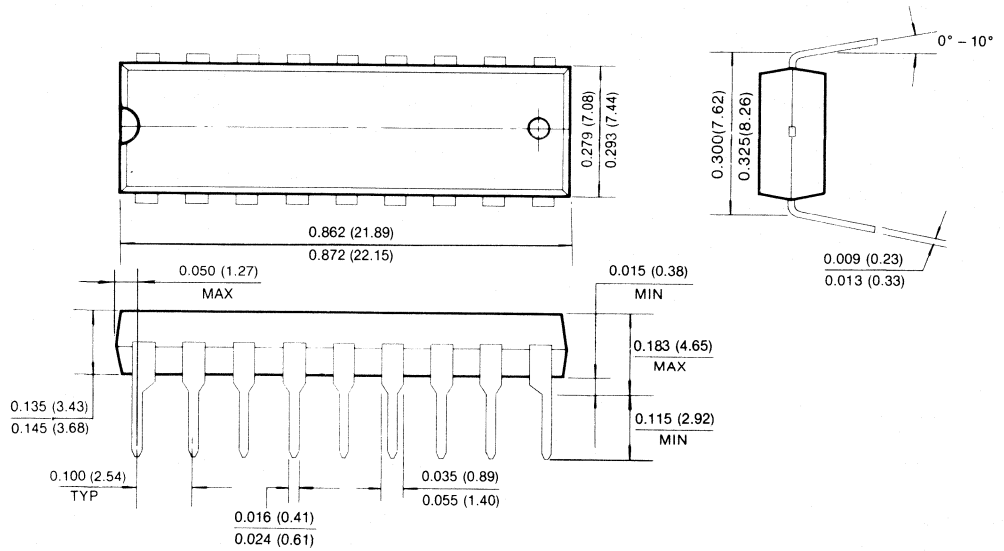
If $\overline{RAS}$=V_{SS} during power-up, the KM41C4001A could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

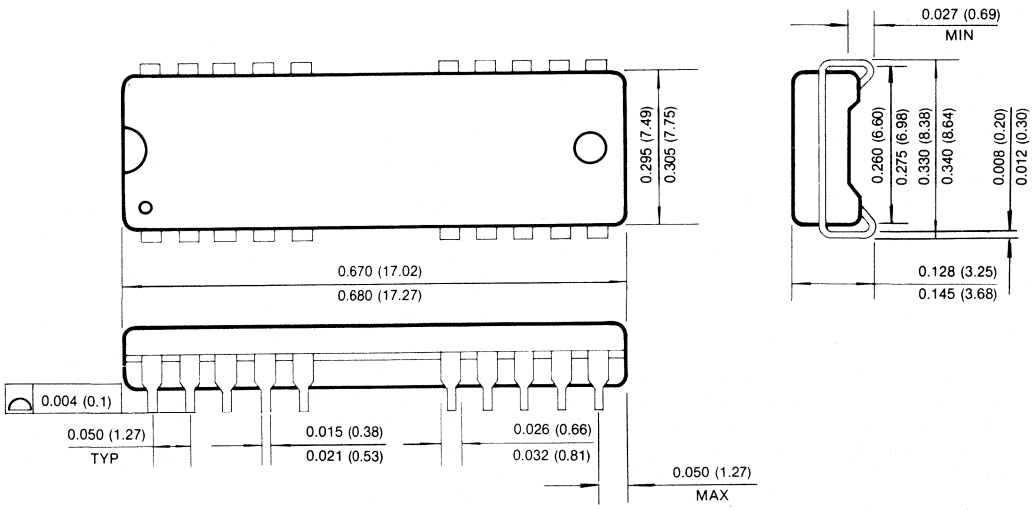
PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (Millimeters)



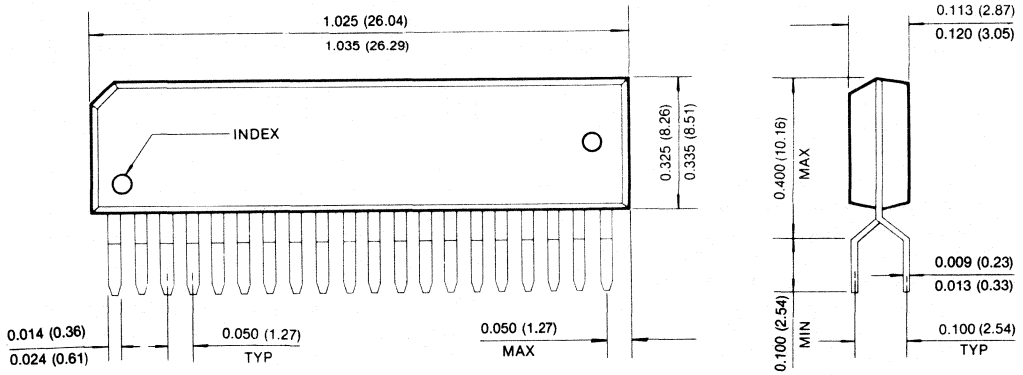
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)



2

4MX1 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C4002A- 7	70ns	20ns	130ns
KM41C4002A- 8	80ns	20ns	150ns
KM41C4002A-10	100ns	25ns	180ns

- **Static Column Mode operation**
- **$\overline{CS}$-before-$\overline{RAS}$ Refresh Capability**
- **$\overline{RAS}$-only and Hidden Refresh Capability**
- **8-bit fast parallel test mode Capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Write**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, DIP, ZIP**

GENERAL DESCRIPTION

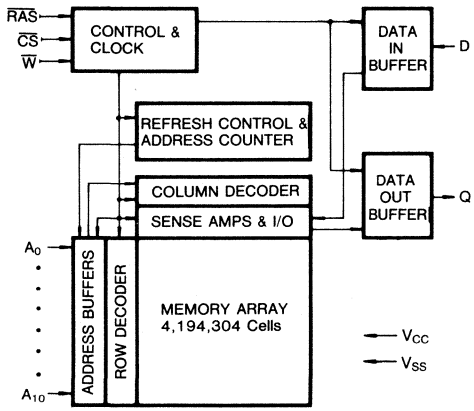
The Samsung KM41C4002A is a high speed CMOS 4,194,304 bit X 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C4002A features Static Column Mode operation which allows high speed random or sequential access within a row. Static Column Mode operation offers high performance while relaxing many critical system timing requirements for fast usable speed.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and output are fully TTL compatible.

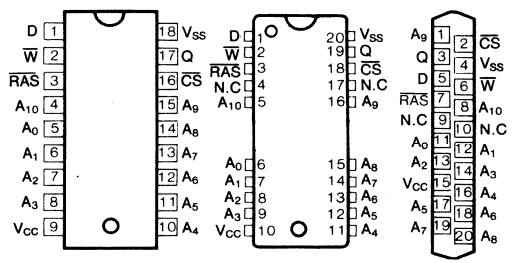
The KM41C4002A is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)

- **KM41C4002AP** • **KM41C4002AJ** • **KM41C4002AZ**



Pin Name	Pin Function
A0-A10	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, V_{CC}=5.0V±10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CS}$, Address Cycling @ t_{RC}=min)	KM41C4002A- 7	I_{CC1}	—	105	mA
	KM41C4002A- 8		—	95	mA
	KM41C4002A-10		—	85	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}, @ t_{RC}=min)	KM41C4002A- 7	I_{CC3}	—	105	mA
	KM41C4002A- 8		—	95	mA
	KM41C4002A-10		—	85	mA
Static Column Mode Current* ($\overline{RAS}$=$\overline{CS}$=V_{IL}, Address Cycling @t_{SC}=min)	KM41C4002A- 7	I_{CC4}	—	80	mA
	KM41C4002A- 8		—	70	mA
	KM41C4002A-10		—	60	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$≥V_{CC}-0.2V)		I_{CC5}	—	1	mA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @ t_{RC}=min.)	KM41C4002A- 7	I_{CC6}	—	105	mA
	KM41C4002A- 8		—	95	mA
	KM41C4002A-10		—	85	mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CS}$=V_{IL}, D_{OUT}=Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test=0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{10}, D)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$)	C_{IN2}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM41C4002A-7		KM41C4002A-8		KM41C4002A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	155		175		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3,12
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CS}$ pulse width	t_{CS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM41C4002A-7		KM41C4002A-8		KM41C4002A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CS}$ to write enable delay time	t_{CWD}	20		20		25		ns	8
$\overline{RAS}$ to write enable delay time	t_{RWD}	70		80		100		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		50		ns	8
$\overline{CS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	
Static column mode cycle time	t_{SC}	40		45		55		ns	
Static column mode read-write cycle time	t_{SRWC}	70		80		100		ns	
Access time from last write	t_{ALW}		65		75		95	ns	3,12
Output data hold time from column address	t_{AOH}	5		5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		45		50		70	ns	
Output data hold time from $\overline{W}$	t_{WOH}	0		0		0		ns	
$\overline{RAS}$ pulse width (static column mode)	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CS}$ precharge time (static column mode)	t_{CP}	10		10		10		ns	
Write address hold time reference to $\overline{RAS}$	t_{AWR}	55		60		75		ns	6
Column address hold time referenced to $\overline{RAS}$ rise	t_{AH}	5		5		10		ns	
Last write to column address delay time	t_{LWAD}	20	30	20	35	25	45	ns	
Last write to column address hold time	t_{AHLW}	65		75		95		ns	
Write command inactive time	t_{WI}	10		10		10		ns	
Write command set-up time (Test mode In)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode In)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	

TEST MODE CYCLE

(Note. 13)

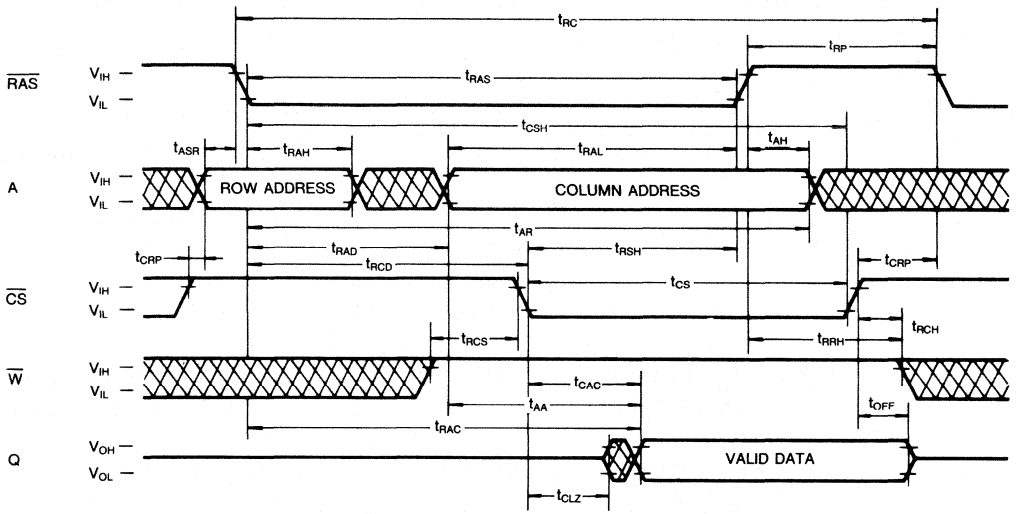
Standard Operation	Symbol	KM41C4002A-7		KM41C4002A-8		KM41C4002A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	135		155		185		ns	
Read-modify-write cycle time	t_{RWC}	160		180		215		ns	
Access time from $\overline{RAS}$	t_{RAC}		75		85		105	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		25		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		45		55	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	75	10,000	85	10,000	105	10,000	ns	
$\overline{CS}$ pulse width	t_{CS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{CS}$ hold time	t_{CSH}	75		85		105		ns	
Column Address to $\overline{RAS}$ lead time	t_{RAL}	40		45		55		ns	
$\overline{CS}$ to write enable delay	t_{CWD}	25		25		30		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	75		85		105		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	40		45		55		ns	8
Static column mode cycle time	t_{SC}	45		50		60		ns	
Static column mode read-modefy-write	t_{SRWC}	75		85		105		ns	
$\overline{RAS}$ pulse width (Static column mode)	t_{RASC}	75	100,000	85	100,000	105	100,000	ns	
Access time from last write	t_{ALW}		70		80		100	ns	3,12
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	25	100,000	25	100,000	30	100,000	ns	

NOTES

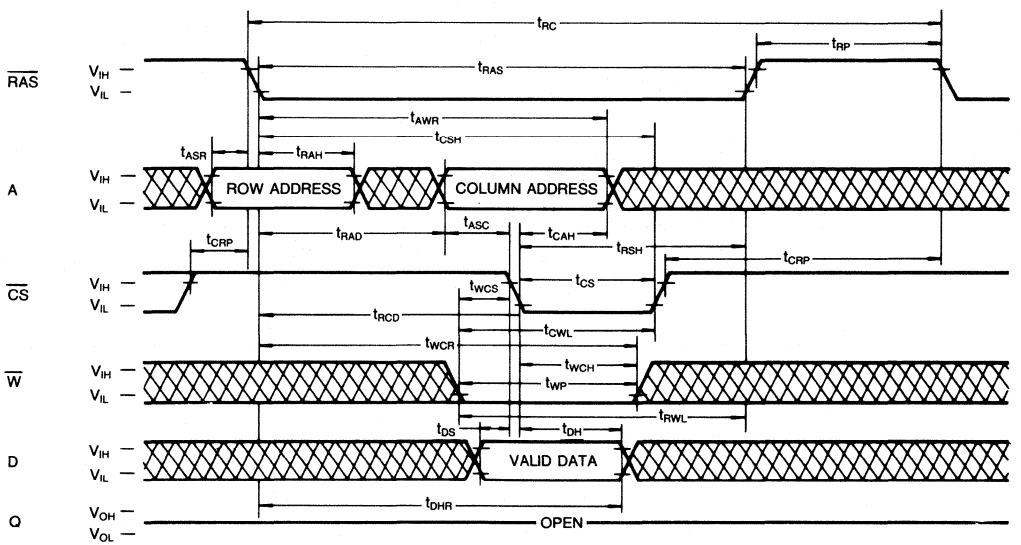
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycle before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AWR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. Operation within the $t_{LWAD(max)}$ limit insures that $t_{ALW(max)}$ can be met. $t_{LWAD(max)}$ is specified as a reference point only. t_{LWAD} is greater than the specified $t_{LWAD(max)}$ limit, then access time is controlled by t_{AA}.
13. These specifications are applied in the test mode.

TIMING DIAGRAMS

READ CYCLE



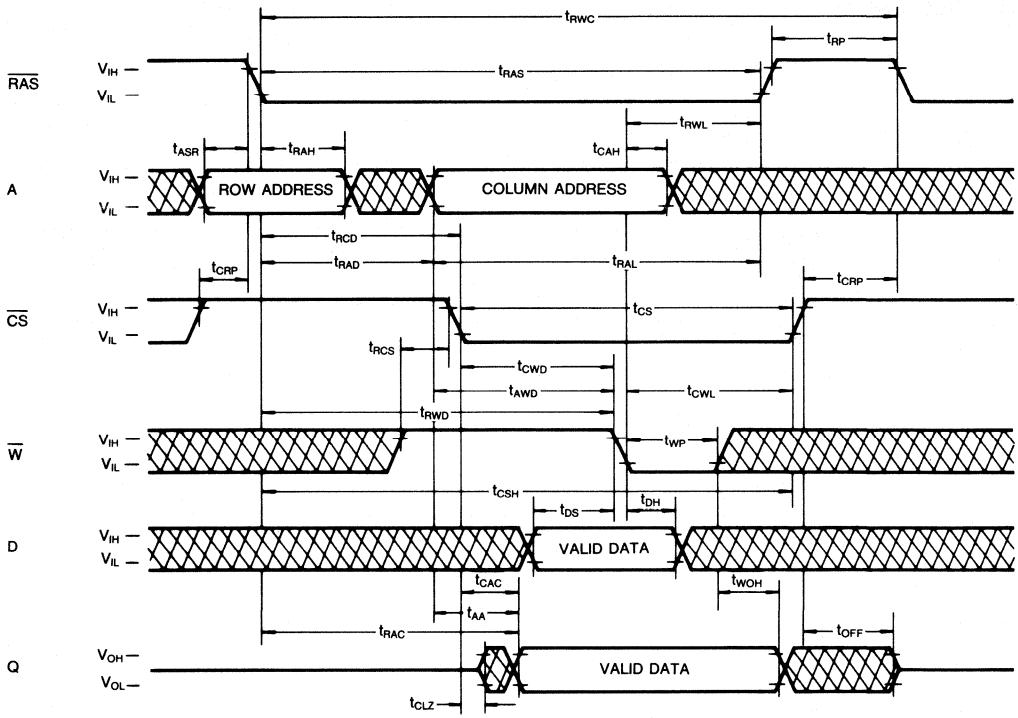
WRITE CYCLE (EARLY WRITE)



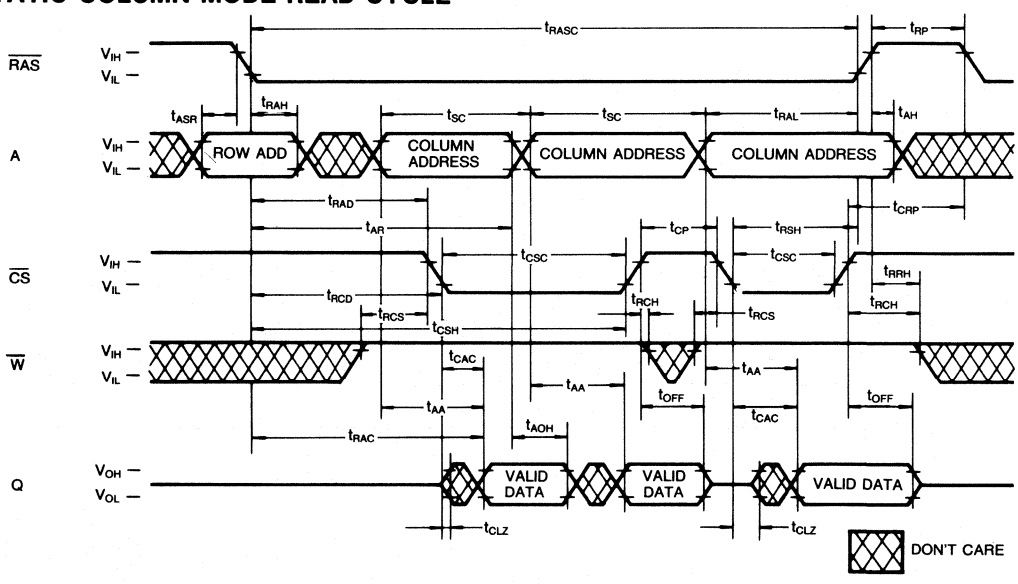
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

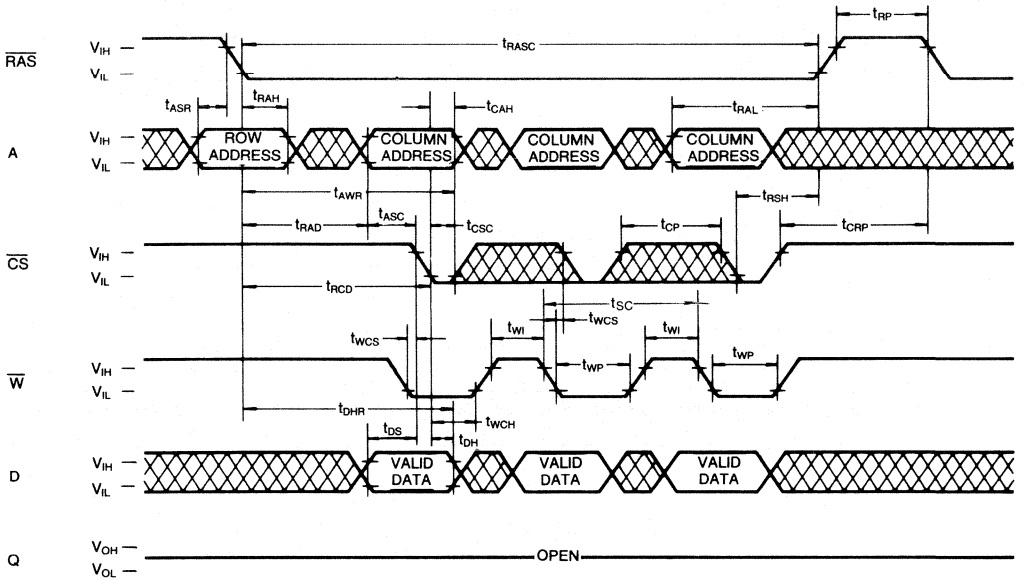


STATIC COLUMN MODE READ CYCLE

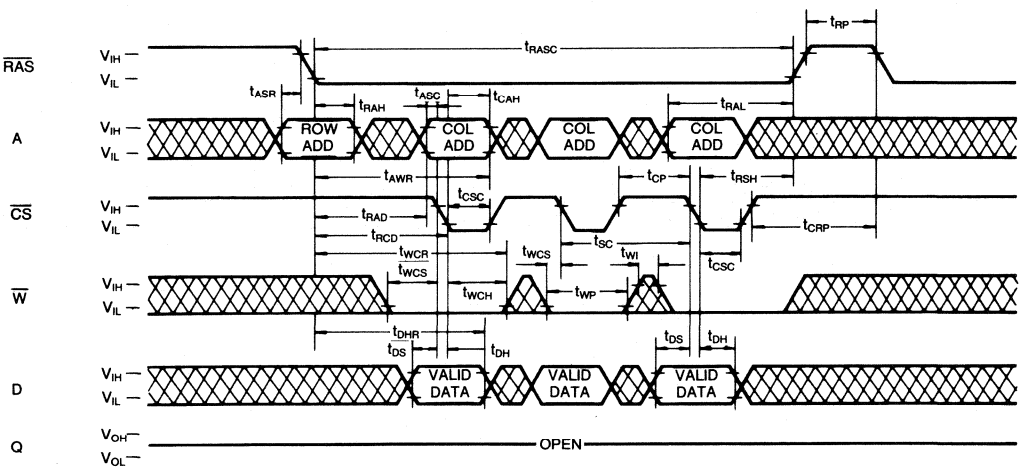


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ CONTROLLED EARLY WRITE)



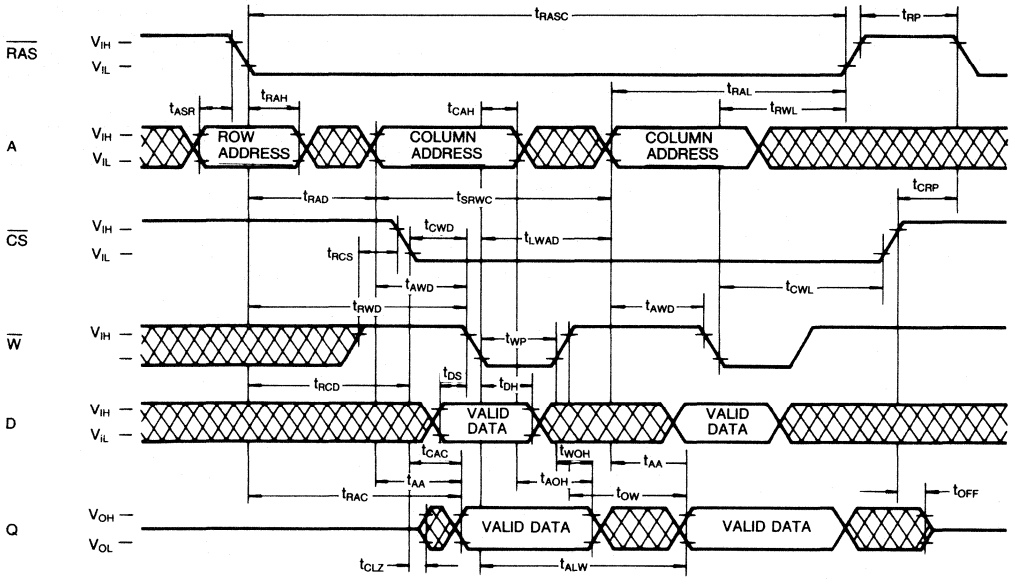
STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ CONTROLLED EARLY WRITE)



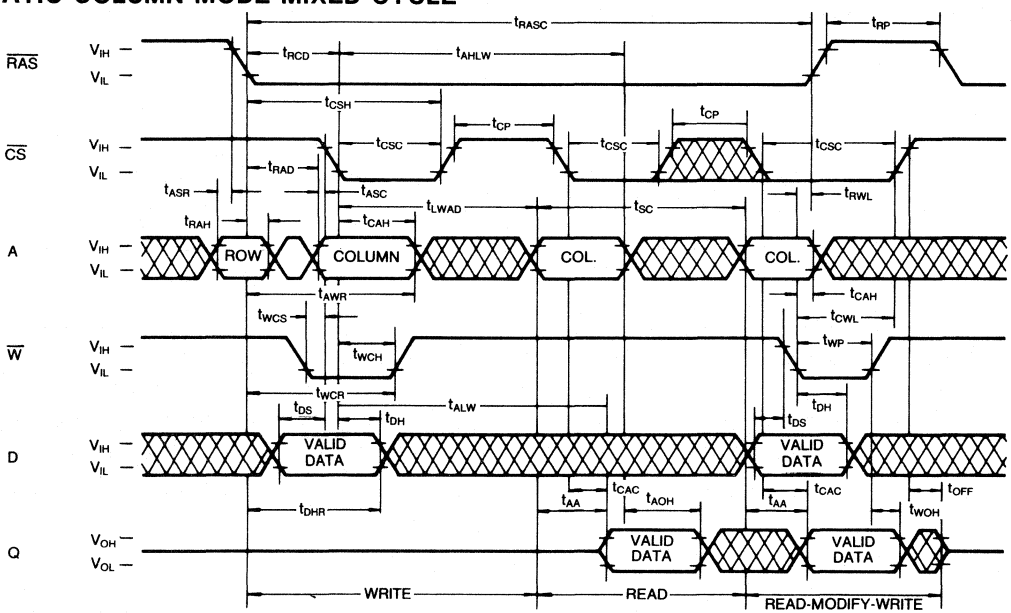
DON'T CARE

TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ-WRITE CYCLE



STATIC COLUMN MODE MIXED CYCLE

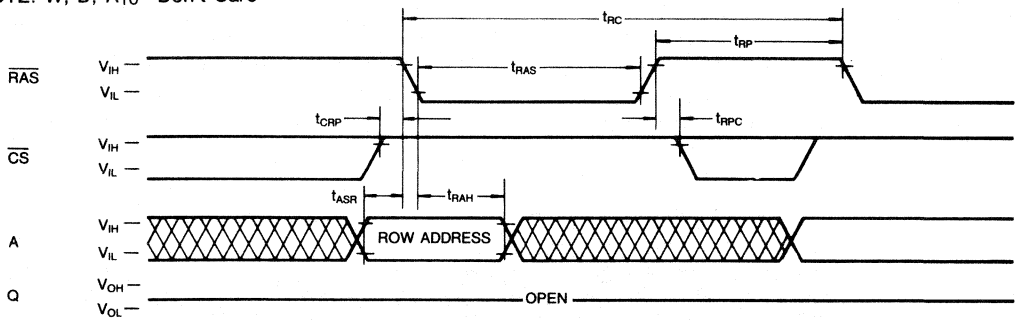


DONT'T CARE

TIMING DIAGRAMS (Continued)

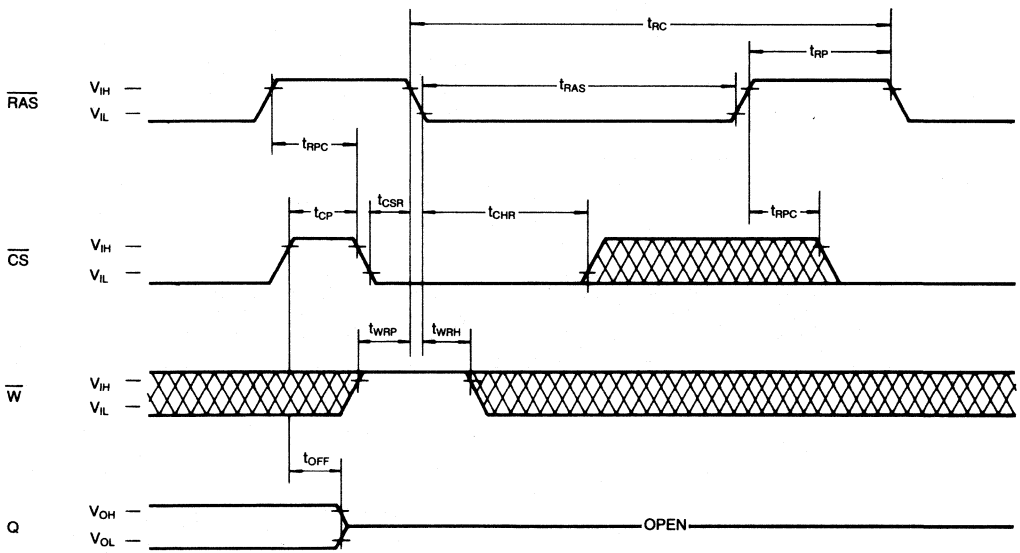
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{W}$, D, A_{10}=Don't Care



$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

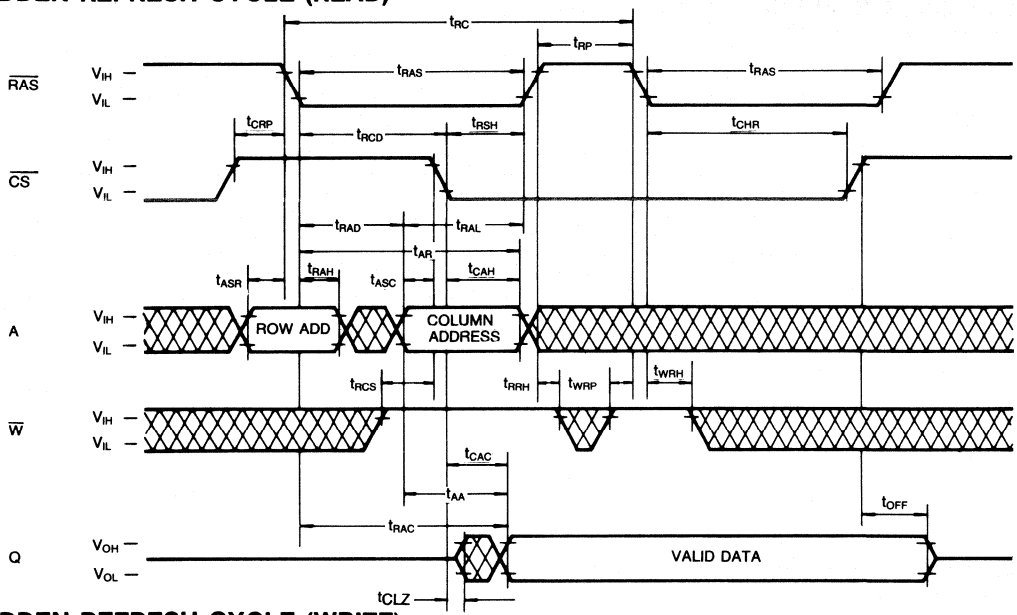
NOTE: Address=Don't Care



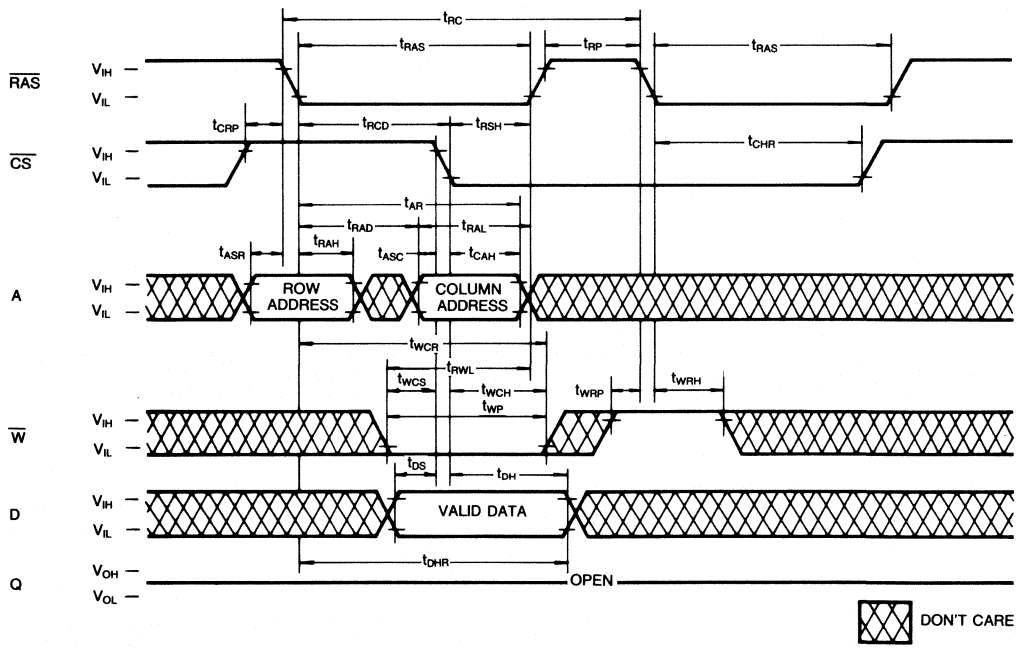
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

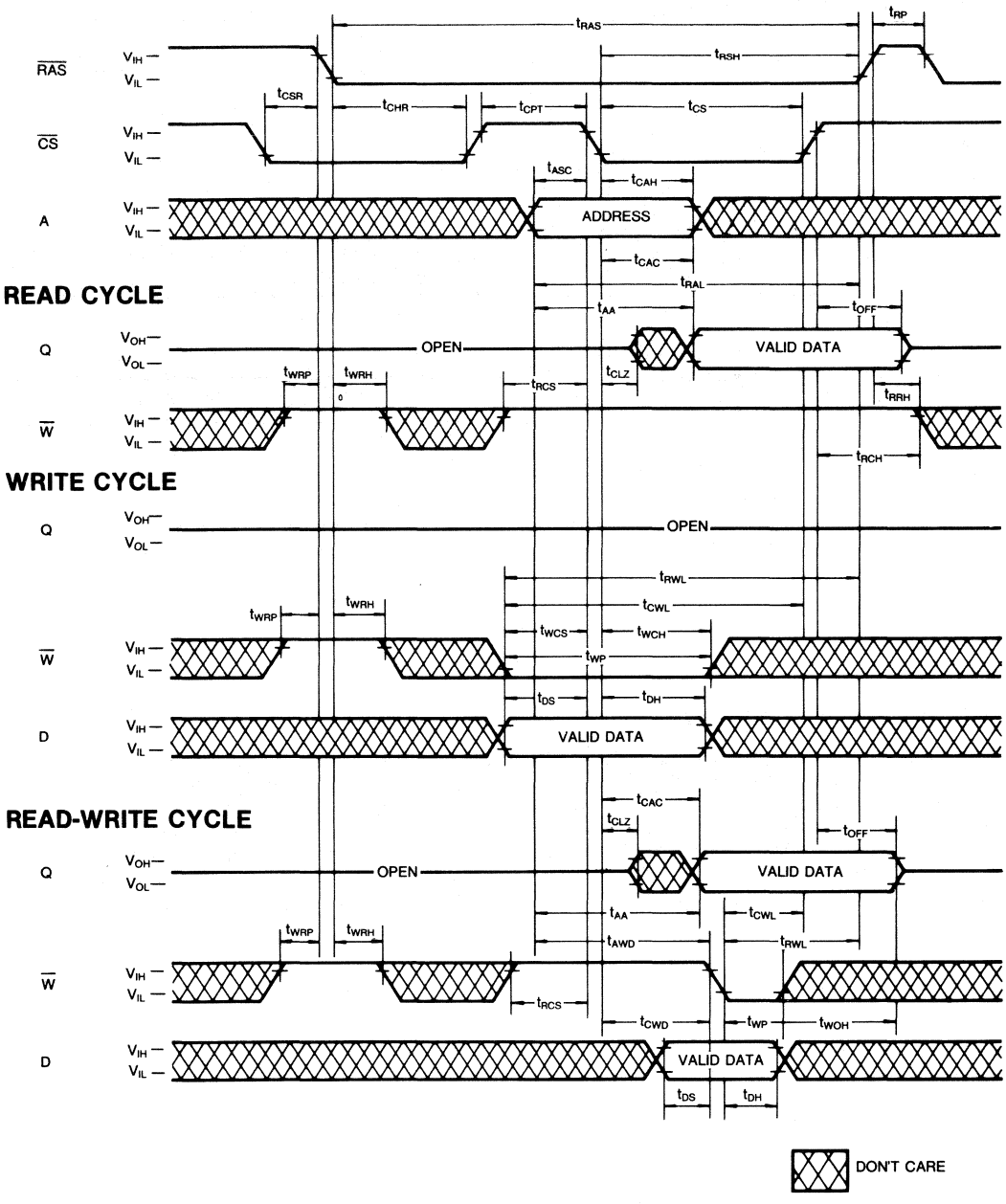


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

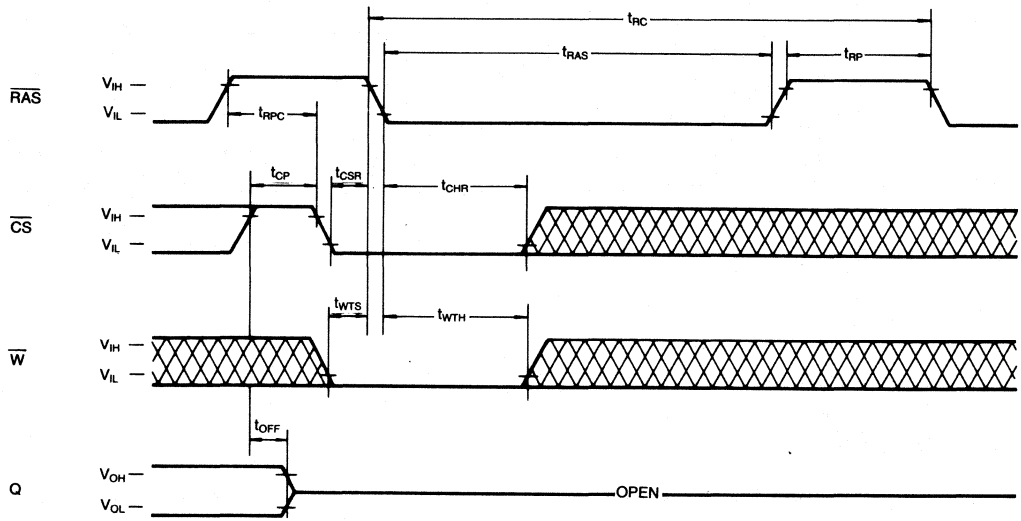
$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address=Don't Care



TEST MODE DESCRIPTION

The KM41C4002A is true RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}, A_{10C} and A_{0C} are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0" In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM. $\overline{W}$, $\overline{CS}$ Before $\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/8 in cases of N test pattern).

DEVICE OPERATIONS

Device Operation

The KM41C4002A contains 4,194,304 memory locations. Twenty-two address bits are required to address a particular memory location. Since the KM41C4002A has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the chip select input ($\overline{CS}$) and the valid row and column address inputs.

Operating of the KM41C4002A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{CS}$. This is the beginning of any KM41C4002A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths are specified by t_{RAS}(min) and t_{CS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C4002A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CS}$ and on the valid column address transition.

If $\overline{CS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM41C4002A can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C4002A has a three-state output buffer which is controlled by $\overline{CS}$. Whenever $\overline{CS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C4002A operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Static Column Mode Read, Static Column Mode Read-Modify-Write.

Hi-Z Output Static: Early Write, $\overline{RAS}$-only Refresh, Static Column Mode Write, $\overline{CS}$-Before-$\overline{RAS}$ Refresh, $\overline{CS}$-only cycle.
Indeterminate Output State: Delayed Write.

DEVICE OPERATIONS (Continued)

Refresh

The data in the KM41C4002A is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CS}$ remains high. This cycle must be repeated for each row.

$\overline{CS}$-before-$\overline{RAS}$ Refresh: The KM41C4002A has $\overline{CS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CS}$ active time and cy~ling $\overline{RAS}$. The KM41C4002A hidden refresh cycle is actually a $\overline{CS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C4002A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CS}$-before-$\overline{RAS}$ refresh is the preferred method.

Static Column Mode

Static Column Mode allows high speed read, write or read-modity-write random access to all the memory cells within a selected row. Operation within a selected row is similar to a static RAM. The read, write or readmodify-write cycles may be mixed in any order.

A Static Column mode read cycle starts as a normal cycle. Additional cells within the selected row are written by by applying a new column address while $\overline{W}=V_{IH}$ and $\overline{RAS}=V_{IL}$.

A Static Column mode write cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{RAS}=V_{IL}$ and toggiling either $\overline{W}$ or $\overline{CS}$. The data is written into the cell trigered by the latter fallin edge of $\overline{W}$ or $\overline{CS}$.

$\overline{CS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CS}$ goes high and then low again while RAS is held low, the read and write operations are enabled.

This is shown in the $\overline{CS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter. The A_{10} bit is set high internally.

Column Address—Bits A_0 through A_{10} are strobed-in by the falling edge of $\overline{CS}$ as in a normal memory cycle.

Suggested $\overline{CS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 512 times so that highs are written into the 512 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

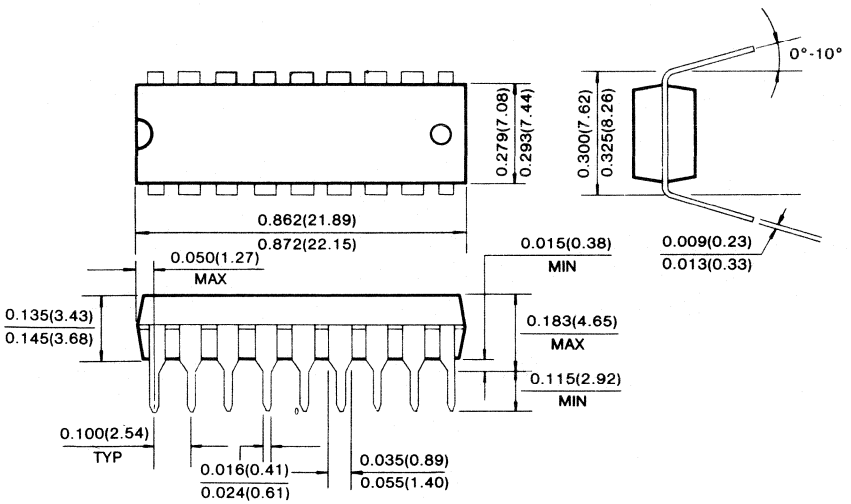
If $\overline{RAS}=V_{SS}$ during power-up, the KM41C4002A could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

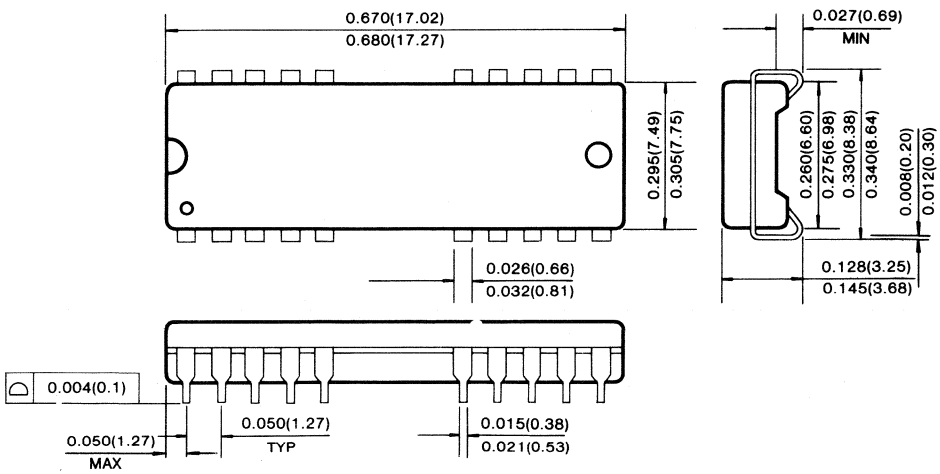
PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

Unit: Inches (Millimeters)



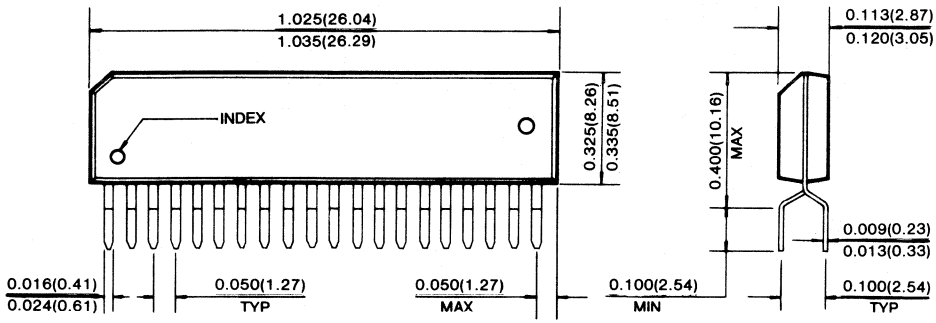
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)



4M x 1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C4000B-6	60ns	15ns	110ns
KM41C4000B-7	70ns	20ns	130ns
KM41C4000B-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode capability**
- **TTL compatible inputs and output**
- **Common I/O using early write**
- **Single +5V ± 10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in plastic DIP, SOJ, ZIP and TSOP packages**

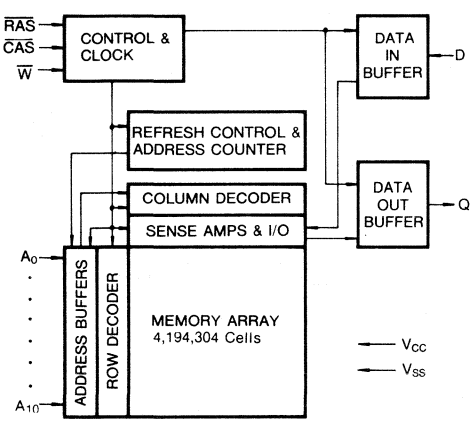
GENERAL DESCRIPTION

The Samsung KM41C4000B is a high speed CMOS 4,194,304 x 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C4000B features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

The KM41C4000B is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

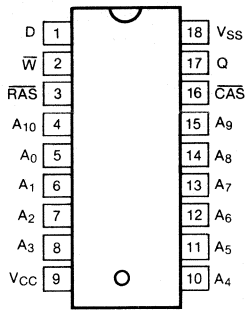


ORDERING INFORMATION

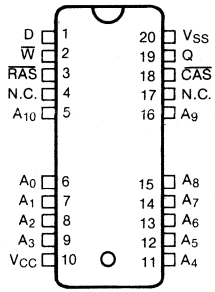
Part No.	Access Time	Package
KM41C4000BP-6	60 ns	300 mil, 18 DIP
KM41C4000BP-7	70 ns	
KM41C4000BP-8	80 ns	
KM41C4000BJ-6	60 ns	300 mil, 20 SOJ
KM41C4000BJ-7	70 ns	
KM41C4000BJ-8	80 ns	
KM41C4000BZ-6	60 ns	400 mil, 20 ZIP
KM41C4000BZ-7	70 ns	
KM41C4000BZ-8	80 ns	
KM41C4000BV-6	60 ns	20 TSOP (I) (Forward)
KM41C4000BV-7	70 ns	
KM41C4000BV-8	80 ns	
KM41C4000BVR-6	60 ns	20 TSOP (I) (Reverse)
KM41C4000BVR-7	70 ns	
KM41C4000BVR-8	80 ns	
KM41C4000BT-6	60 ns	20 TSOP (II) (Forward)
KM41C4000BT-7	70 ns	
KM41C4000BT-8	80 ns	
KM41C4000BTR-6	60 ns	20 TSOP (II) (Reverse)
KM41C4000BTR-7	70 ns	
KM41C4000BTR-8	80 ns	

PIN CONFIGURATION (Top Views)

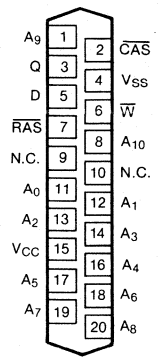
• KM41C4000BP



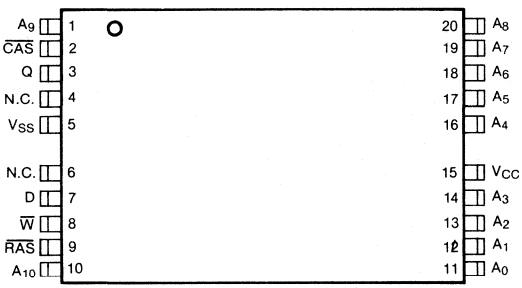
• KM41C4000BJ



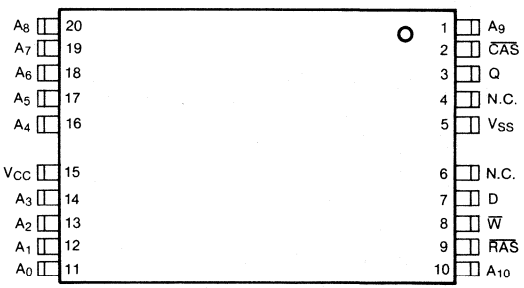
• KM41C4000BZ



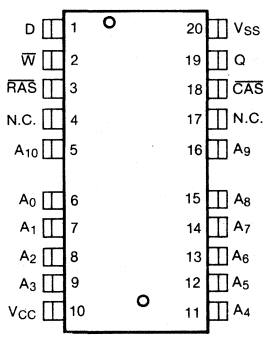
• KM41C4000BV



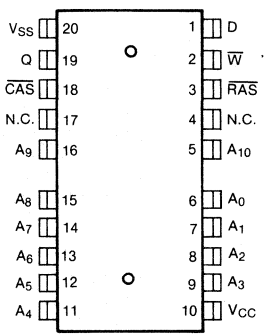
• KM41C4000BVR



• KM41C4000BT



• KM41C4000BTR



Pin Names	Pin Function
A_0-A_{10}	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM41C4000B-6	I_{CC1}	—	90	mA
	KM41C4000B-7		—	80	mA
	KM41C4000B-8		—	70	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @ t_{RC}=min.)	KM41C4000B-6	I_{CC3}	—	90	mA
	KM41C4000B-7		—	80	mA
	KM41C4000B-8		—	70	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @ t_{PC}=min.)	KM41C4000B-6	I_{CC4}	—	70	mA
	KM41C4000B-7		—	60	mA
	KM41C4000B-8		—	50	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM41C4000B-6	I_{CC6}	—	90	mA
	KM41C4000B-7		—	80	mA
	KM41C4000B-8		—	70	mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL}, D_{OUT} Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

* Note: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	—	5	pF
Input Capacitance (A_0-A_{10})	C_{IN2}	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN3}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	KM41C4000B-6		KM41C4000B-7		KM41C4000B-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	130		155		175		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

Parameter	Symbol	KM41C4000B-6		KM41C4000B-7		KM41C4000B-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (1,024 cycles)	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	15		20		20		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	60		70		80		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	30		35		40		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	60		70		75		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
Write command set-up time (test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ cycle)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ cycle)	t_{WRH}	10		10		10		ns	

TEST MODE CYCLE

(Note. 12)

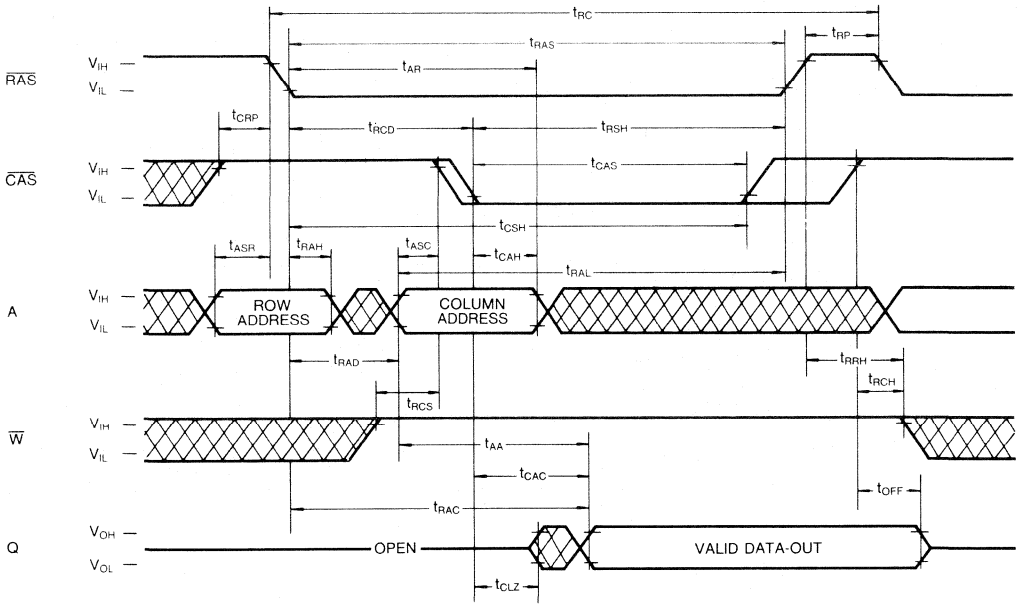
Parameter	Symbol	KM41C4000B-6		KM41C4000B-7		KM41C4000B-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	135		160		180		ns	
Access time from $\overline{RAS}$	t_{RAC}		65		75		85	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,10
$\overline{RAS}$ pulse width	t_{RAS}	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		45		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	20		25		25		ns	7
$\overline{RAS}$ to write enable delay	t_{RWD}	65		75		85		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		45		ns	7
Fast mode cycle time	t_{PC}	45		50		55		ns	
Fast page mode read-modefy-write	t_{PRWC}	65		75		80		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3

NOTES

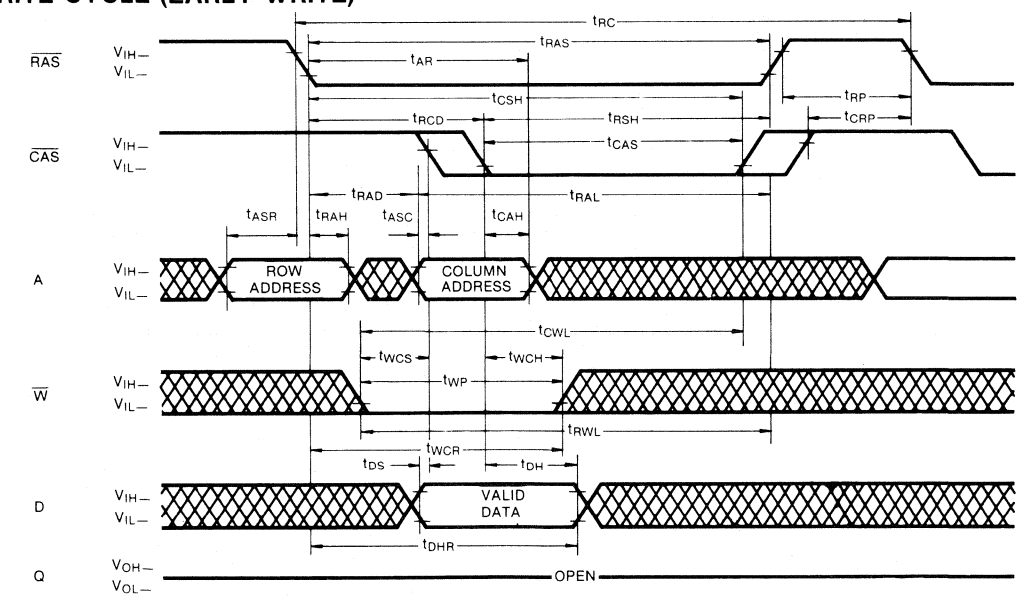
1. An initial pause of 200μs is required after power up followed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only Refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF(max)}$ and $t_{OEZ(max)}$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

TIMING DIAGRAMS

READ CYCLE



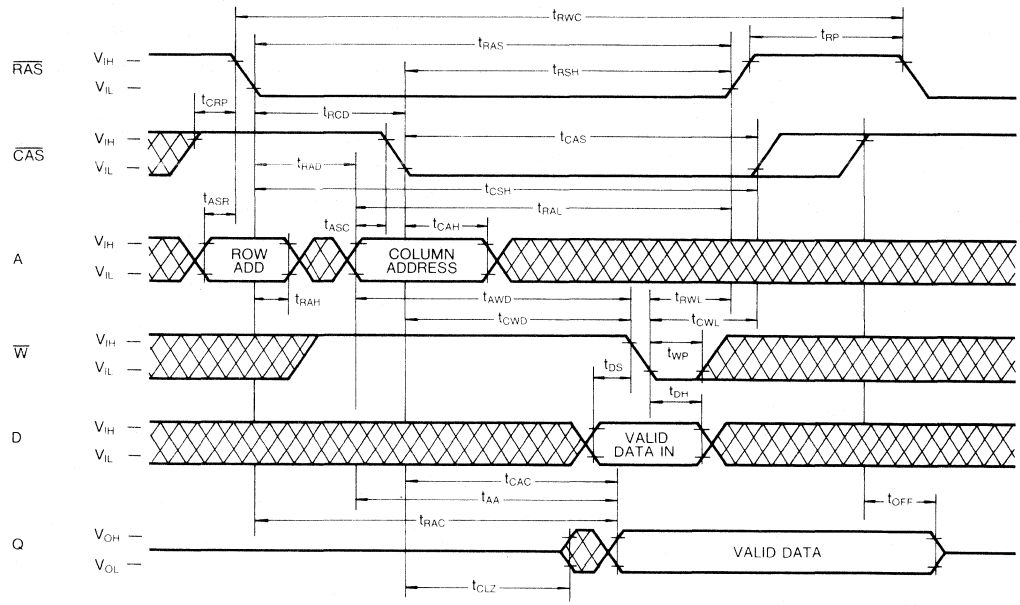
WRITE CYCLE (EARLY WRITE)



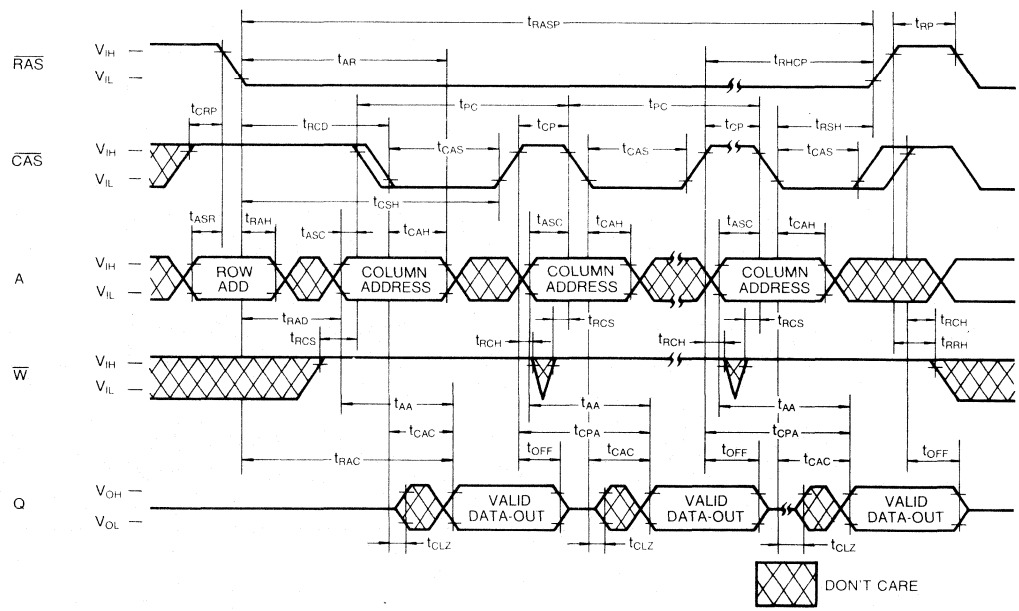
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

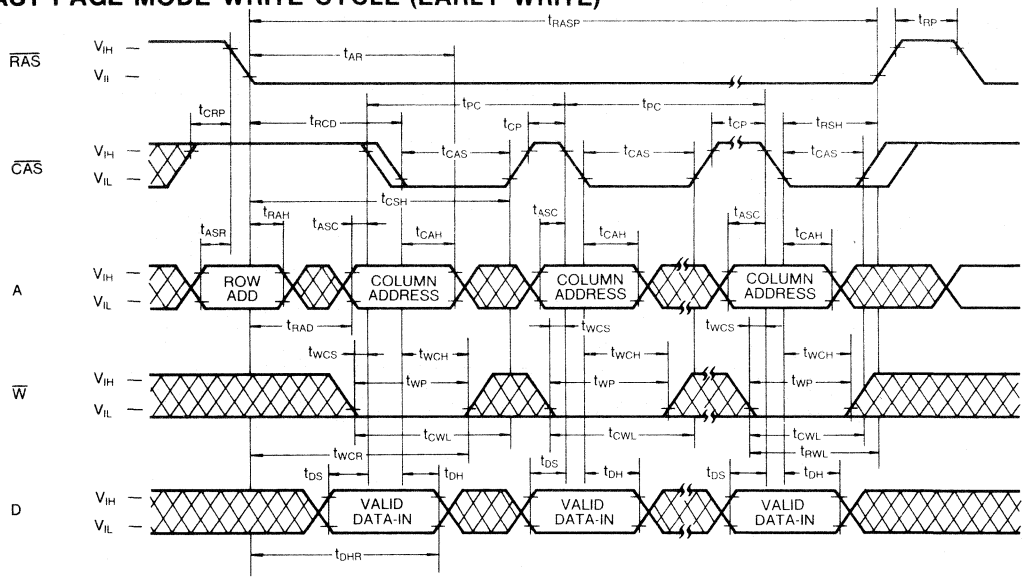


FAST PAGE MODE READ CYCLE

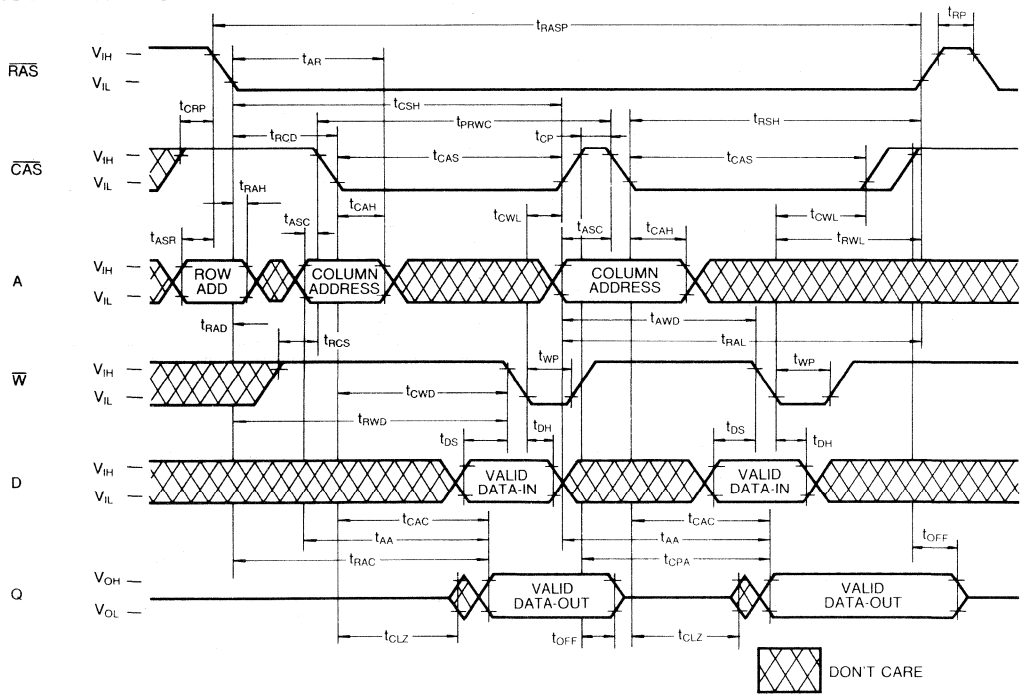


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



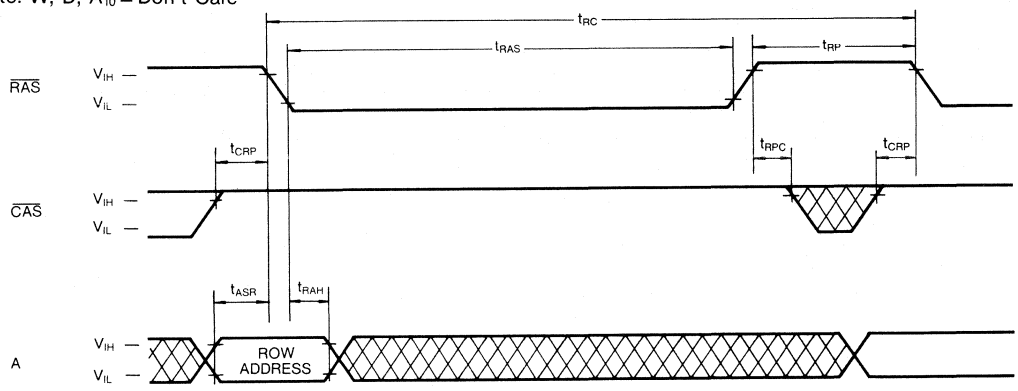
FAST PAGE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

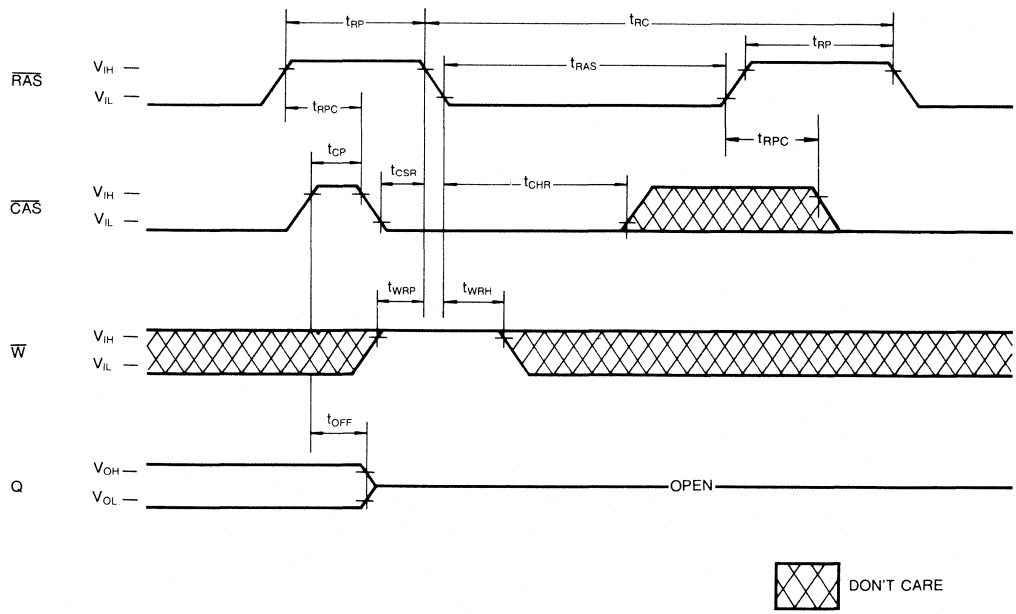
$\overline{RAS}$ ONLY REFRESH CYCLE

Note: $\overline{W}$, D, A_{10} = Don't Care



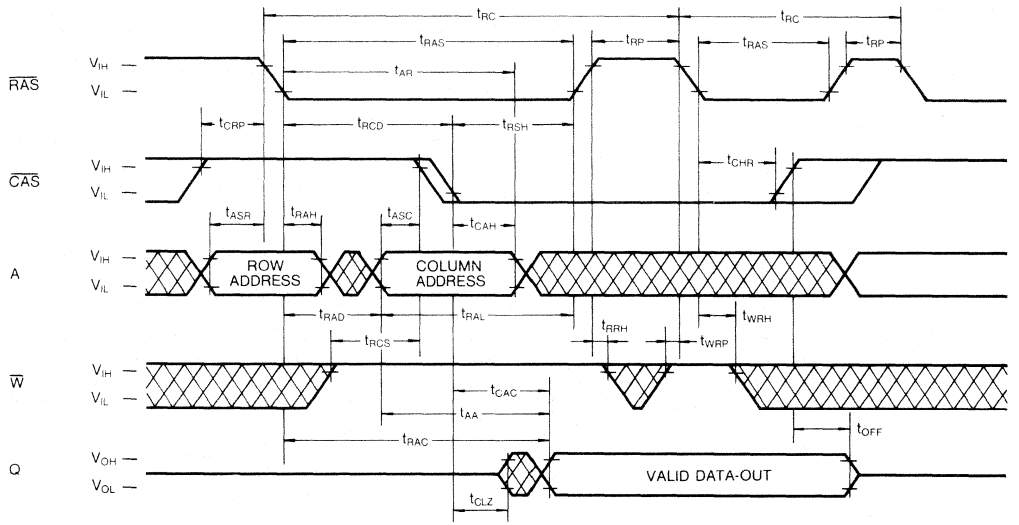
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: Address = Don't Care

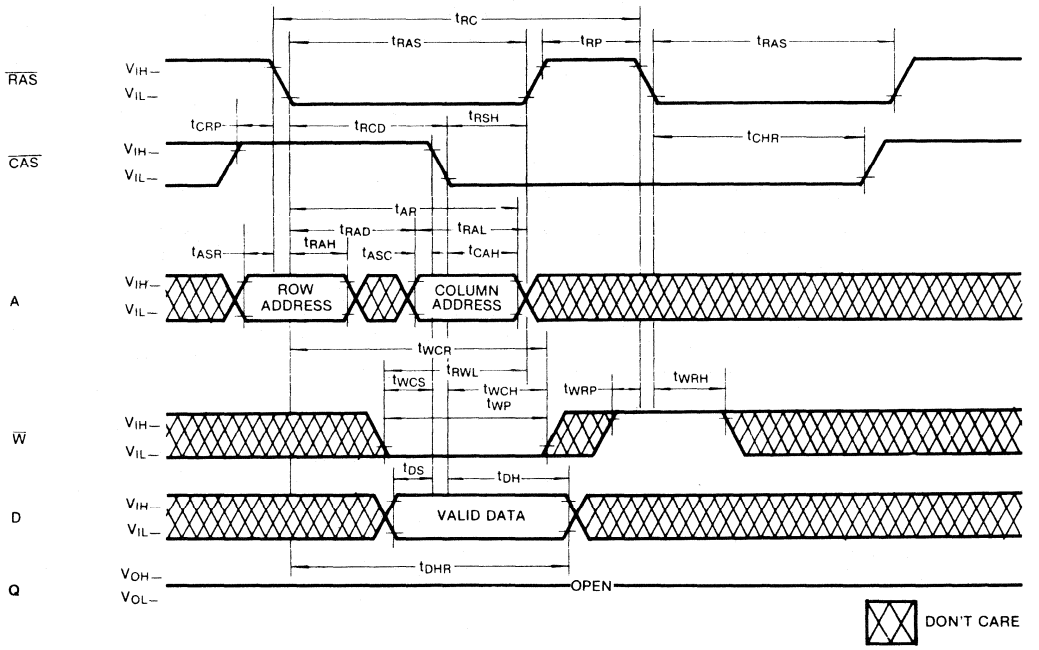


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

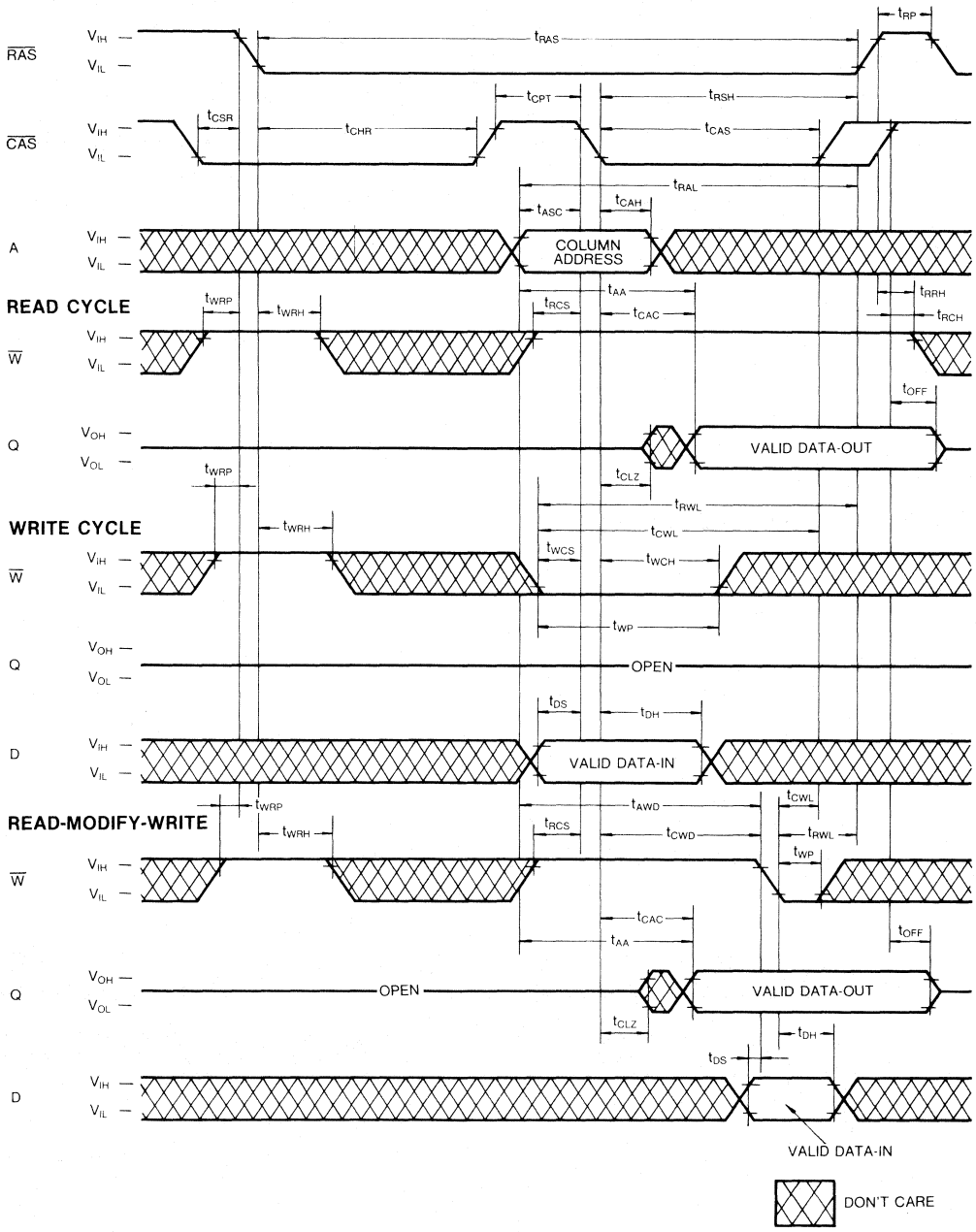


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

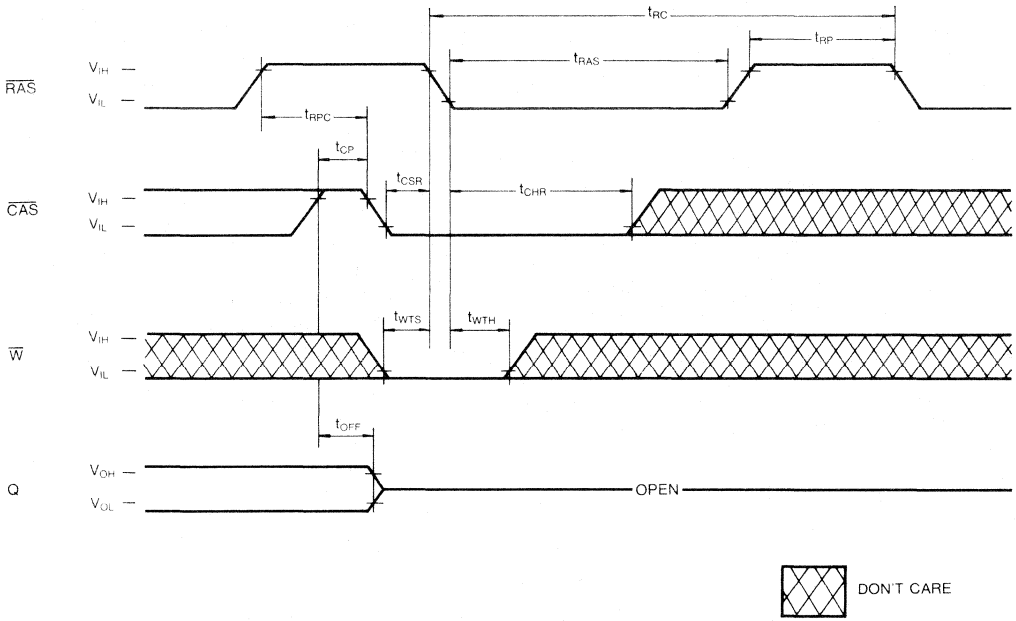
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: D, Address: Don't Care



TEST MODE DESCRIPTION

The KM41C4000B is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode," data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 and A_{10} are not used. If, upon reading, all bits are equal (all "1" or "0"s) the Q pin indicates a "1."
If they were not equal, the Q pin would indicate a "0."

In "Test Mode," the 4M DRAM can be tested as if it were a 512K DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode." And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode." The "Test Mode" function reduces test time (1/8 in cases of N test pattern).

DEVICE OPERATIONS

The KM41C4000B contains 4,194,304 memory locations. Twenty-two address bits are required to address a particular memory location. Since the KM41C4000B has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM41C4000B begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C4000B cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C4000B begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41C4000B can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. The cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C4000B has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}), the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C4000B operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

DEVICE OPERATION (Continued)

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C4000B is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C4000B has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C4000B hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C4000B by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM41C4000B has Fast page mode capability. Fast page mode memory cycles provides faster access and lower power dissipation than normal memory cycles. In Fast page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page. Up to 2048 memory cells can be accessed with the same row address.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter. This A_{10} bit is set high interally.

Column Address — Bits A_0 through A_{10} are strobed-in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested CAS-before-RAS Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM41C4000B could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

DEVICE OPERATION (Continued)

An initial pause of 200 μsec is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. Eight initialization cycles are also required after any 16 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41C4000B inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C4000B input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

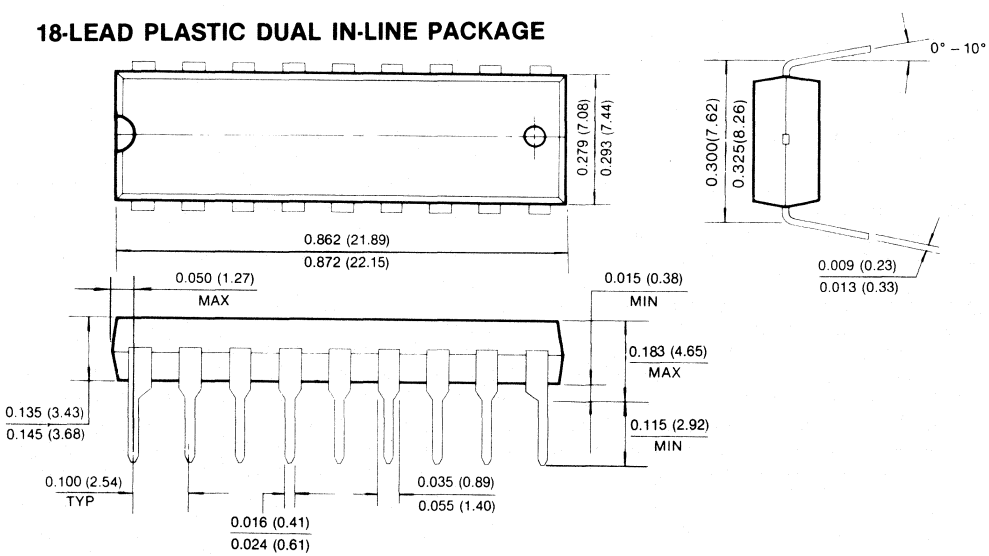
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM41C4000B using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C4000B and they supply much of the current used by the KM41C4000B during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

Units: Inches (Millimeters)

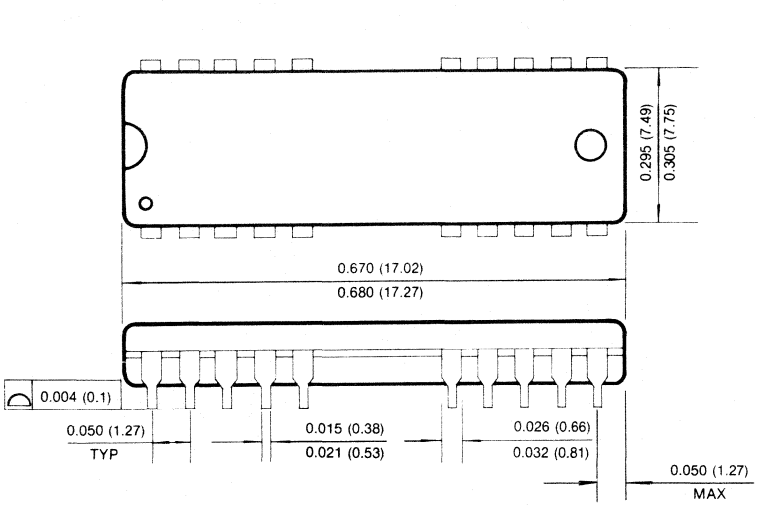
18-LEAD PLASTIC DUAL IN-LINE PACKAGE



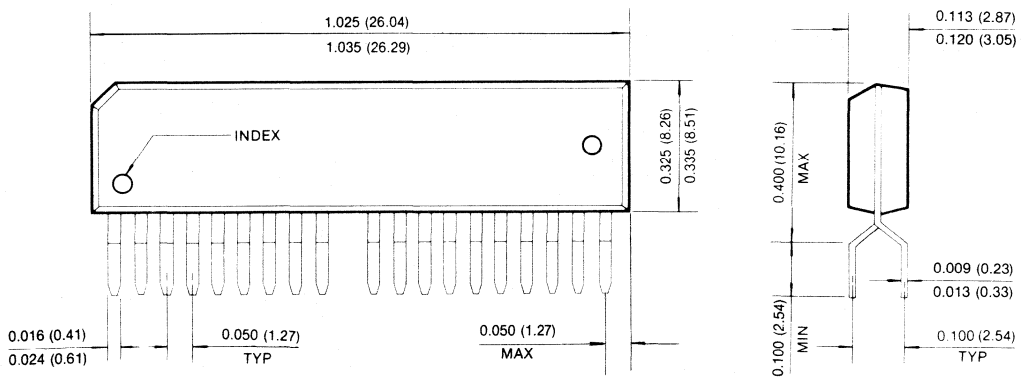
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



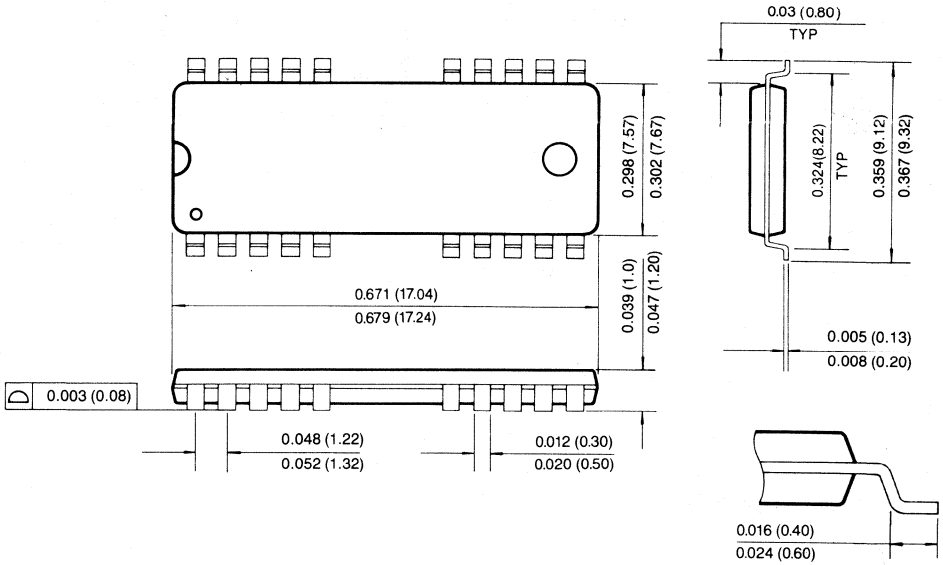
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



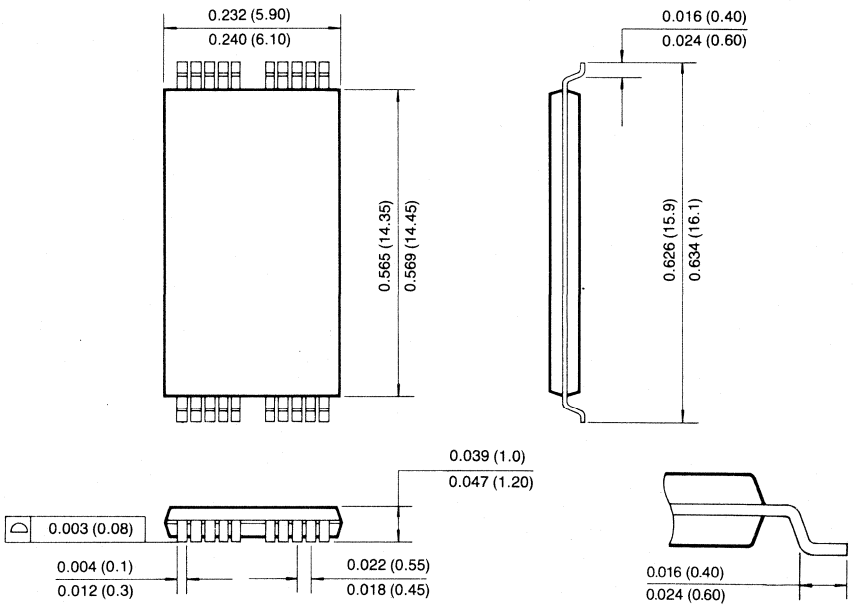
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (I) (Forward and Reverse Type)



1M×4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C1000A- 7	70ns	20ns	130ns
KM44C1000A- 8	80ns	20ns	150ns
KM44C1000A-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8-bit fase parallel test mode capability**
- **TTL compatible inputs and output**
- **Early Write or output enable controlled write**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, DIP, ZIP**

GENERAL DESCRIPTION

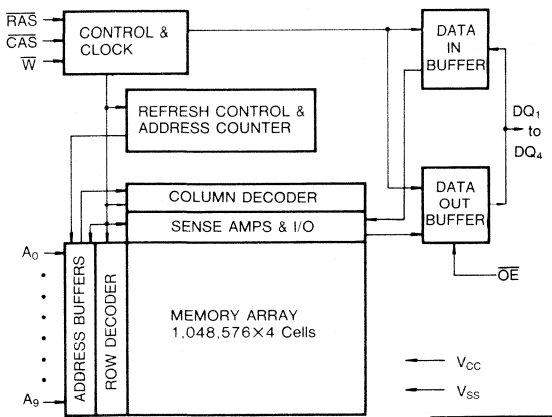
The Samsung KM44C1000A is a high speed CMOS 1,048,576 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C1000A features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

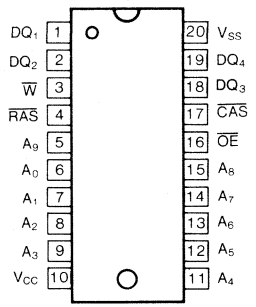
The KM44C1000A is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

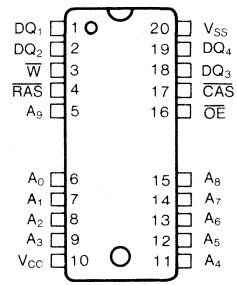


PIN CONFIGURATION (Top Views)

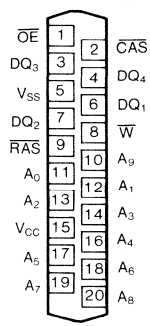
- **KM44C1000AP**



- **KM44C1000AJ**



- **KM44C1000AZ**



Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ_{1-4}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, V_{CC}=5.0V±10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM44C1000A- 7	I_{CC1}	—	105	mA
	KM44C1000A- 8		—	95	mA
	KM44C1000A-10		—	85	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min.)	KM44C1000A- 7	I_{CC3}	—	105	mA
	KM44C1000A- 8		—	95	mA
	KM44C1000A-10		—	85	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling @ t_{PC}=min.)	KM44C1000A- 7	I_{CC4}	—	80	mA
	KM44C1000A- 8		—	70	mA
	KM44C1000A-10		—	60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=W≥V_{CC}-0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM44C1000A- 7	I_{CC6}	—	105	mA
	KM44C1000A- 8		—	95	mA
	KM44C1000A-10		—	85	mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL}, Dout Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test=0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0 \leq V_{OUT} \leq 5.5V$)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4} Address can be changed maximum once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM44C1000A-7		KM44C1000A-8		KM44C1000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	185		205		245		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM44C1000A-7		KM44C1000A-8		KM44C1000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to write enable delay	t_{CWD}	50		50		60		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	100		110		135		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	65		70		85		ns	8
$\overline{CAS}$ setup time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
FAst Page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	45		45		55		ns	
Fast page modered-modify-write	t_{PRWC}	105		105		125		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		20		25		ns	
Output buffer tum off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

TEST MODE CYCLE

(Note. 12)

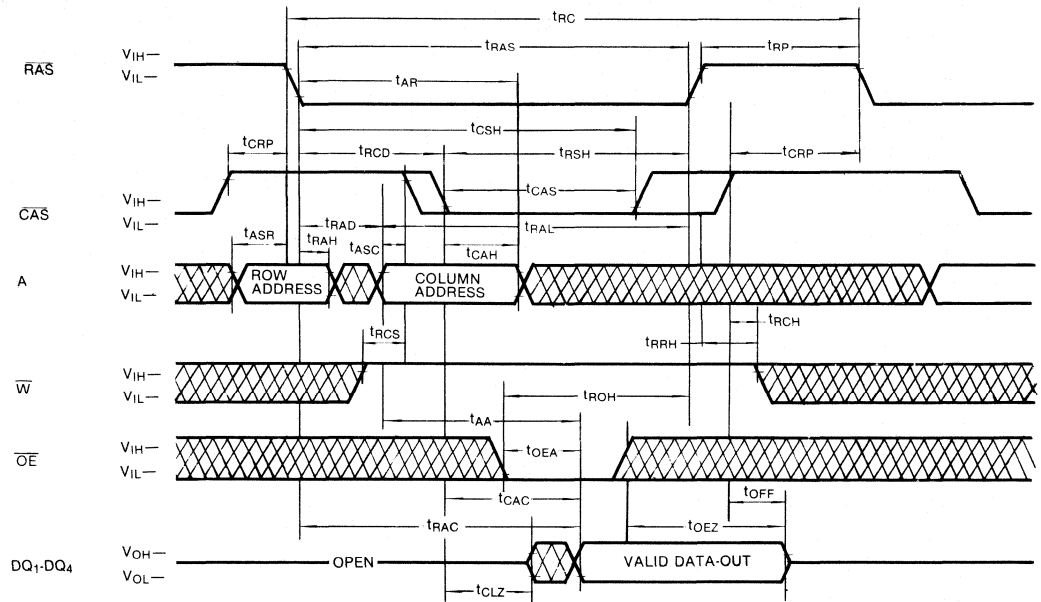
Standard Operation	Symbol	KM44C1000A-7		KM44C1000A-8		KM44C1000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	135		155		185		ns	
Read-modify-write cycle time	t_{RWC}	190		210		250		ns	
Access time from $\overline{RAS}$	t_{RAC}		75		85		105	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		25		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		45		55	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	75	10,000	85	10,000	105	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{CAS}$ hold time	t_{CSH}	75		85		105		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		45		55		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	55		55		65		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	105		115		140		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	70		75		90		ns	8
Fast mode cycle time	t_{PC}	55		55		65		ns	
Fast page mode read-modefy-write	t_{PRWC}	110		110		130		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	75	200,000	85	200,000	105	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		50		60	ns	3
$\overline{OE}$ access time	t_{OEA}		25		25		30	ns	
$\overline{OE}$ to data delay	t_{OED}	25		25		30		ns	
$\overline{OE}$ command hold time	t_{OEH}	25		25		30		ns	

NOTES

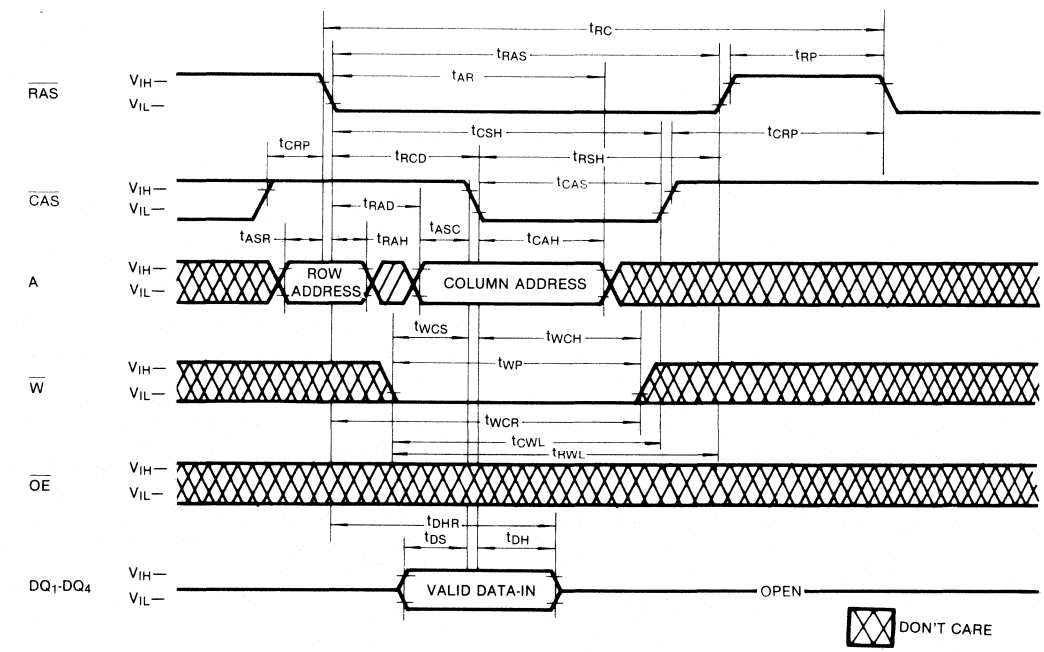
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.

TIMING DIAGRAMS

READ CYCLE

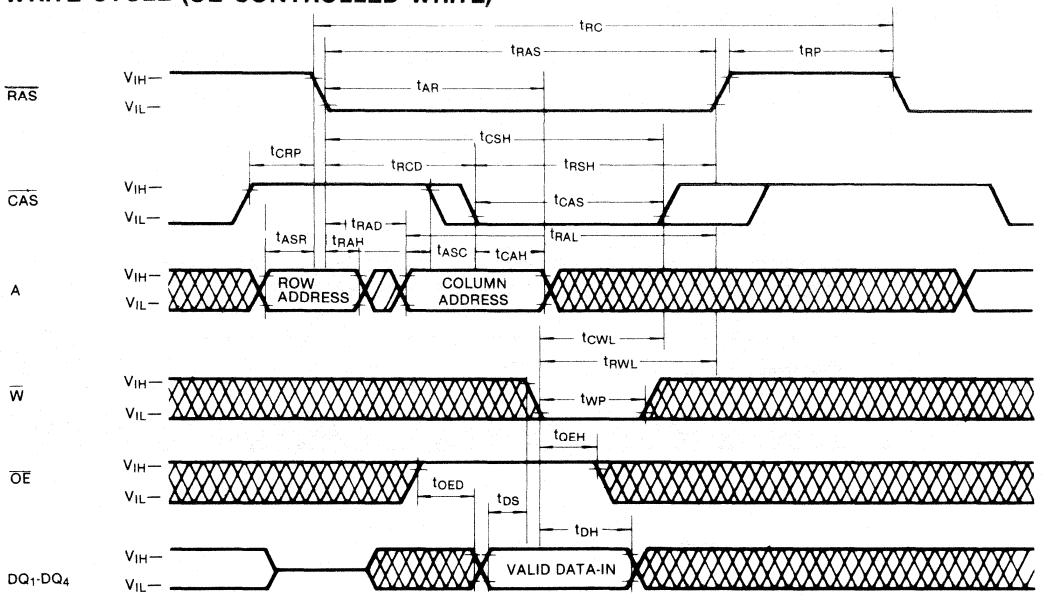


WRITE CYCLE (EARLY WRITE)

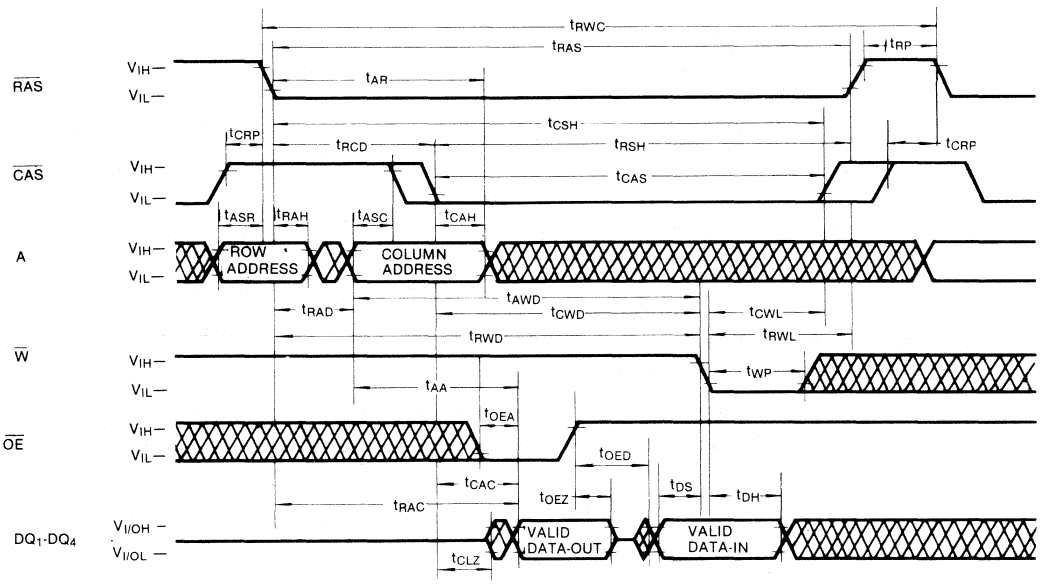


TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



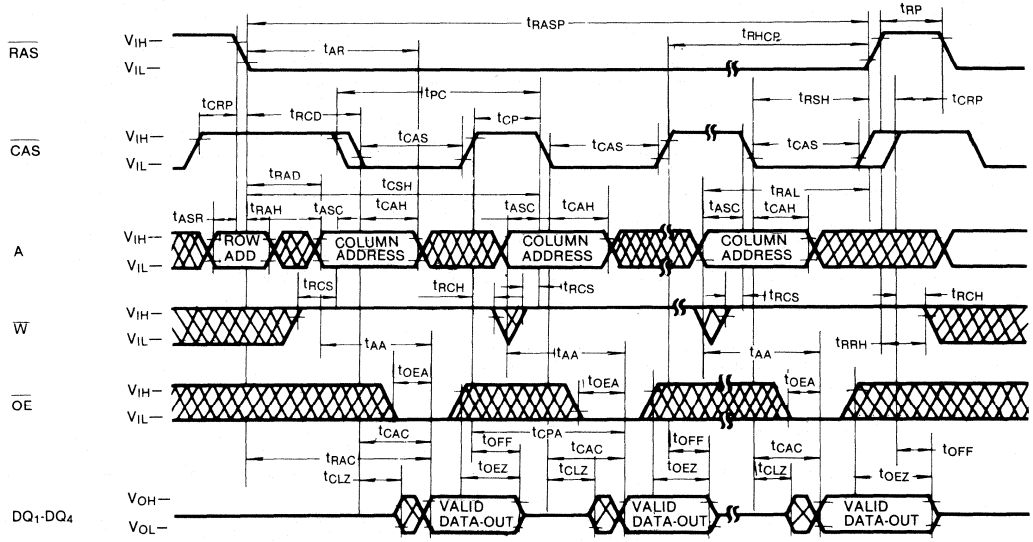
READ-MODIFY-WRITE CYCLE



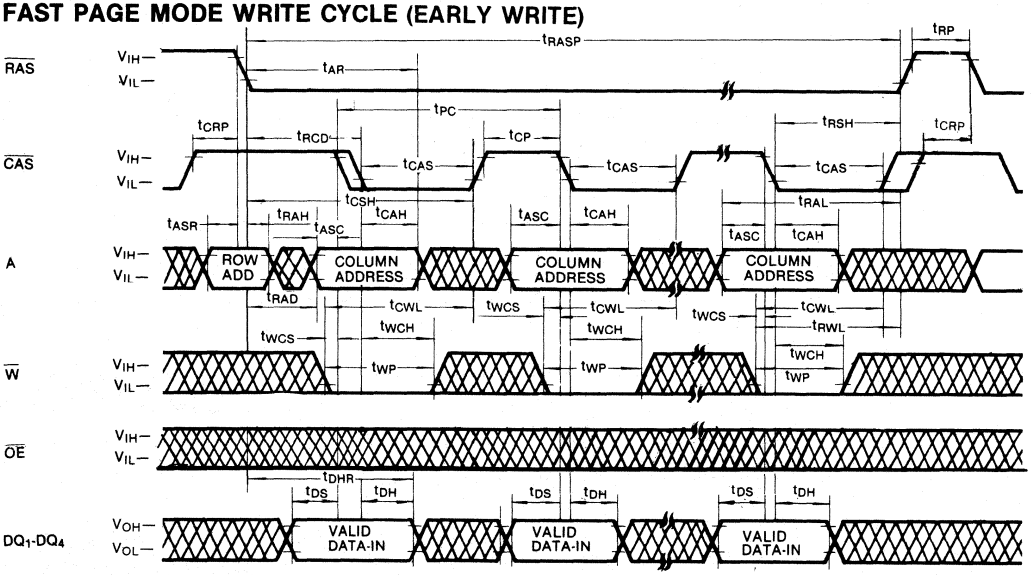
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



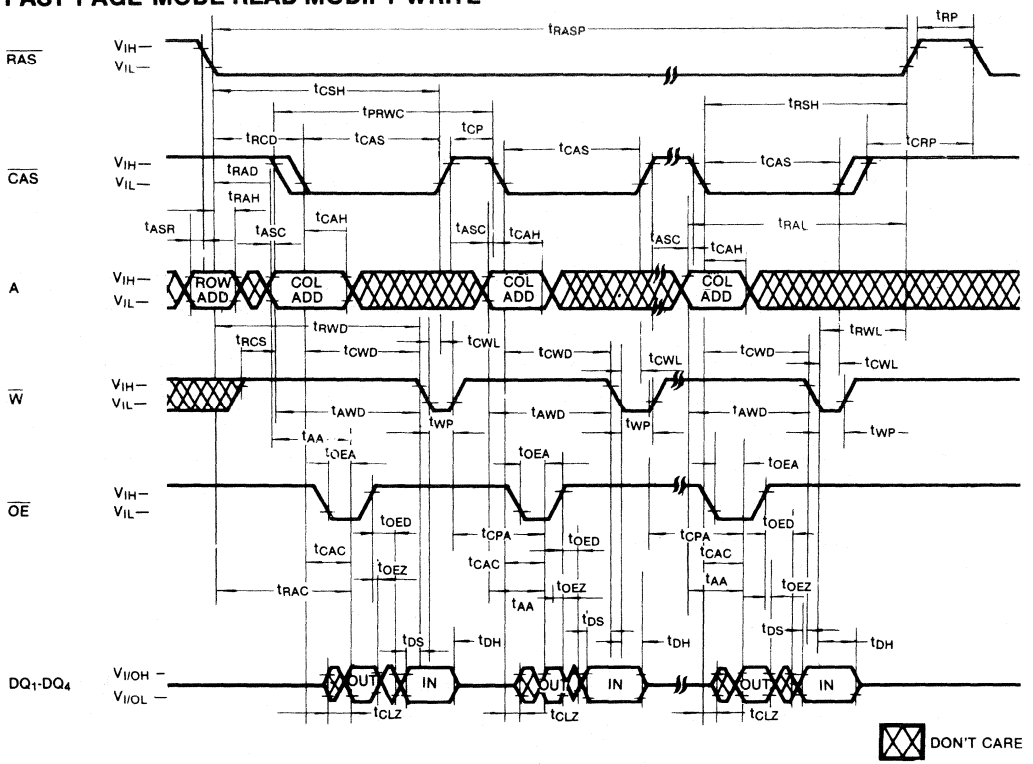
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



DON'T CARE

TIMING DIAGRAMS (Continued)

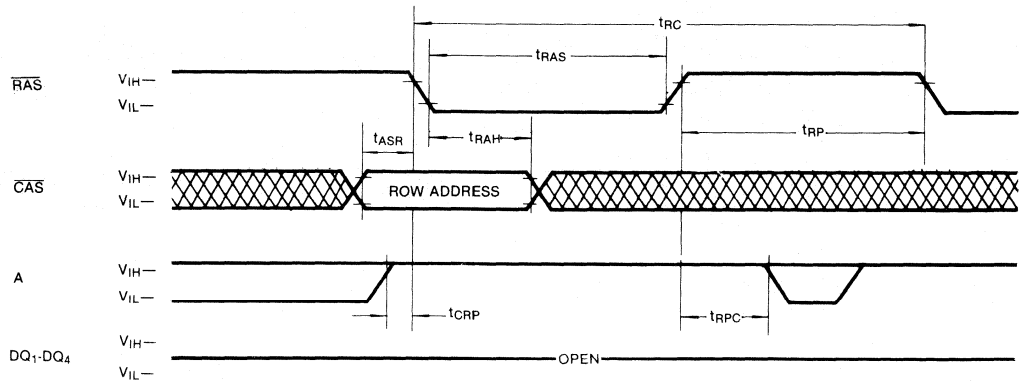
FAST PAGE MODE READ-MODIFY-WRITE



TIMING DIAGRAMS (Continued)

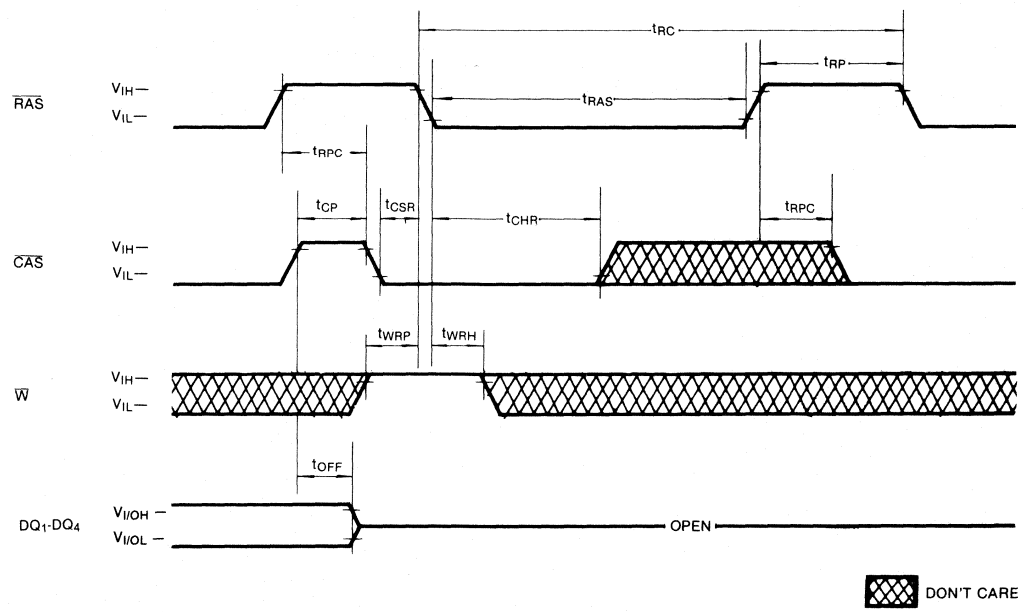
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



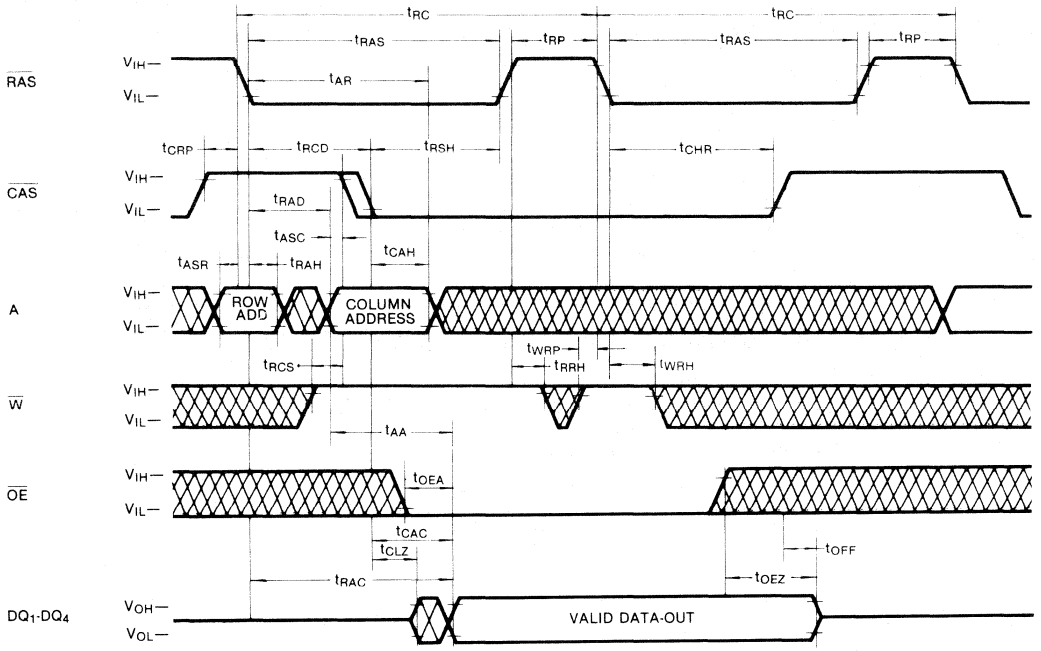
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{OE}$, Address = Don't Care

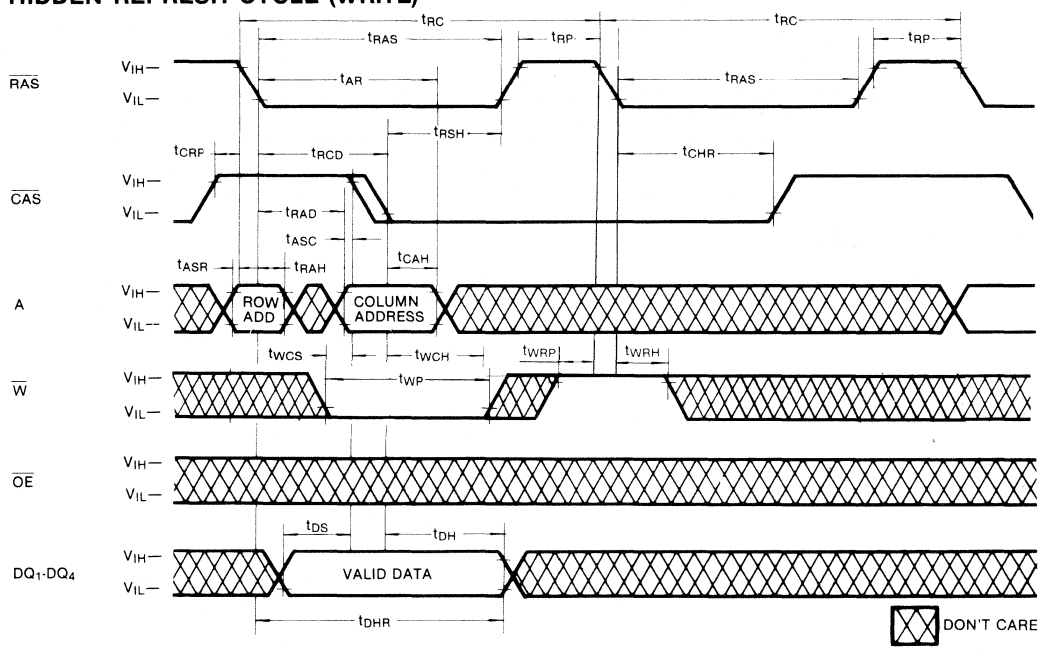


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

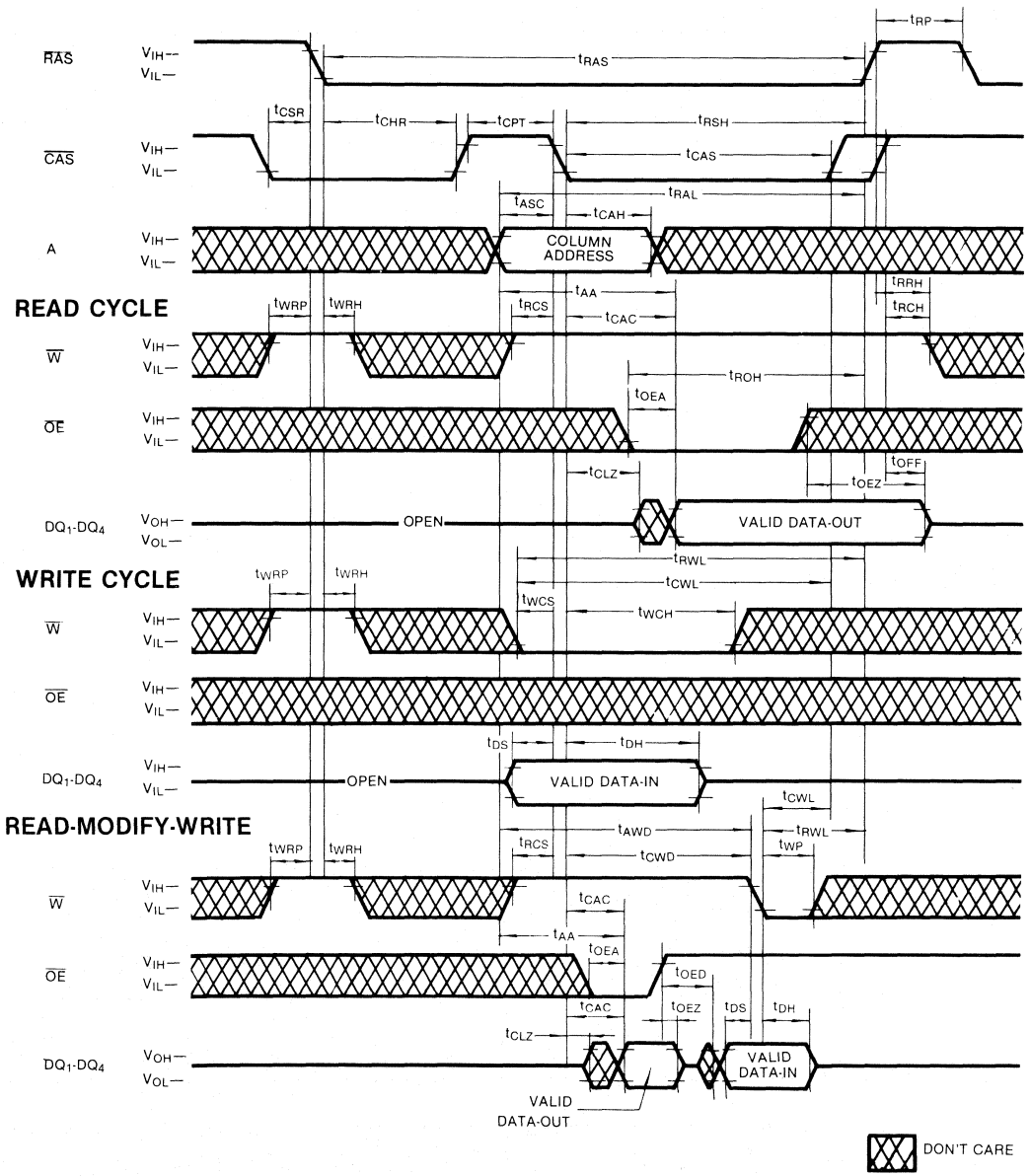


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

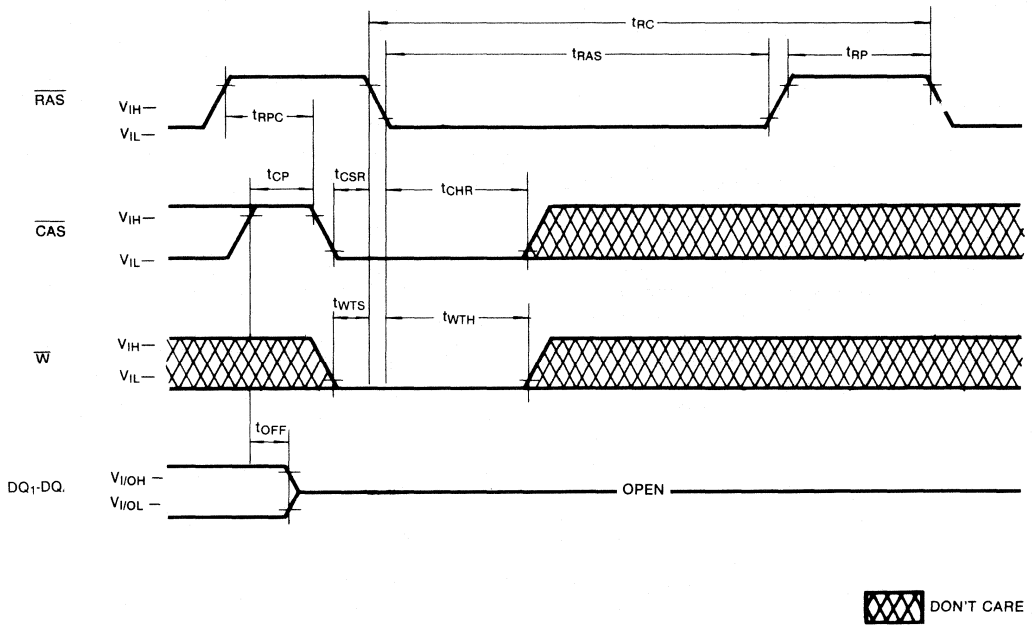
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: $\overline{OE}$, Address=Don't Care



TEST MODE DESCRIPTION

The KM44C1000A is the RAM organized 1,048,576 words by 4 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DARM. $\overline{W}$, $\overline{CAS}$-Before-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM44C1000A contains 4,194,304 memory locations. Twenty address bits are required to address a particular memory location. Since the KM44C1000A has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM44C1000A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C1000A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1000A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM44C1000A can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44C1000A has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C1000A operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle. $\overline{OE}$ controlled write.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM44C1000A is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16 ms. There are several ways to accomplish this.

DEVICE OPERATION (Continued)

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with RAS while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C1000A has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuity is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C1000A hidden refresh cycle is actually a $\overline{CAS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1000A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general RAS-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM44C1000A has Fast Page mode capability. Fast Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In Fast Page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A Fast Page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row address for the same page. Up to 2048 memory cells can be accessed with the same row address.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter.

Column Address—Bits A_0 through A_9 are strobedin by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

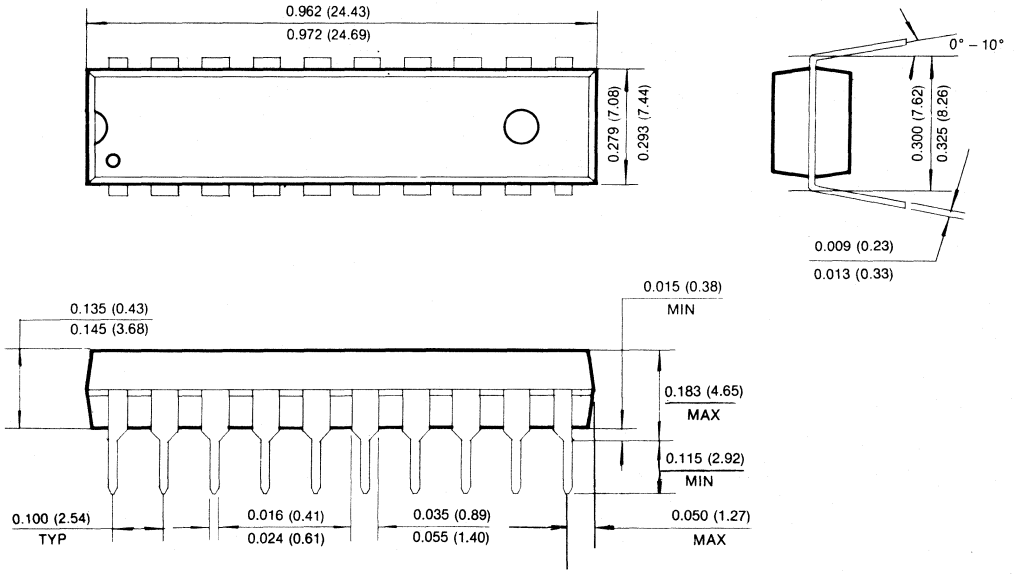
Power-up

If $\overline{RAS}=V_{SS}$ during power-up, the KM44C1000A could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

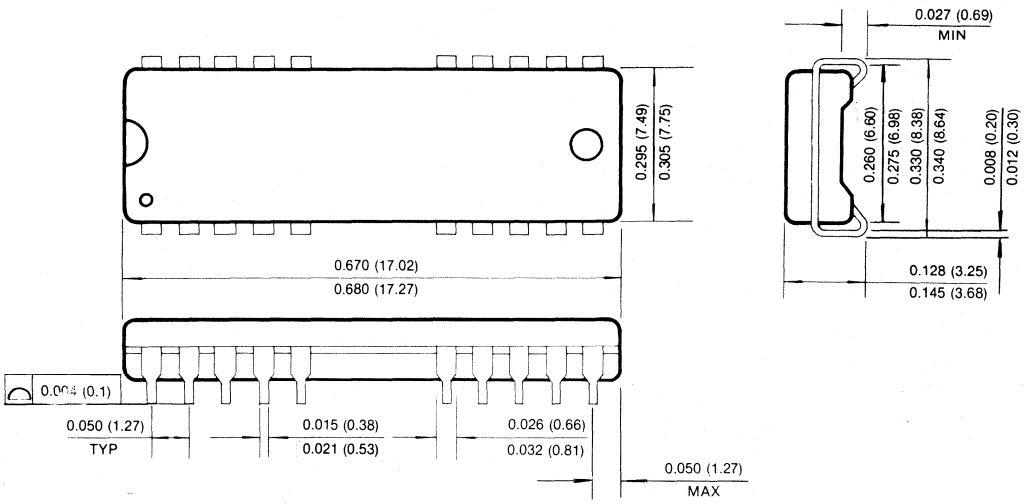
An initial pause of 200μs is required power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE



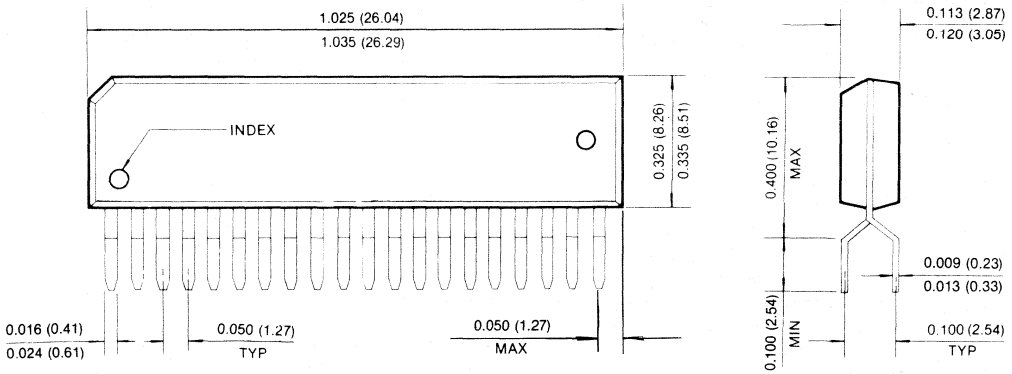
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)



2

1M×4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C1000AL- 7	70ns	20ns	130ns
KM44C1000AL- 8	80ns	20ns	150ns
KM44C1000AL-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8-bit fast parallel test mode capability**
- **TTL compatible inputs and output**
- **Early Write or output enable controlled write**
- **Single +5V±10% power supply**
- **1024 cycles/128ms refresh**
- **Low power dissipation**
  - **—Standby: 1.1mW**
  - **—Active (70/80/100ns): 578/523/468mW**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, DIP, ZIP**

GENERAL DESCRIPTION

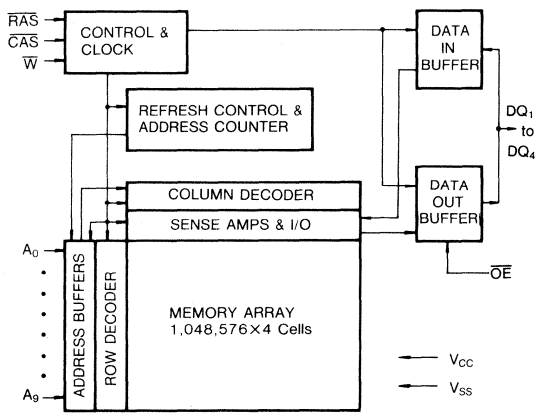
The Samsung KM44C1000AL is a high speed CMOS 1,048,576 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C1000AL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

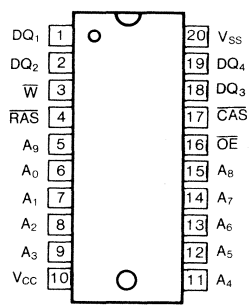
The KM44C1000AL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

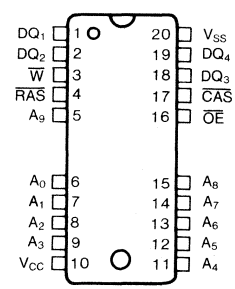


PIN CONFIGURATION (Top Views)

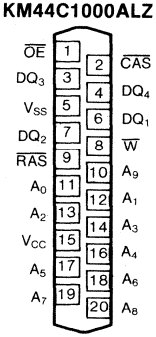
- **KM44C1000ALP**



- **KM44C1000ALJ**



- **KM44C1000ALZ**



Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ_{1-4}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, V_{CC}=5.0V±10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM44C1000AL- 7	I_{CC1}	—	105	mA
	KM44C1000AL- 8		—	95	mA
	KM44C1000AL-10		—	85	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min.)	KM44C1000AL- 7	I_{CC3}	—	105	mA
	KM44C1000AL- 8		—	95	mA
	KM44C1000AL-10		—	85	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling @ t_{PC}=min.)	KM44C1000AL- 7	I_{CC4}	—	80	mA
	KM44C1000AL- 8		—	70	mA
	KM44C1000AL-10		—	60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=W≥V_{CC}−0.2V)		I_{CC5}	—	200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM44C1000AL- 7	I_{CC6}	—	105	mA
	KM44C1000AL- 8		—	95	mA
	KM44C1000AL-10		—	85	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{CC}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V DQ_{1-4}=Don't Care T_{RC}=125μS, T_{RAS}=t_{RAS} min.~1μS		I_{CC7}	—	300	μA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL}, Dout Enable)		I_{CC8}	—	5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*Note: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM44C1000AL-7		KM44C1000AL-8		KM44C1000AL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	185		205		245		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM44C1000AL-7		KM44C1000AL-8		KM44C1000AL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		128		128		128	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to write enable delay	t_{CWD}	50		50		60		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	100		110		135		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	65		70		85		ns	8
$\overline{CAS}$ setup time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
FAst Page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	45		45		55		ns	
Fast page modered-modify-write	t_{PRWC}	105		105		125		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		20		25		ns	
Output buffer tum off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

TEST MODE CYCLE

(Note. 12)

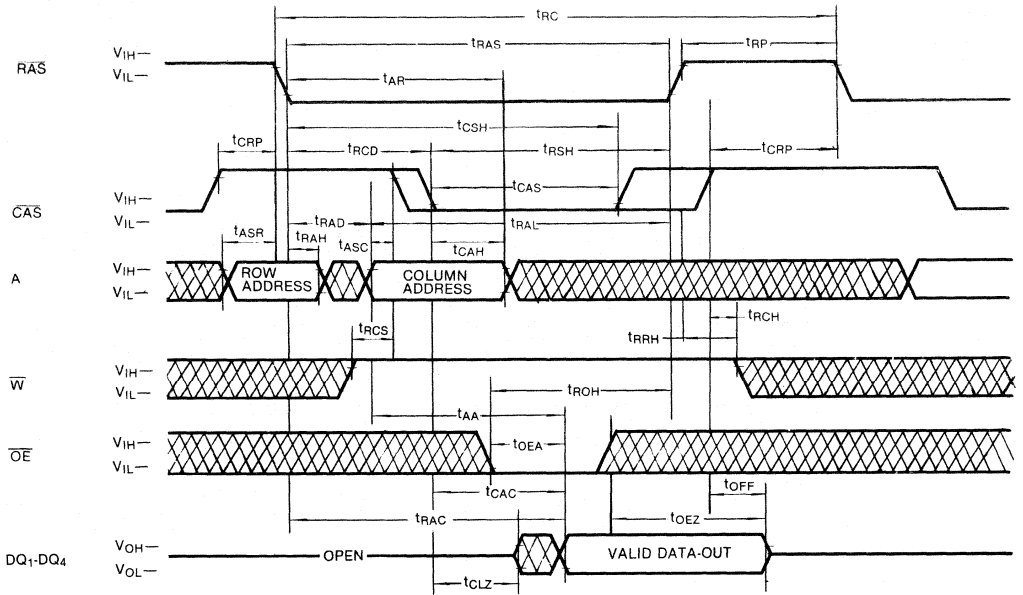
Standard Operation	Symbol	KM44C1000AL-7		KM44C1000AL-8		KM44C1000AL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	135		155		185		ns	
Read-modify-write cycle time	t_{RWC}	190		210		250		ns	
Access time from $\overline{RAS}$	t_{RAC}		75		85		105	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		25		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		45		55	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	75	10,000	85	10,000	105	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{CAS}$ hold time	t_{CSH}	75		85		105		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		45		55		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	55		55		65		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	105		115		140		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	70		75		90		ns	8
Fast mode cycle time	t_{PC}	55		55		65		ns	
Fast page mode read-modefy-write	t_{PRWC}	110		110		130		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	75	200,000	85	200,000	105	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		50		60	ns	3
$\overline{OE}$ access time	t_{OEA}		25		25		30	ns	
$\overline{OE}$ to data delay	t_{OED}	25		25		30		ns	
$\overline{OE}$ command hold time	t_{OEH}	25		25		30		ns	

NOTES

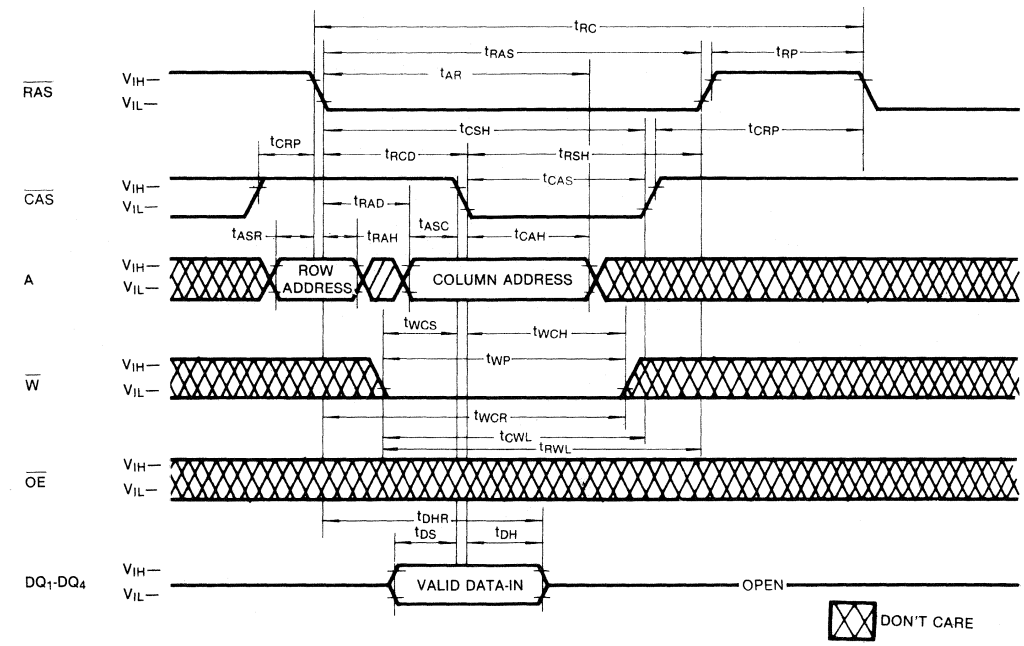
1. An initial pause of 200μs is required after power-up followed by and 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.

TIMING DIAGRAMS

READ CYCLE

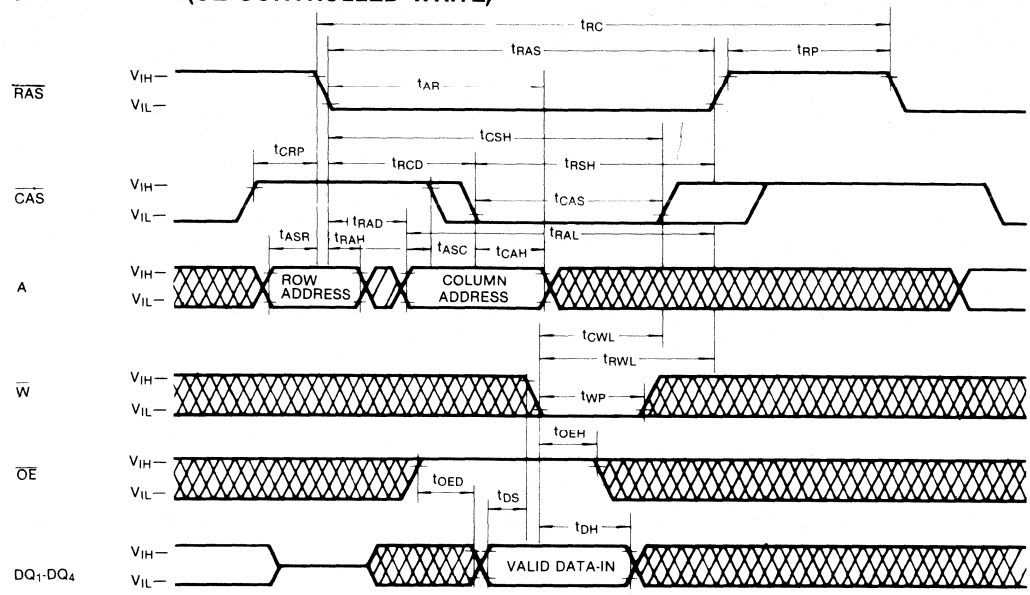


WRITE CYCLE (EARLY WRITE)

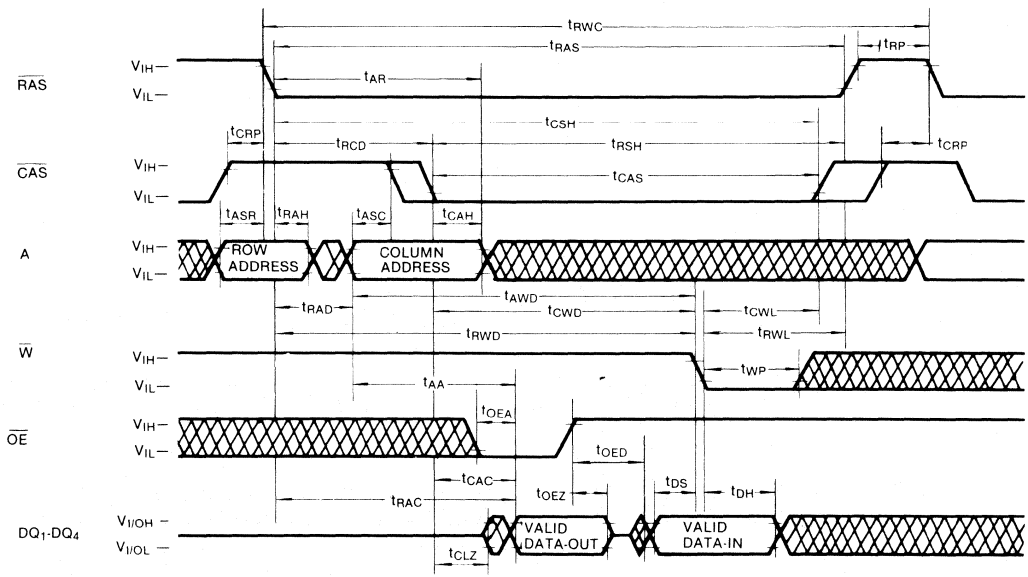


TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



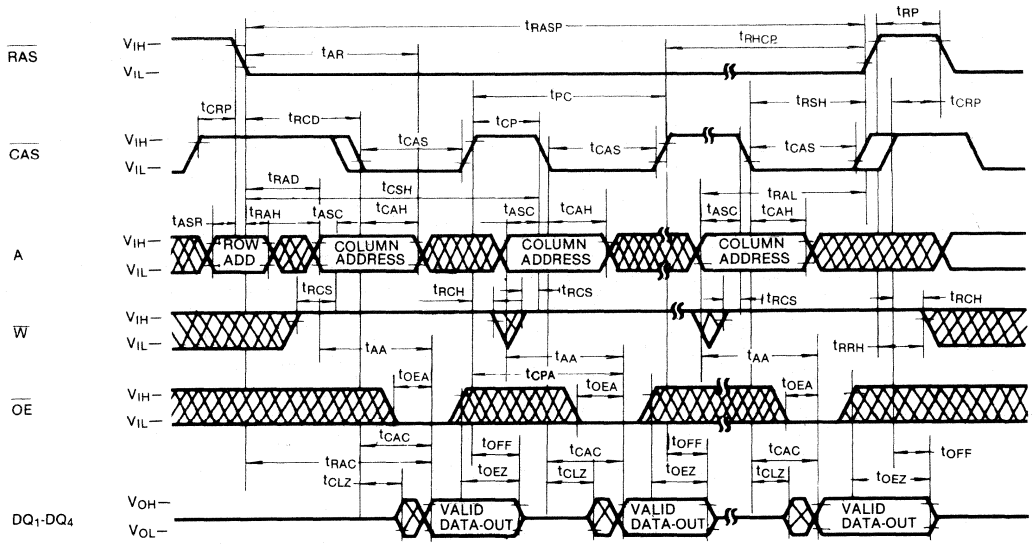
READ-MODIFY-WRITE CYCLE



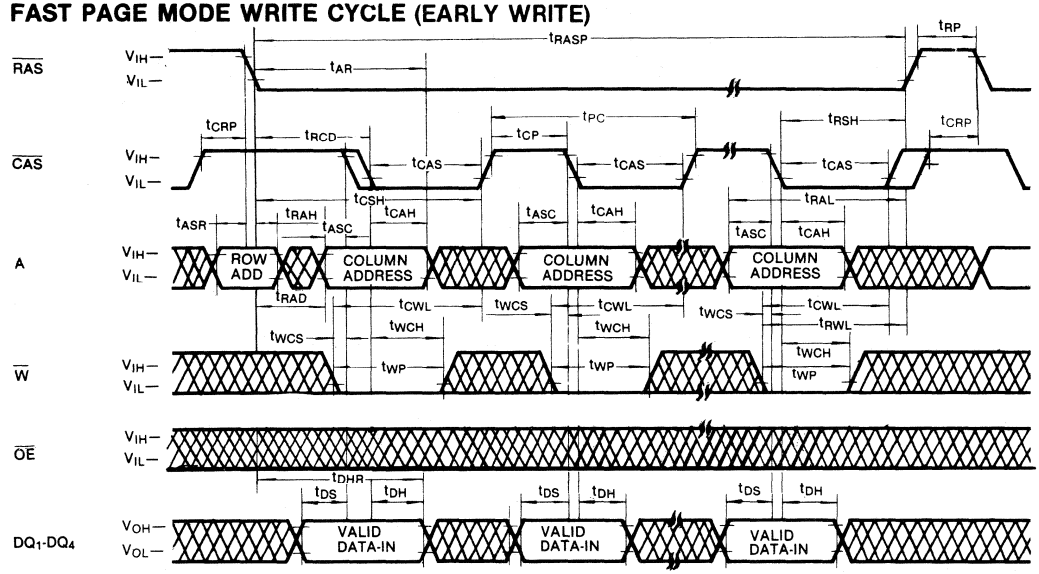
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



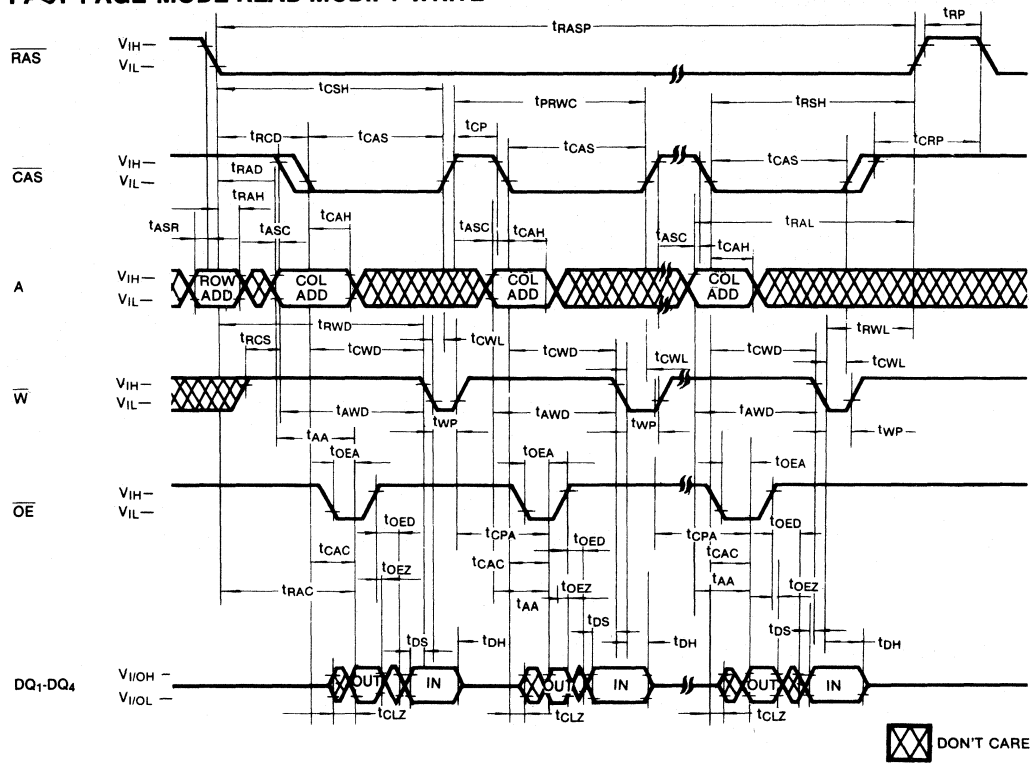
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



DON'T CARE

TIMING DIAGRAMS (Continued)

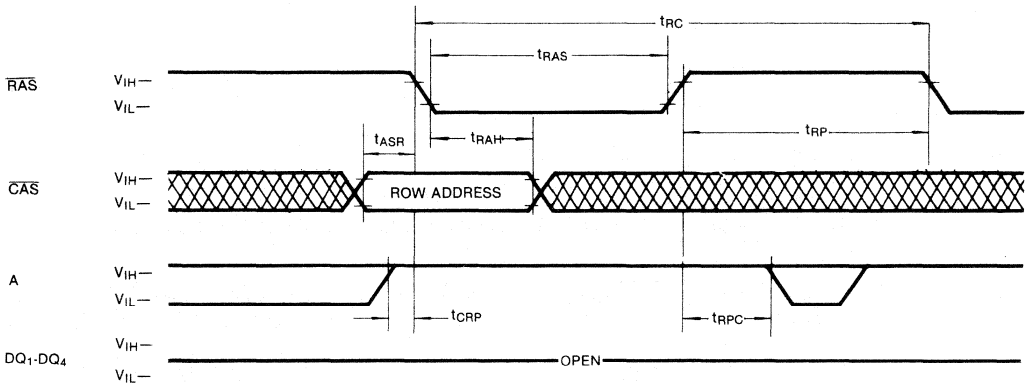
FAST PAGE MODE READ-MODIFY-WRITE



TIMING DIAGRAMS (Continued)

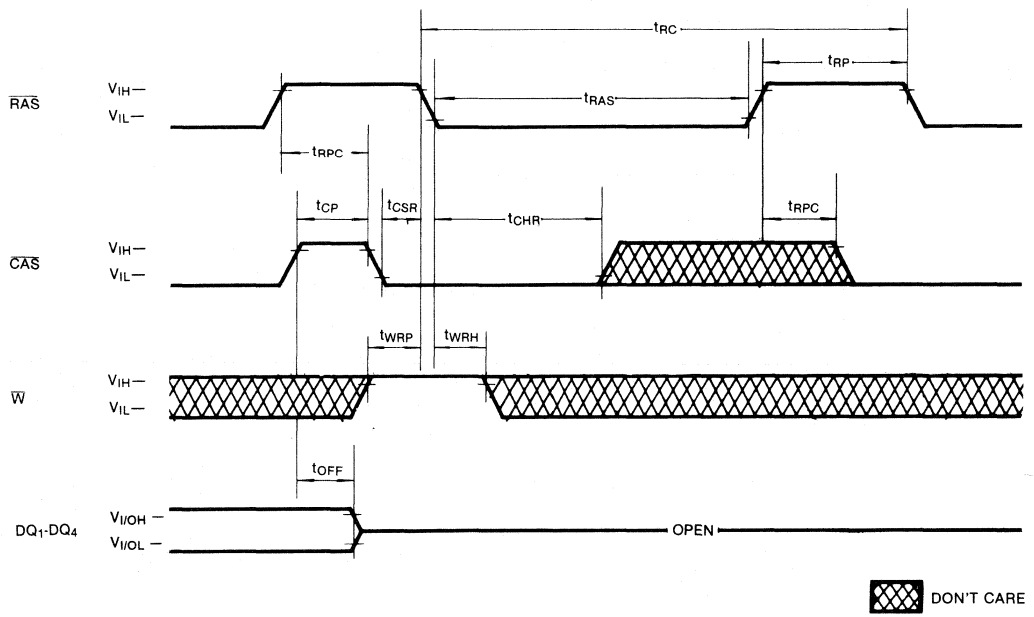
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



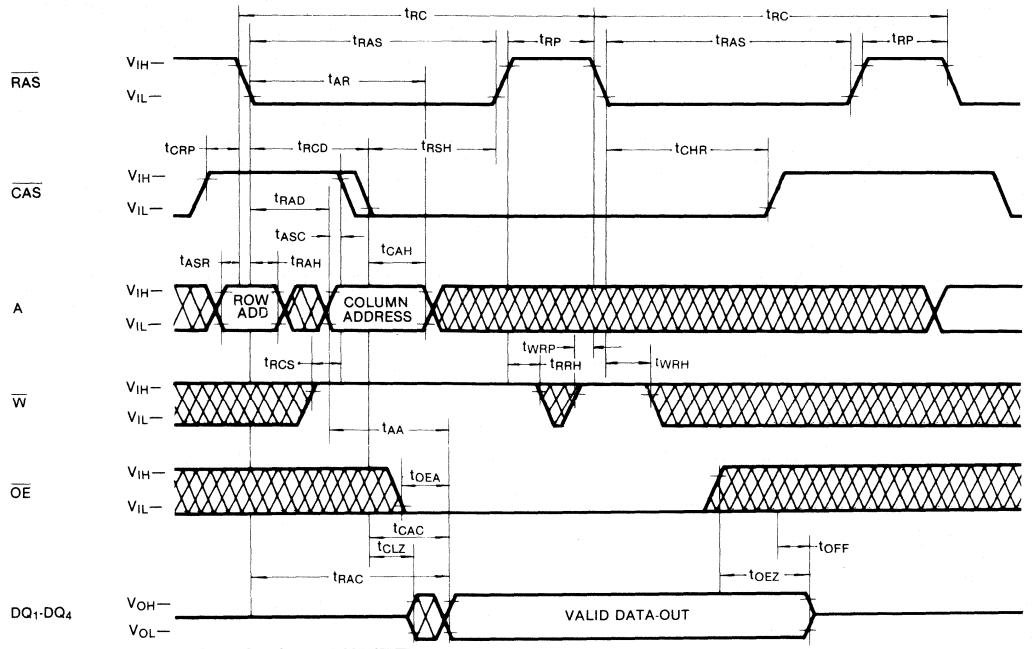
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{OE}$, Address = Don't Care

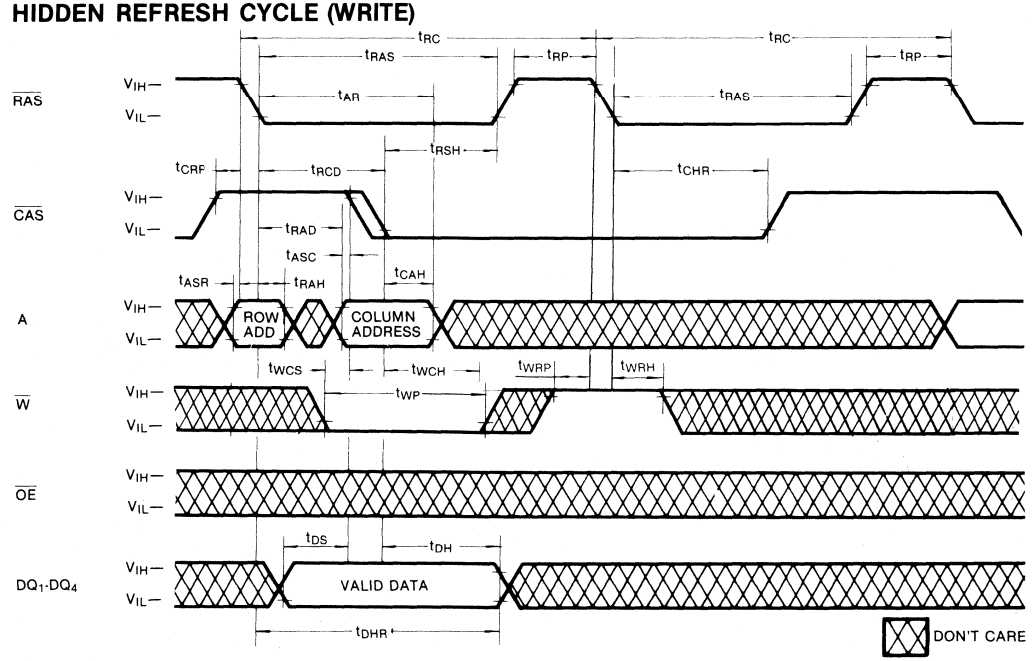


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

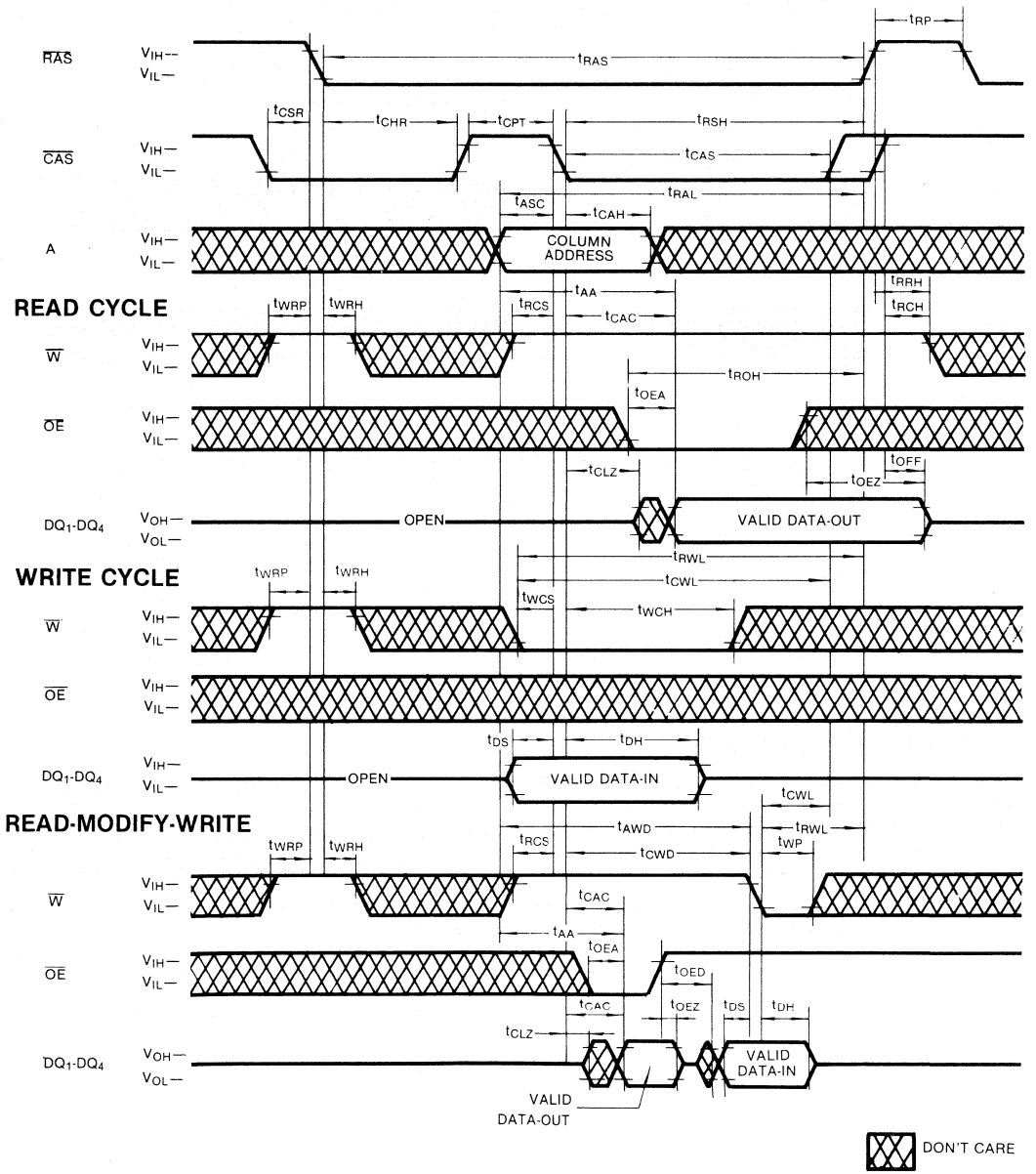


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

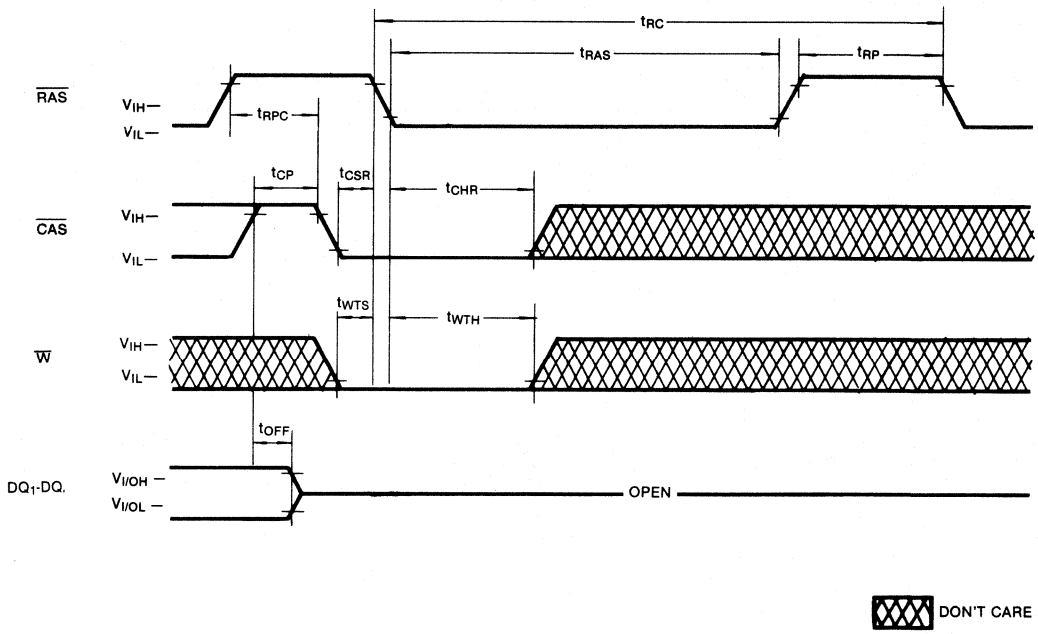
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: $\overline{OE}$, Address=Don't Care



TEST MODE DESCRIPTION

The KM44C1000AL is the RAM organized 1,048,576 words by 4 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM. $\overline{W}$, $\overline{CAS}$-Before-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM44C1000AL contains 4,194,304 memory locations. Twenty address bits are required to address a particular memory location. Since the KM44C1000AL has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM44C1000AL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C1000AL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1000AL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM44C1000AL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44C1000AL has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C1000AL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle. $\overline{OE}$ controlled write.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM44C1000AL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 128 ms. There are several ways to accomplish this.

DEVICE OPERATION (Continued)

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with RAS while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C1000AL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuity is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C1000AL hidden refresh cycle is actually a $\overline{CAS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1000AL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general RAS-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM44C1000AL has Fast Page mode capability. Fast Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In Fast Page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A Fast Page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row address for the same page. Up to 2048 memory cells can be accessed with the same row address.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter.

Column Address—Bits A_0 through A_9 are strobedin by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

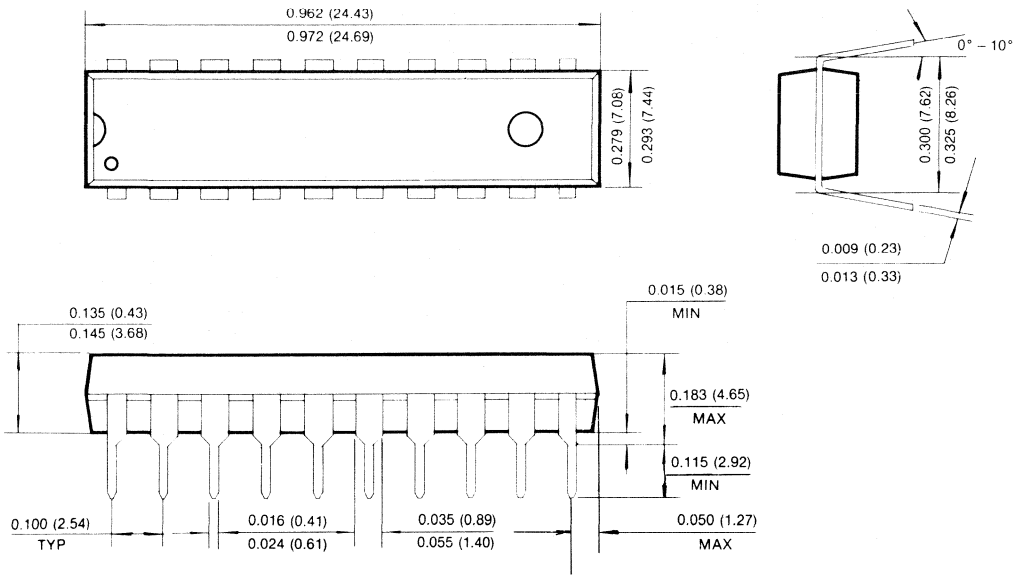
Power-up

If $\overline{RAS}=V_{SS}$ during power-up, the KM44C1000AL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

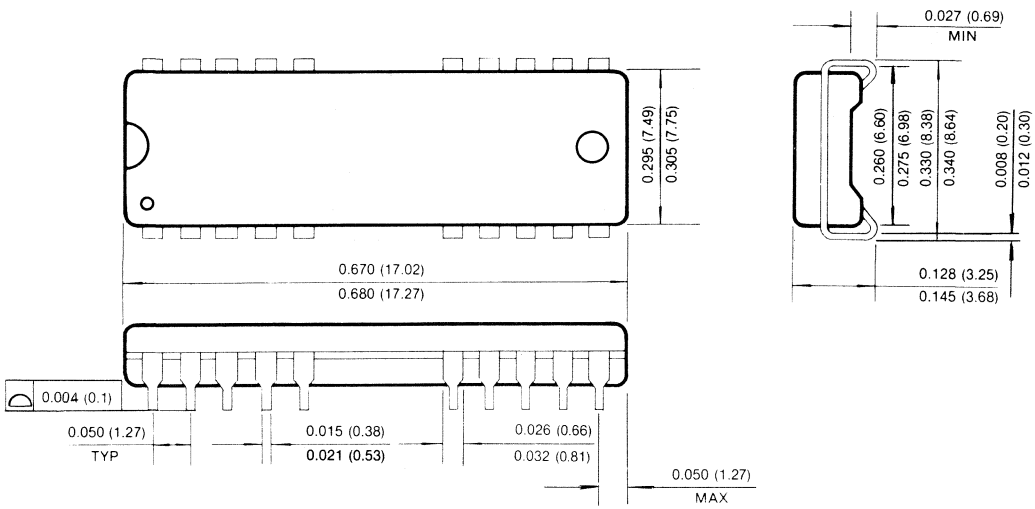
An initial pause of 200μs is required after power-up flowed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$ only refresh cycles before proper device operation is achieved.

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE



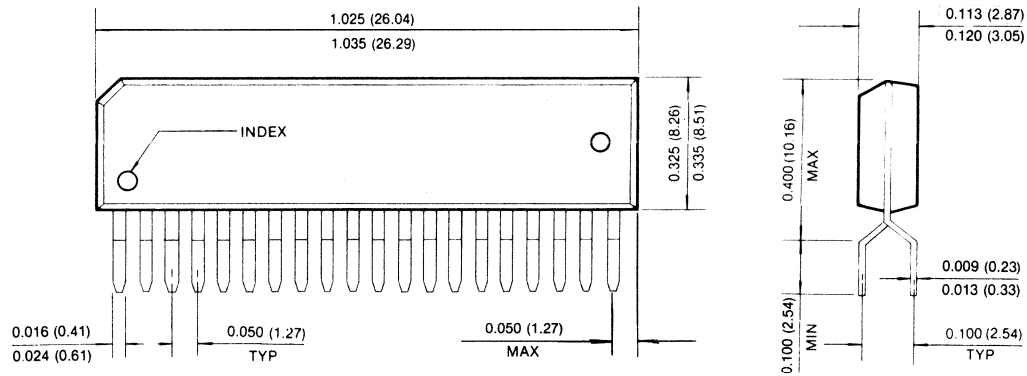
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)



1M×4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C1000ASL- 7	70ns	20ns	130ns
KM44C1000ASL- 8	80ns	20ns	150ns
KM44C1000ASL-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8-bit fast parallel test mode capability**
- **TTL compatible inputs and output**
- **Early Write or output enable controlled write**
- **Single +5V±10% power supply**
- **1024 cycles/256ms refresh**
- **Low power dissipation**
  - **—Standby: 0.6mW**
  - **—Active (70/80/100ns): 578/523/468mW**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, DIP, ZIP**

GENERAL DESCRIPTION

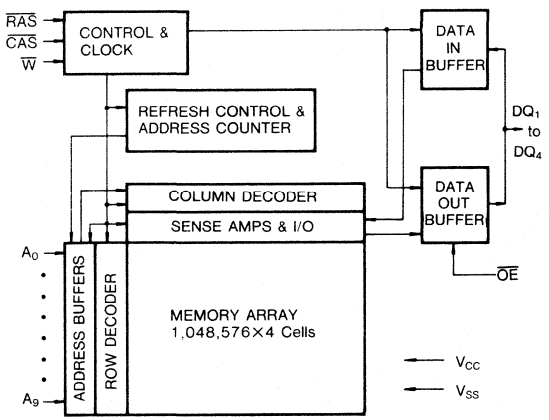
The Samsung KM44C1000ASL is a high speed CMOS 1,048,576 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C1000ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

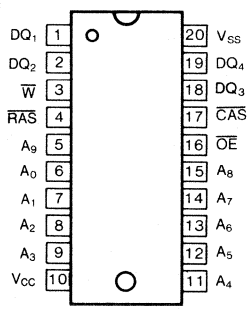
The KM44C1000ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

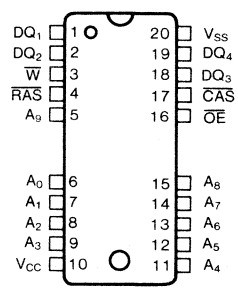


PIN CONFIGURATION (Top Views)

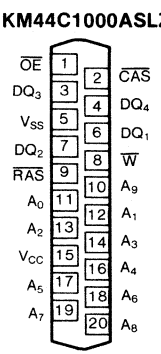
- **KM44C1000ASLP**



- **KM44C1000ASLJ**



- **KM44C1000ASLZ**



Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ_{1-4}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, V_{CC}=5.0V±10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM44C1000ASL- 7	I_{CC1}	—	105	mA
	KM44C1000ASL- 8		—	95	mA
	KM44C1000ASL-10		—	85	mA
Standby Curren ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min.)	KM44C1000ASL- 7	I_{CC3}	—	105	mA
	KM44C1000ASL- 8		—	95	mA
	KM44C1000ASL-10		—	85	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling @ t_{PC}=min.)	KM44C1000ASL- 7	I_{CC4}	—	80	mA
	KM44C1000ASL- 8		—	70	mA
	KM44C1000ASL-10		—	60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$≥V_{CC}−0.2V)		I_{CC5}	—	100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM44C1000ASL- 7	I_{CC6}	—	105	mA
	KM44C1000ASL- 8		—	95	mA
	KM44C1000ASL-10		—	85	mA
Battery Back Up CurrentAverage Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH})=V_{CC}-0.2V Input Low Voltage (V_{IL})=0.2V $\overline{CAS}$=$\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V DQ_{1-4}=Don't Care T_{RC}=250μS, T_{RAS}=t_{RAS} min.~1μS		I_{CC7}	—	150	μA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL}, Dout Enable)		I_{CC8}	—	5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*Note: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM44C1000ASL-7		KM44C1000ASL-8		KM44C1000ASL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	185		205		245		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM44C1000ASL-7		KM44C1000ASL-8		KM44C1000ASL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to write enable delay	t_{CWD}	50		50		60		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	100		110		135		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	65		70		85		ns	8
$\overline{CAS}$ setup time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
FAst Page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	45		45		55		ns	
Fast page mode read-modify-write	t_{PRWC}	105		105		125		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		20		25		ns	
Output buffer tum off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

TEST MODE CYCLE

(Note. 12)

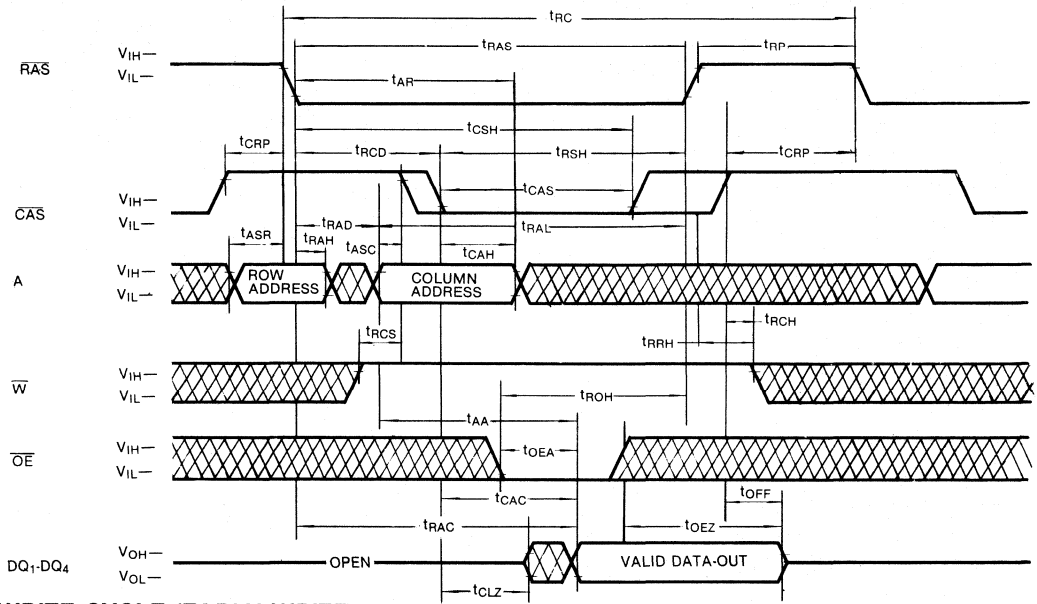
Standard Operation	Symbol	KM44C1000ASL-7		KM44C1000ASL-8		KM44C1000ASL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	135		155		185		ns	
Read-modify-write cycle time	t_{RWC}	190		210		250		ns	
Access time from $\overline{RAS}$	t_{RAC}		75		85		105	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		25		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		45		55	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	75	10,000	85	10,000	105	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{CAS}$ hold time	t_{CSH}	75		85		105		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		45		55		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	55		55		65		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	105		115		140		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	70		75		90		ns	8
Fast mode cycle time	t_{PC}	55		55		65		ns	
Fast page mode read-modefy-write	t_{PRWC}	110		110		130		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	75	200,000	85	200,000	105	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		50		60	ns	3
$\overline{OE}$ access time	t_{OEA}		25		25		30	ns	
$\overline{OE}$ to data delay	t_{OED}	25		25		30		ns	
$\overline{OE}$ command hold time	t_{OEH}	25		25		30		ns	

NOTES

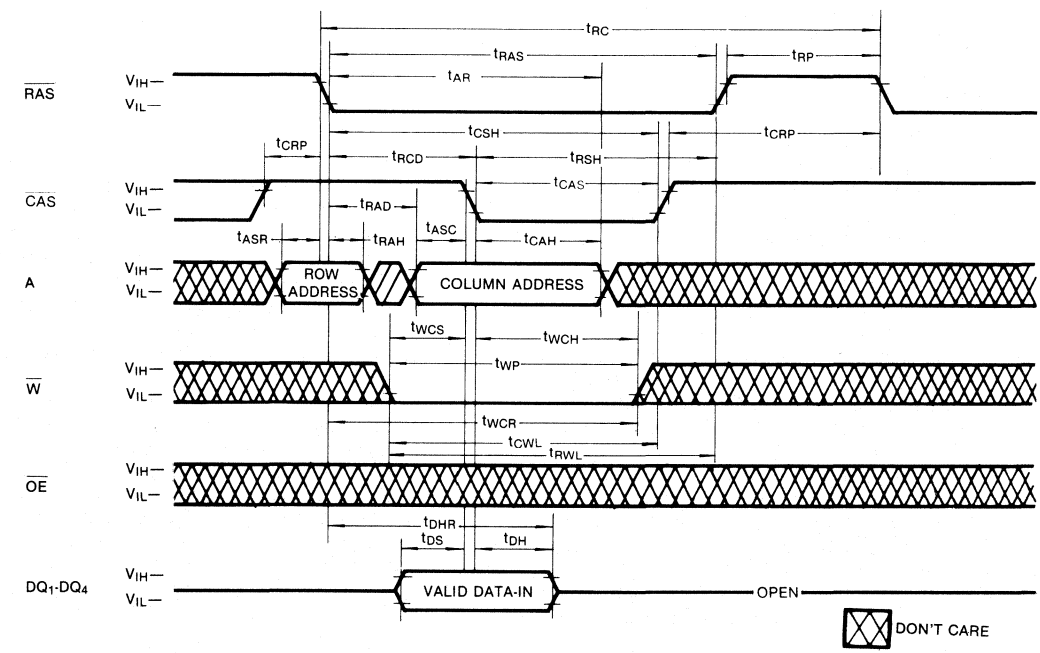
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.

TIMING DIAGRAMS

READ CYCLE

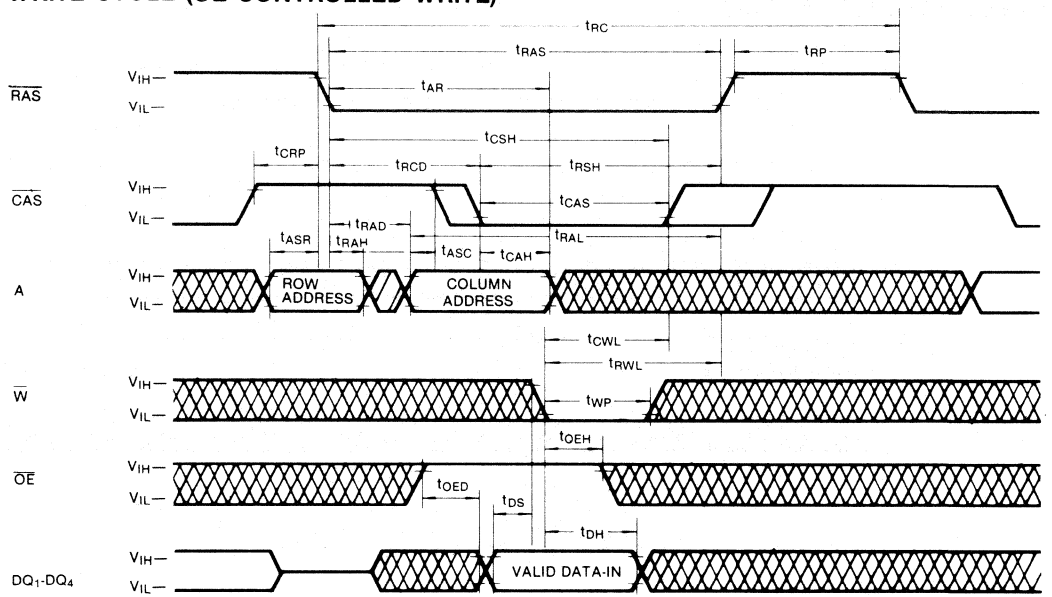


WRITE CYCLE (EARLY WRITE)

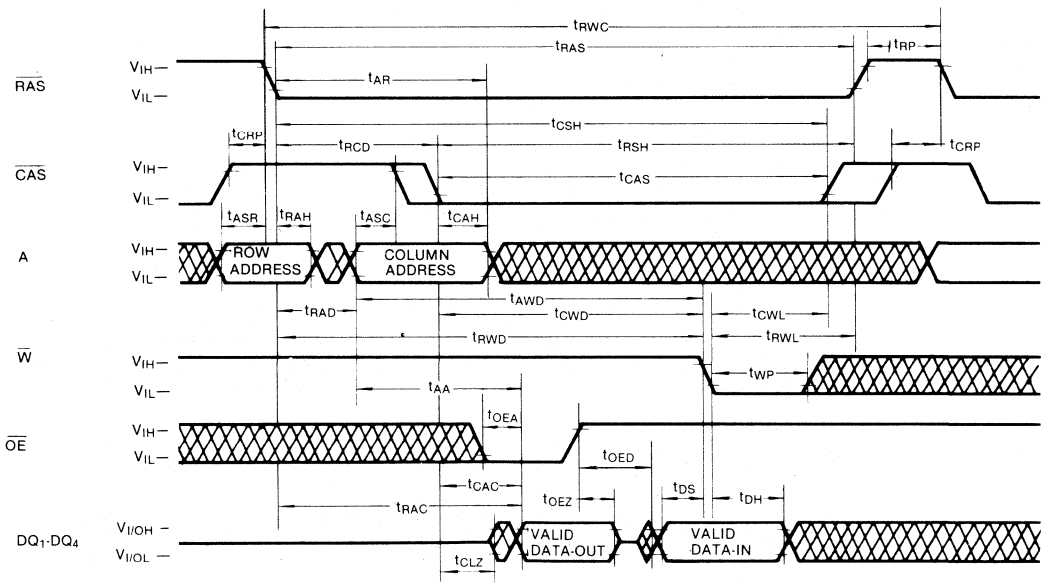


TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



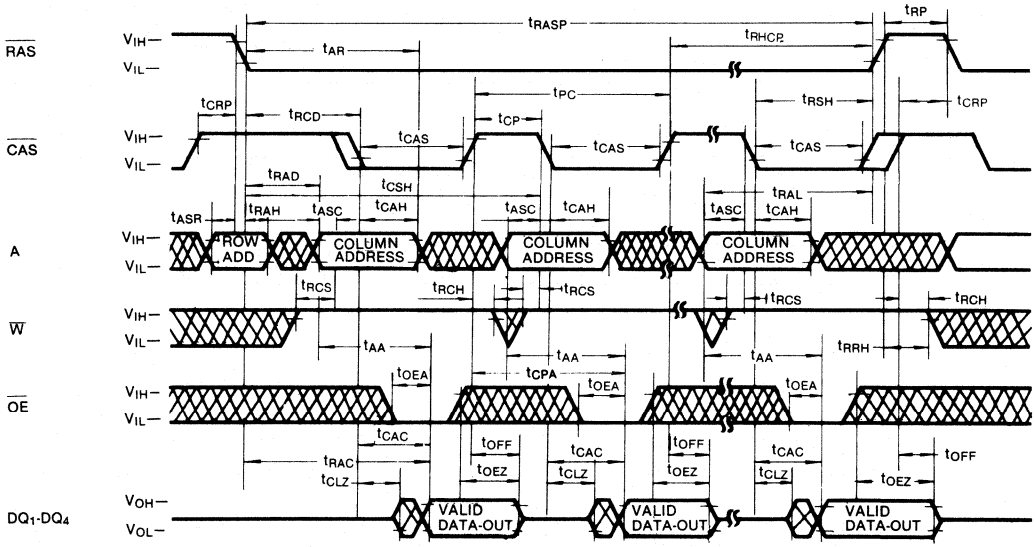
READ-MODIFY-WRITE CYCLE



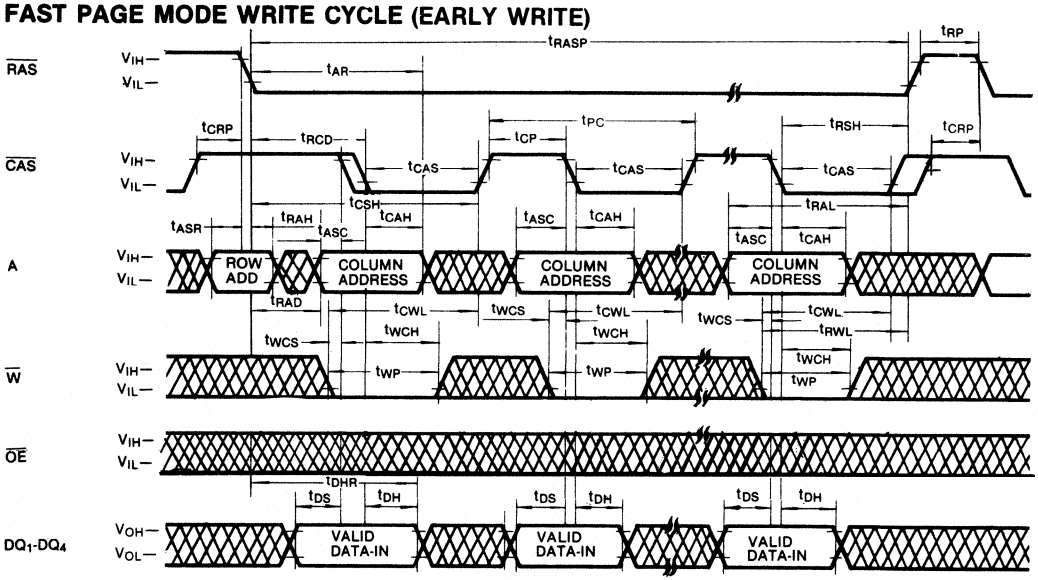
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



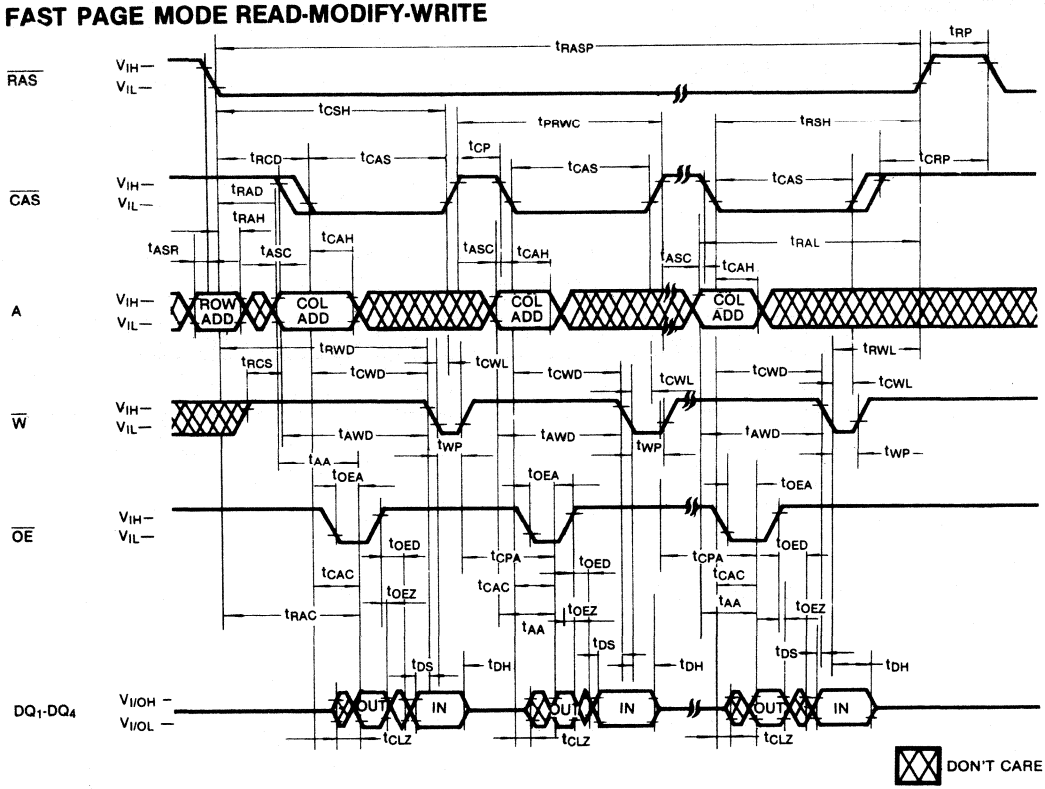
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



DON'T CARE

TIMING DIAGRAMS (Continued)

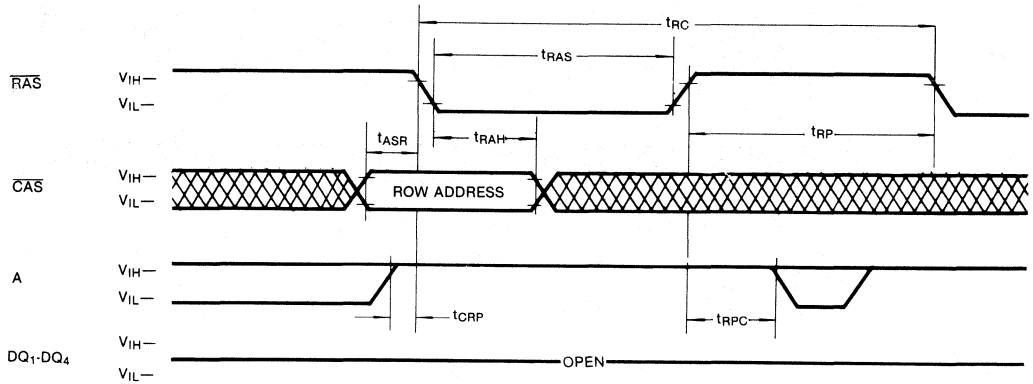
FAST PAGE MODE READ-MODIFY-WRITE



TIMING DIAGRAMS (Continued)

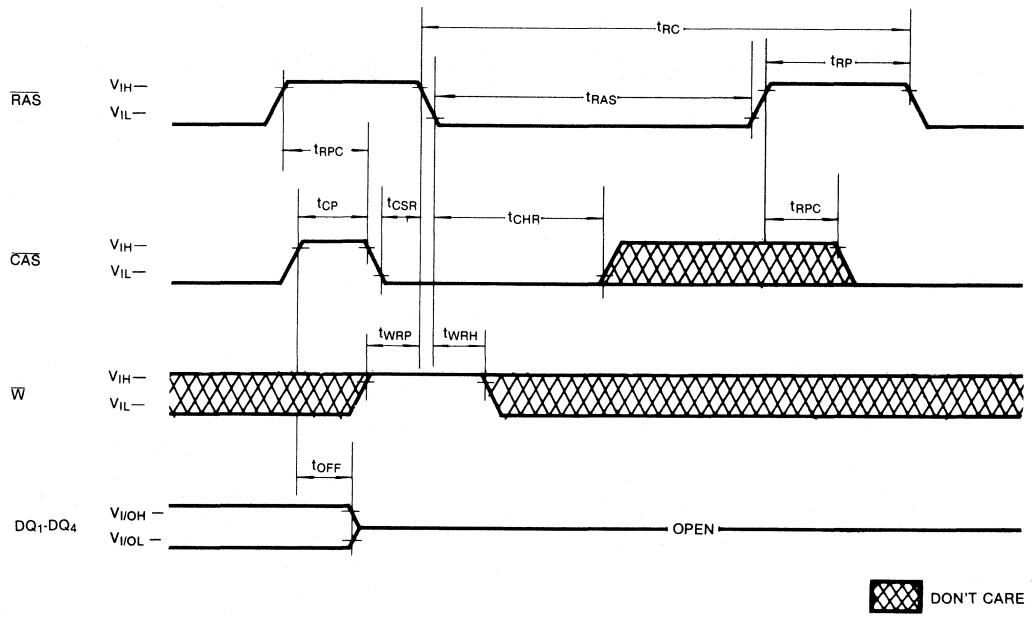
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



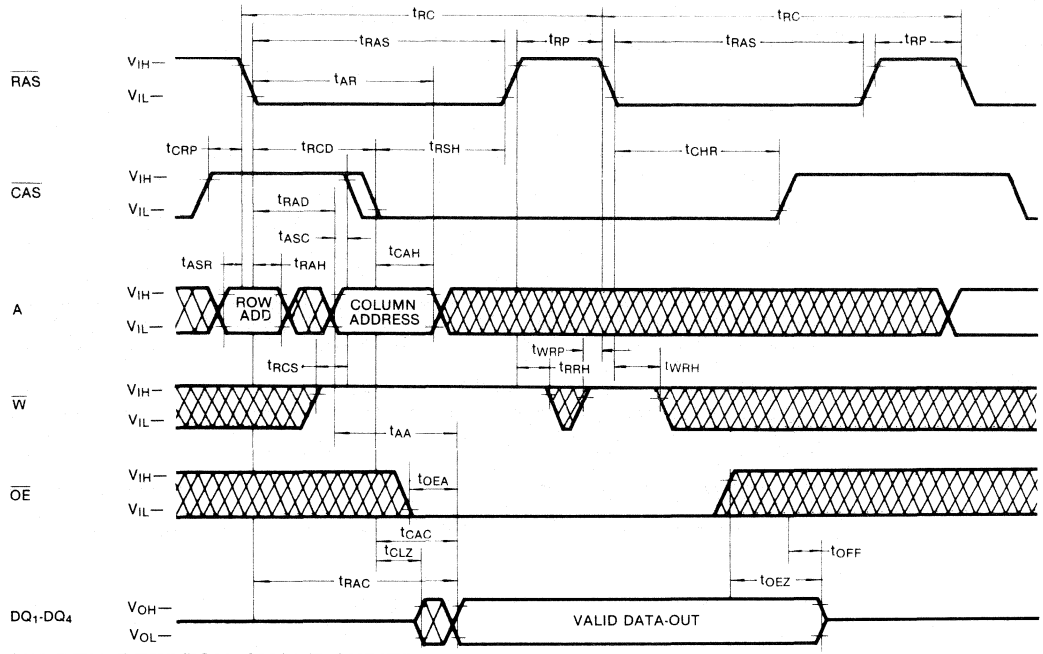
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{OE}$, Address = Don't Care

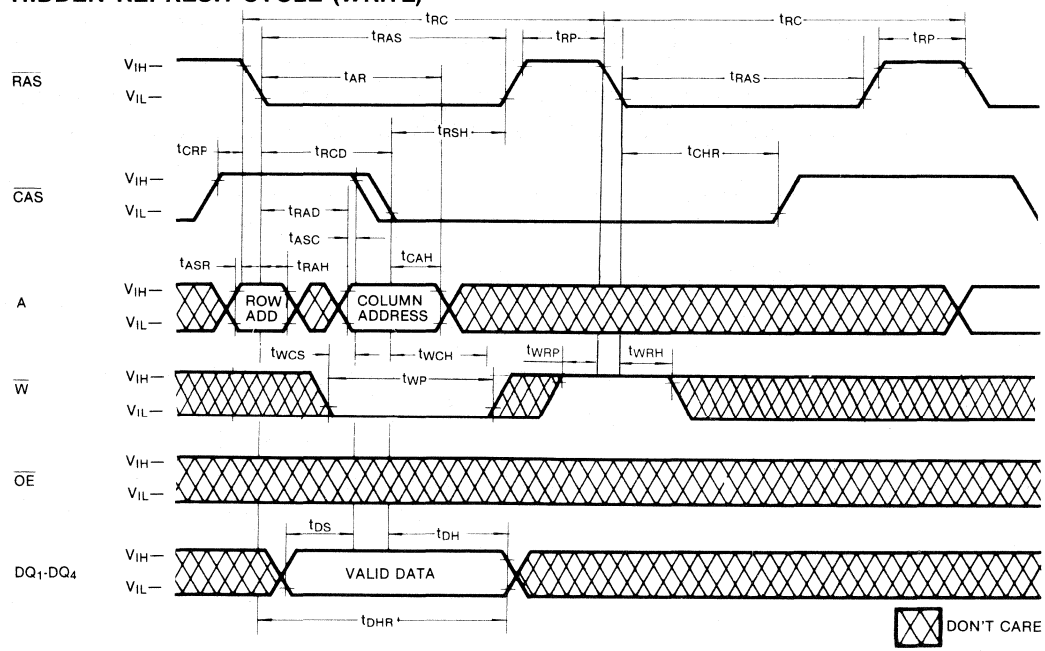


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

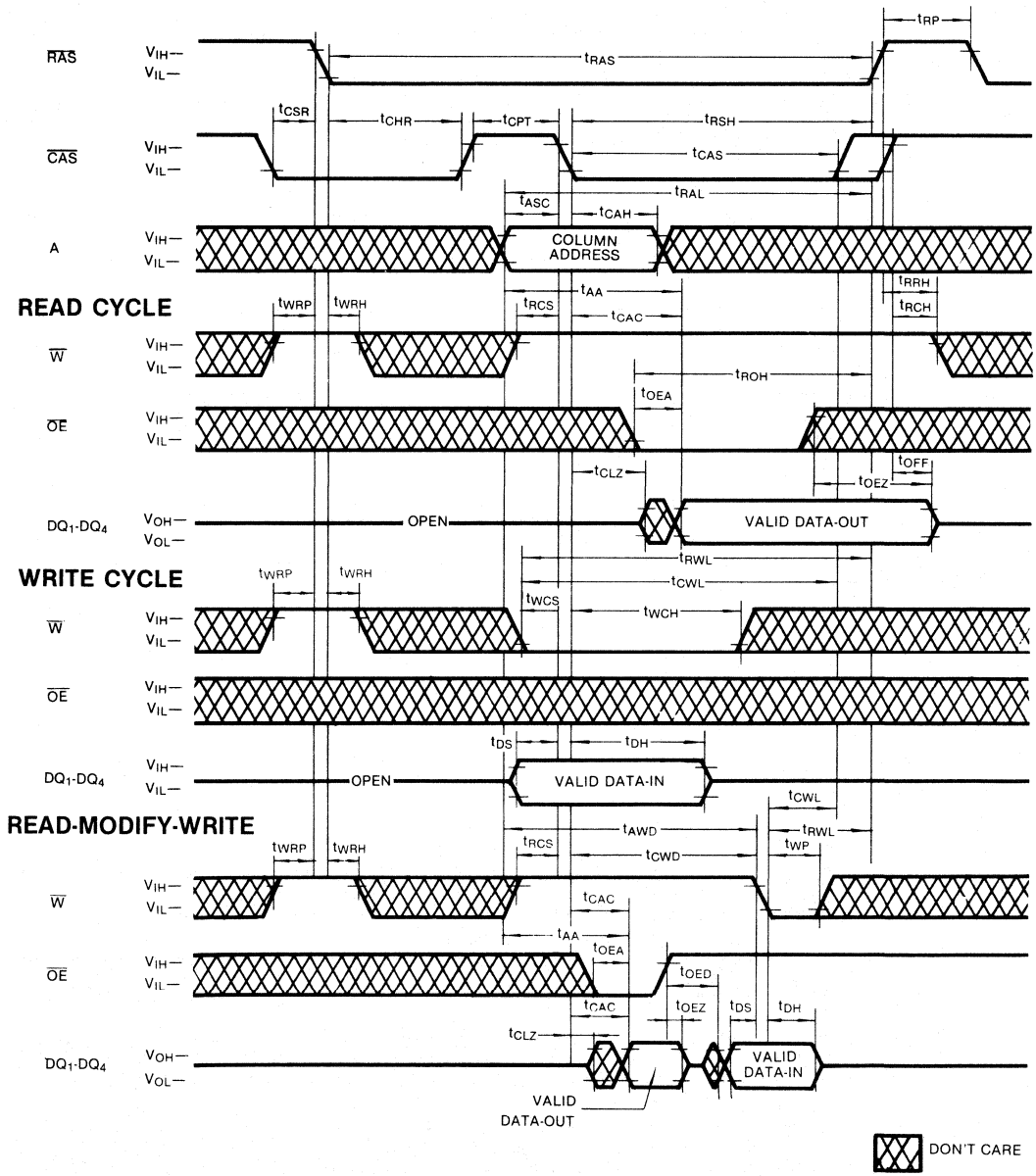


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

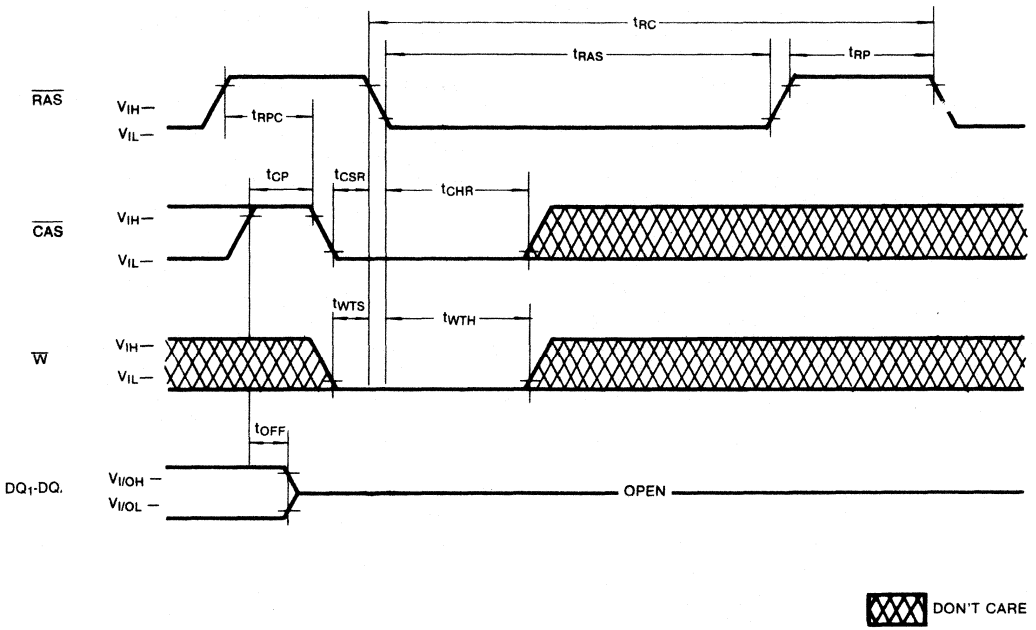
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: $\overline{OE}$, Address=Don't Care



TEST MODE DESCRIPTION

The KM44C1000ASL is the RAM organized 1,048,576 words by 4 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM. $\overline{W}$, $\overline{CAS}$-Before-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM44C1000ASL contains 4,194,304 memory locations. Twenty address bits are required to address a particular memory location. Since the KM44C1000ASL has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM44C1000ASL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C1000ASL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1000ASL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM44C1000ASL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44C1000ASL has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C1000ASL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle. $\overline{OE}$ controlled write.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM44C1000ASL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 256 ms. There are several ways to accomplish this.

DEVICE OPERATION (Continued)

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with RAS while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C1000ASL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuity is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C1000ASL hidden refresh cycle is actually a $\overline{CAS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1000ASL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general RAS-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM44C1000ASL has Fast Page mode capability. Fast Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In Fast Page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A Fast Page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row address for the same page. Up to 2048 memory cells can be accessed with the same row address.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter.

Column Address—Bits A_0 through A_9 are strobedin by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

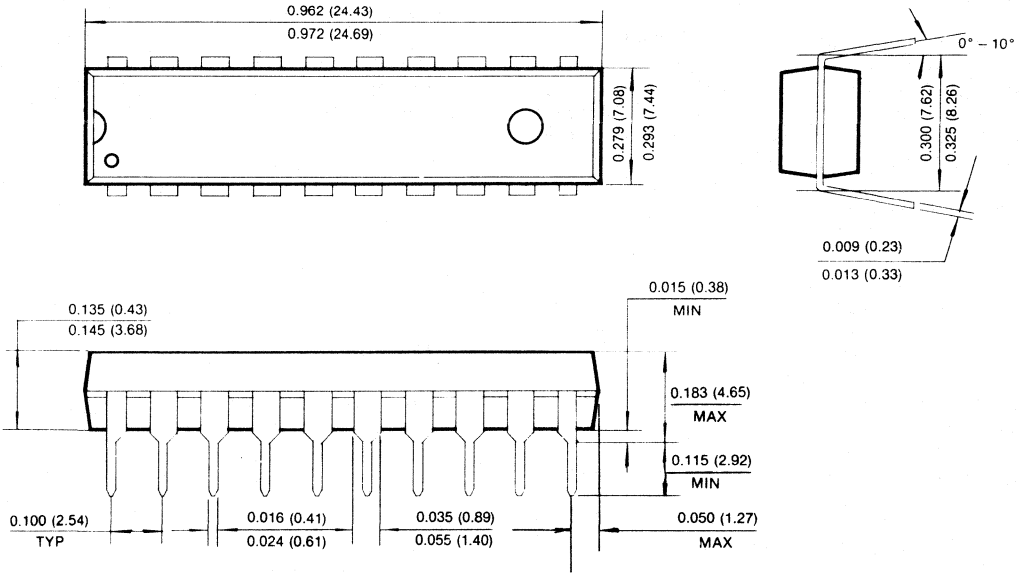
Power-up

If $\overline{RAS}$=V_{SS} during power-up, the KM44C1000ASL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

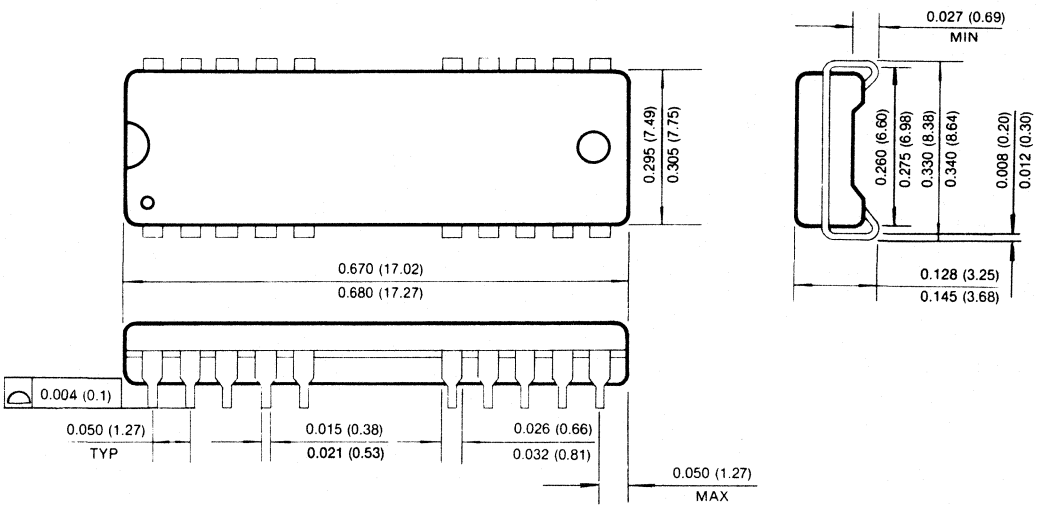
An initial pause of 200μs is required after power-up followed by 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE



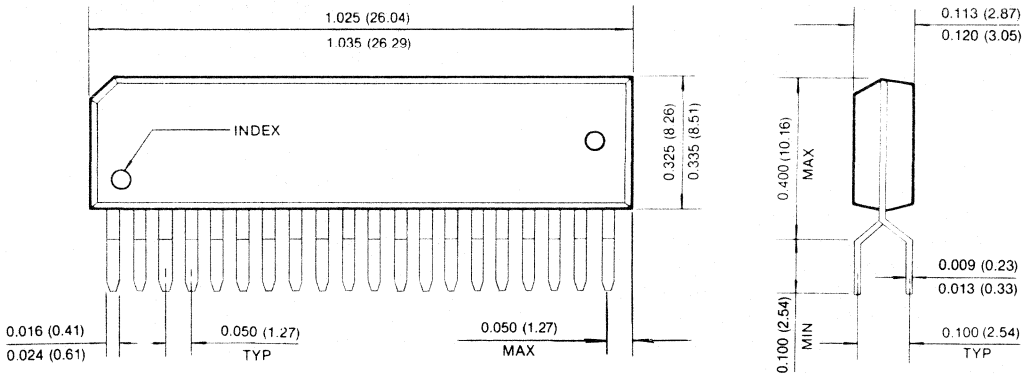
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)



1M×4 Bit CMOS Dynamic RAM with Fast Page Mode (Write Per Bit Mode)

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C1010A-7	70ns	20ns	130ns
KM44C1010A-8	80ns	20ns	150ns
KM44C1010A-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **Write Per Bit Mode capability**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **8-bit fase parallel test mode capability**
- **TTL compatible inputs and output**
- **Early Write or output enable controlled write**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, DIP and ZIP**

GENERAL DESCRIPTION

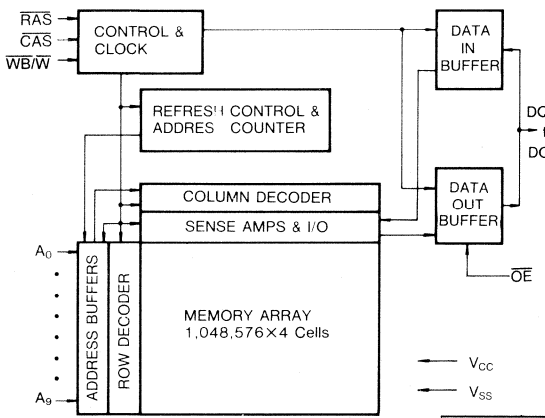
The Samsung KM44C1010A is a CMOS high speed 1,048,576 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C1010A features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

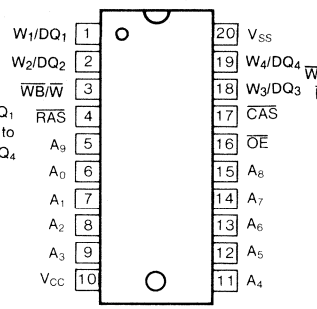
The KM44C1010A is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

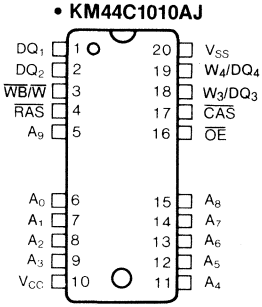


PIN CONFIGURATION (Top Views)

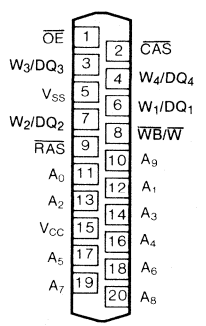
• KM44C1010AP



• KM44C1010AJ



• KM44C1010AZ



Pin Name	Pin Function
A_0-A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB}/\overline{W}$	Write Per Bit/Read/Write Input
$\overline{OE}$	Data Output Enable
W_1/DQ_1 ~ W_4/DQ_4	Write Select/Data In, Out
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC} = min.)	KM44C1010A-7	I_{CC1}	—	105	mA
	KM44C1010A-8		—	95	mA
	KM44C1010A-10		—	85	mA
Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS} = V_{IH}$, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM44C1010A-7	I_{CC3}	—	105	mA
	KM44C1010A-8		—	95	mA
	KM44C1010A-10		—	85	mA
Fast Page Mode Current* ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling @t_{PC} = min.)	KM44C1010A-7	I_{CC4}	—	80	mA
	KM44C1010A-8		—	70	mA
	KM44C1010A-10		—	60	mA
Standby Current ($\overline{RAS} = \overline{CAS} = W \geq V_{CC} - 0.2V$)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min.)	KM44C1010A-7	I_{CC6}	—	105	mA
	KM44C1010A-8		—	95	mA
	KM44C1010A-10		—	85	mA
Standby Current ($\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IL}$, D_{OUT} = Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test = 0V)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed less than two times while $RAS = V_{IL}$. In I_{CC4}, Address can be changed maximum once while $CAS = V_{IH}$.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM44C1010A-7		KM44C1010A-8		KM44C1010A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	185		205		245		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

Parameter	Symbol	KM44C1010A-7		KM44C1010A-8		KM44C1010A-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to write enable delay	t_{CWD}	50		50		60		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	100		110		135		ns	8
Column address to W delay time	t_{AWD}	60		70		85		ns	8
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		45		45		55	ns	3
Fast page mode cycle time	t_{PC}	50		50		60		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	45		45		55		ns	
Fast page modered-modify-write	t_{PRWC}	105		105		125		ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	70	200,000	80	200,000	100	200,000	ns	
Write command set-up time (test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	
Write per bit set-up time	t_{WBS}	0		0		0		ns	
Write per bit hold time	t_{WBH}	10		15		15		ns	
Write per bit selection set-up time	t_{WDS}	0		0		0		ns	
Write per bit selection hold time	t_{WDH}	10		15		15		ns	

TEST MODE CYCLE

(Note. 12)

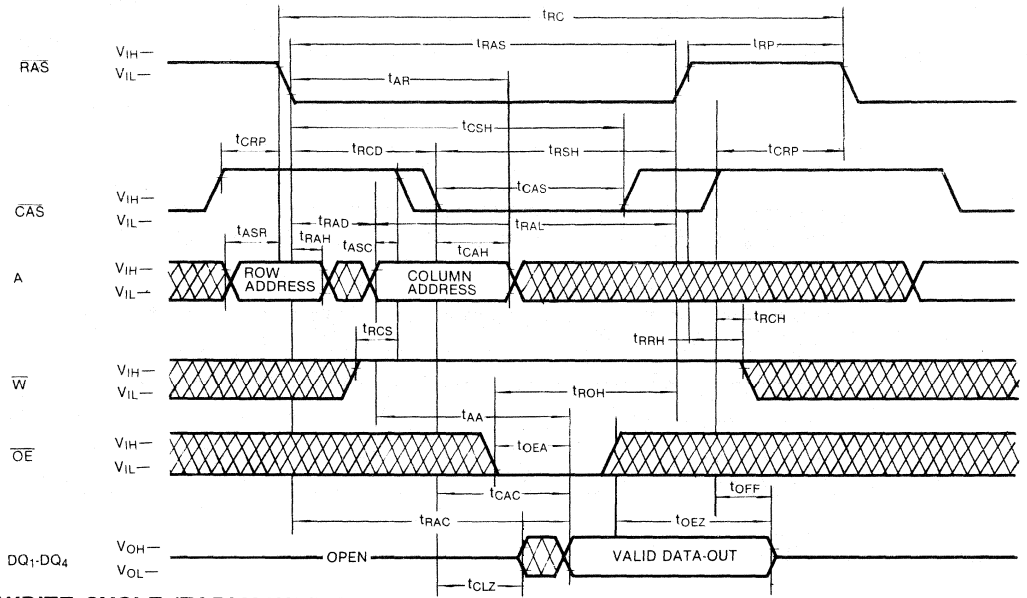
Standard Operation	Symbol	KM44C1000A-7		KM44C1000A-8		KM44C1000A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	135		155		185		ns	
Read-modify-write cycle time	t_{RWC}	190		210		250		ns	
Access time from $\overline{RAS}$	t_{RAC}		75		85		105	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		25		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		45		55	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	75	10,000	85	10,000	105	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{CAS}$ hold time	t_{CSH}	75		85		105		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40		45		55		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	55		55		65		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	105		115		140		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	70		75		90		ns	8
Fast mode cycle time	t_{PC}	55		55		65		ns	
Fast page mode read-modefy-write	t_{PRWC}	110		110		130		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	75	200,000	85	200,000	105	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		50		50		60	ns	3
$\overline{OE}$ access time	t_{OEA}		25		25		30	ns	
$\overline{OE}$ to data delay	t_{OED}	25		25		30		ns	
$\overline{OE}$ command hold time	t_{OEH}	25		25		30		ns	

NOTES

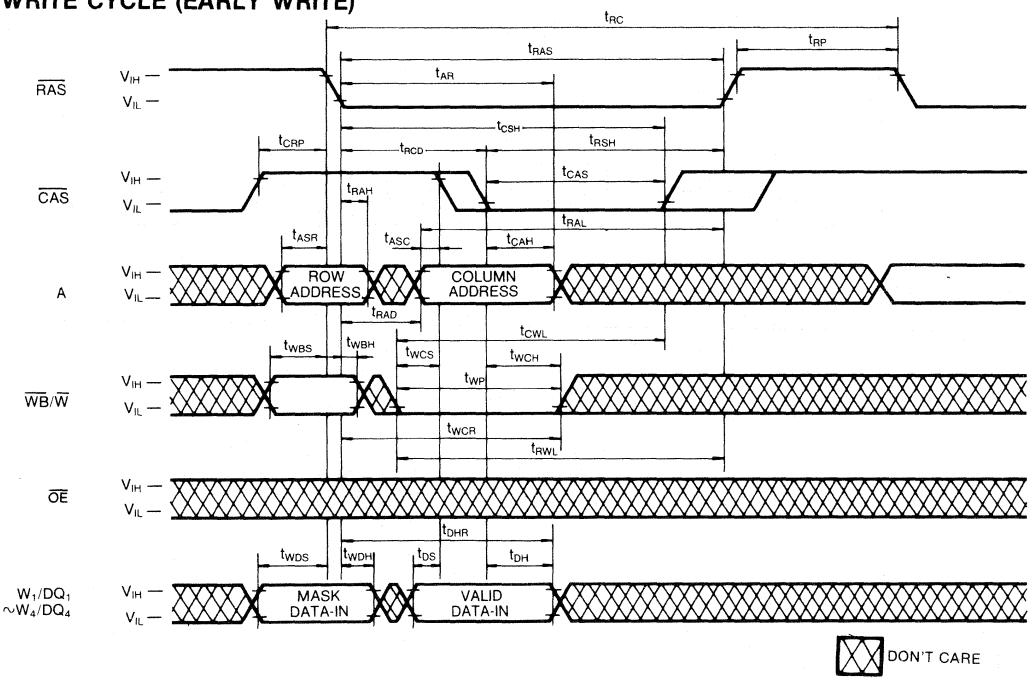
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.

TIMING DIAGRAMS

READ CYCLE

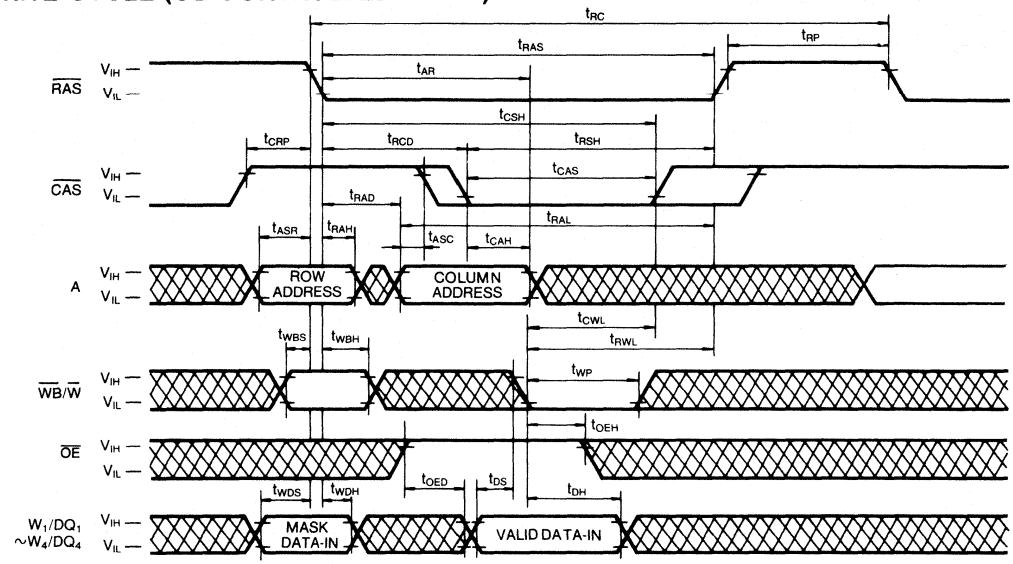


WRITE CYCLE (EARLY WRITE)

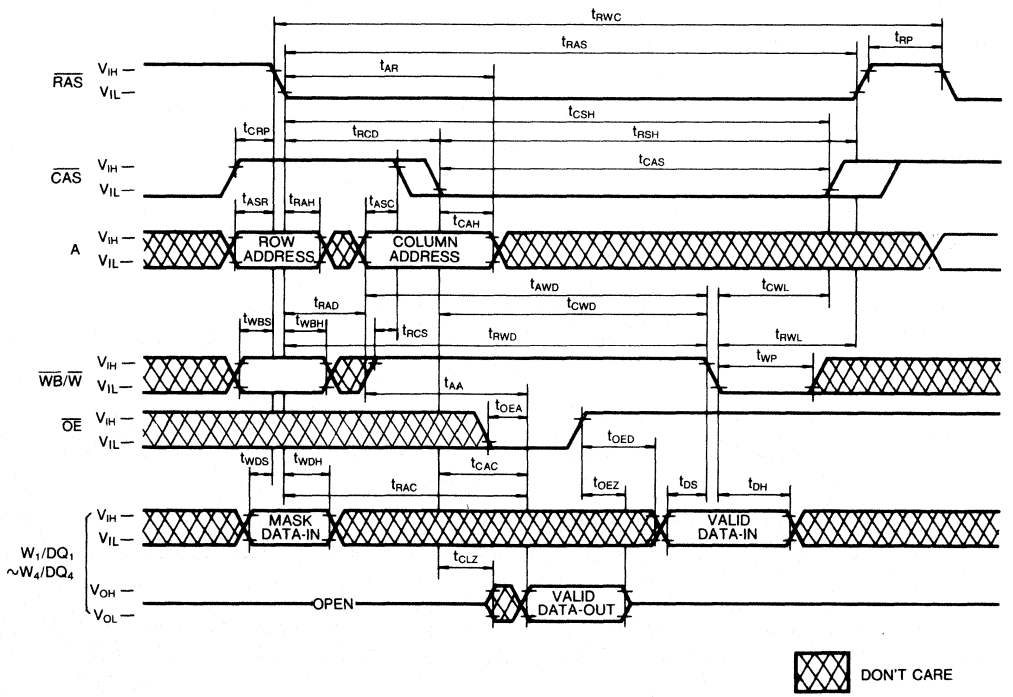


TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

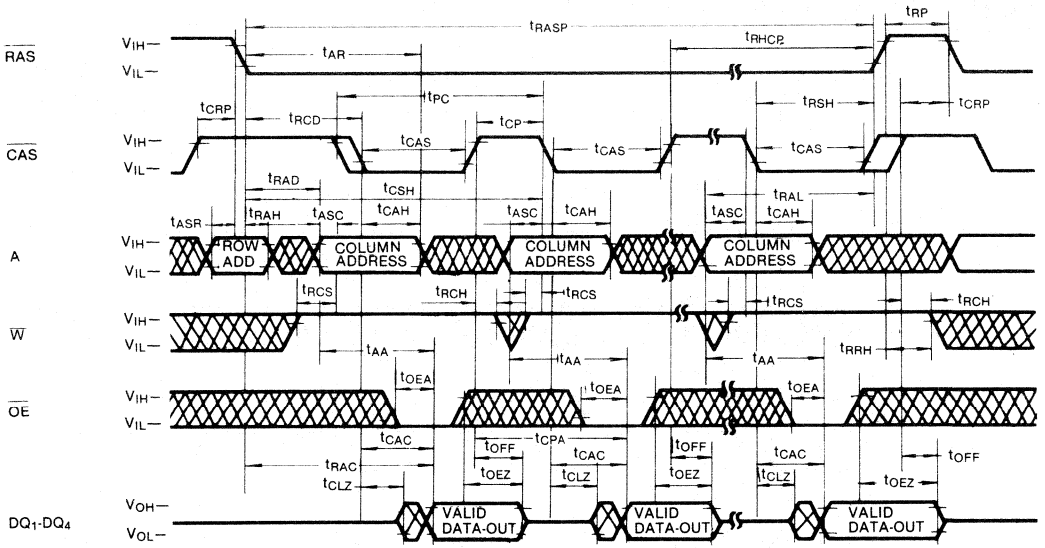


READ-MODIFY-WRITE CYCLE

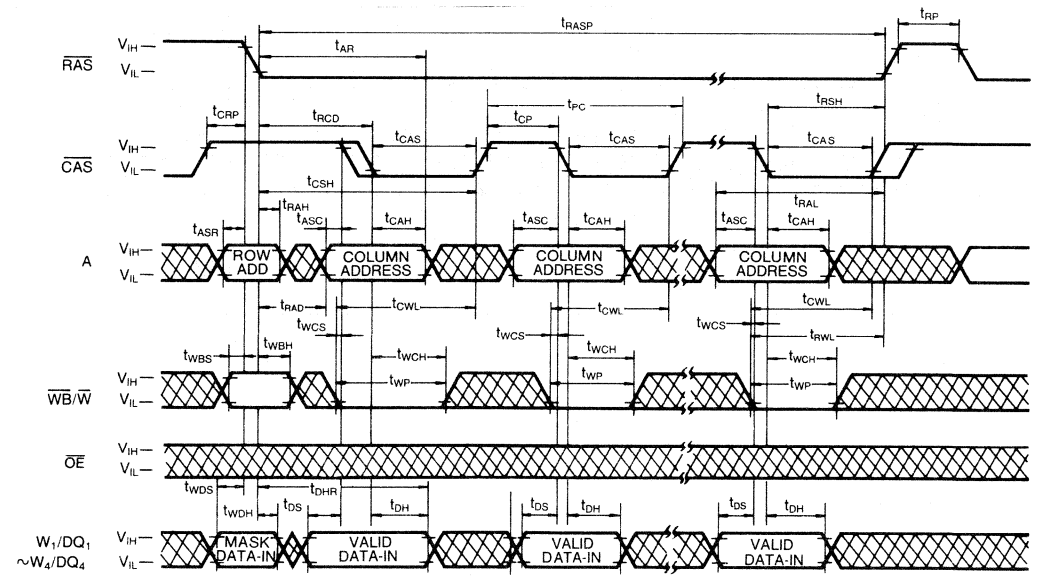


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE

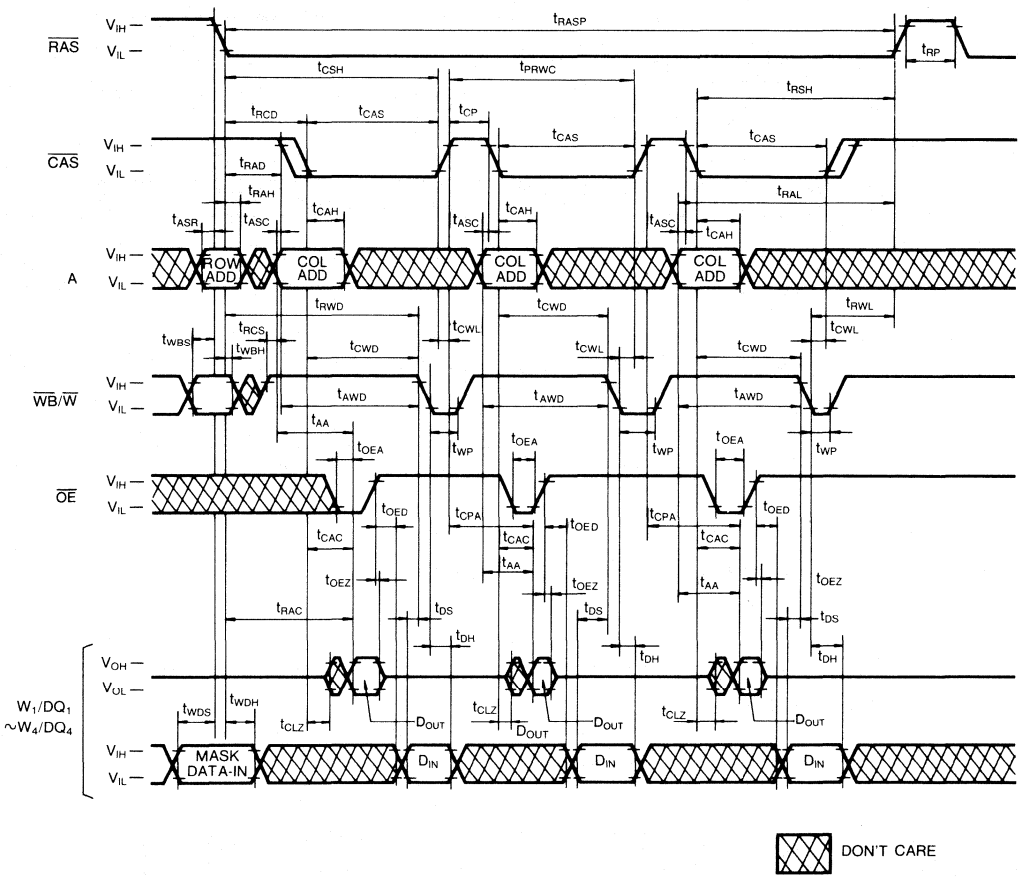


FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)

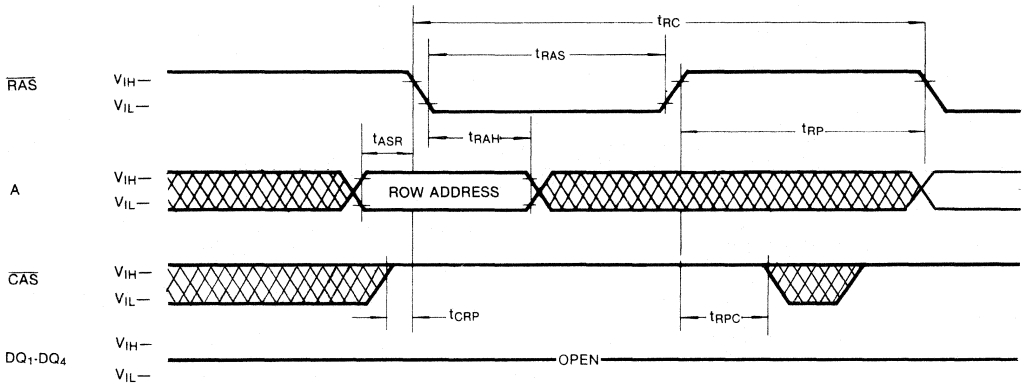
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

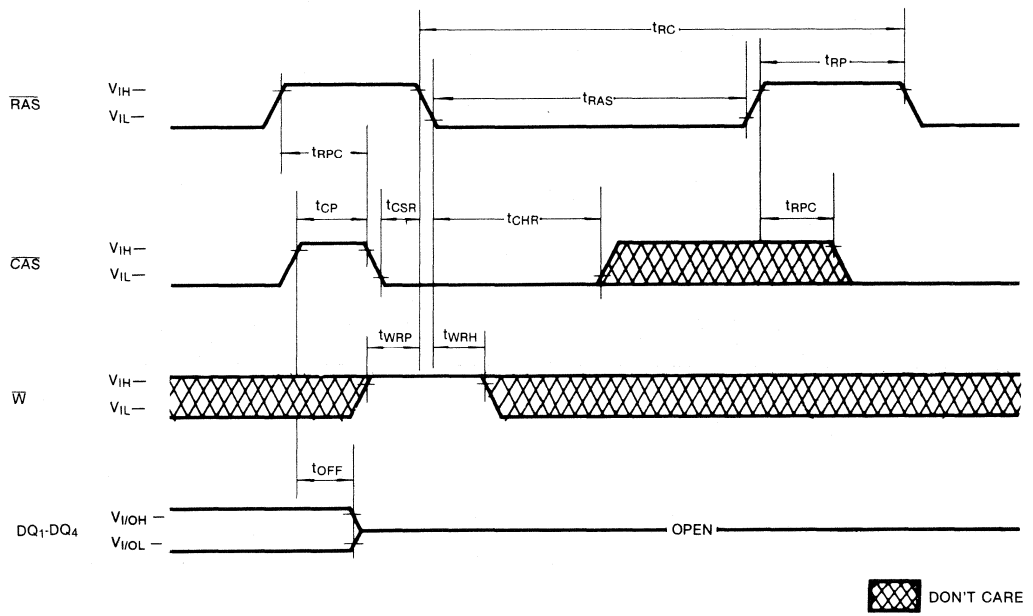
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



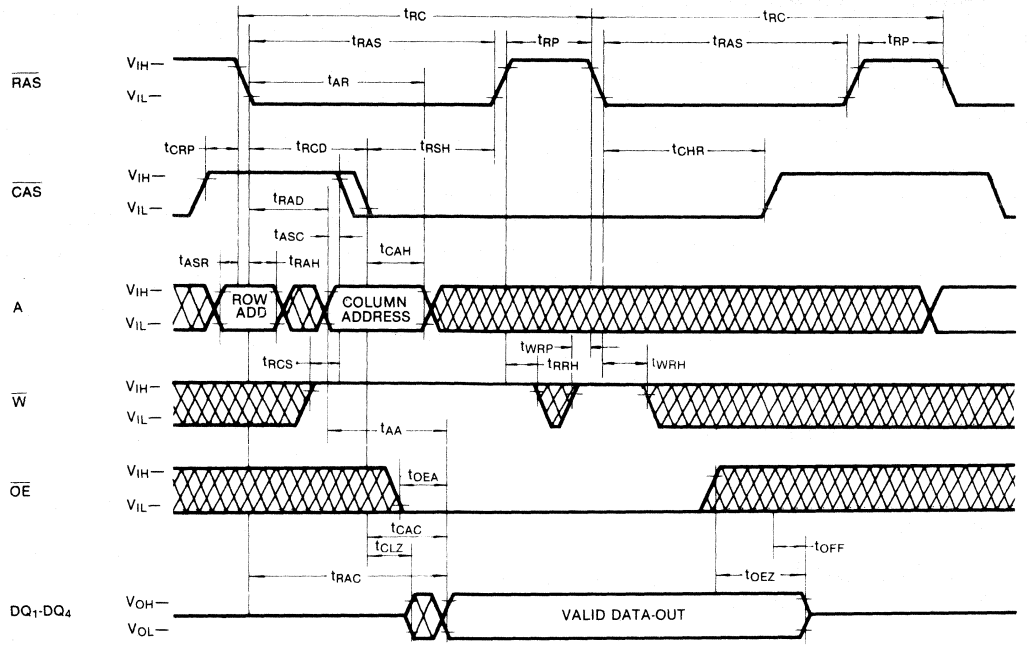
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{OE}$, Address = Don't Care

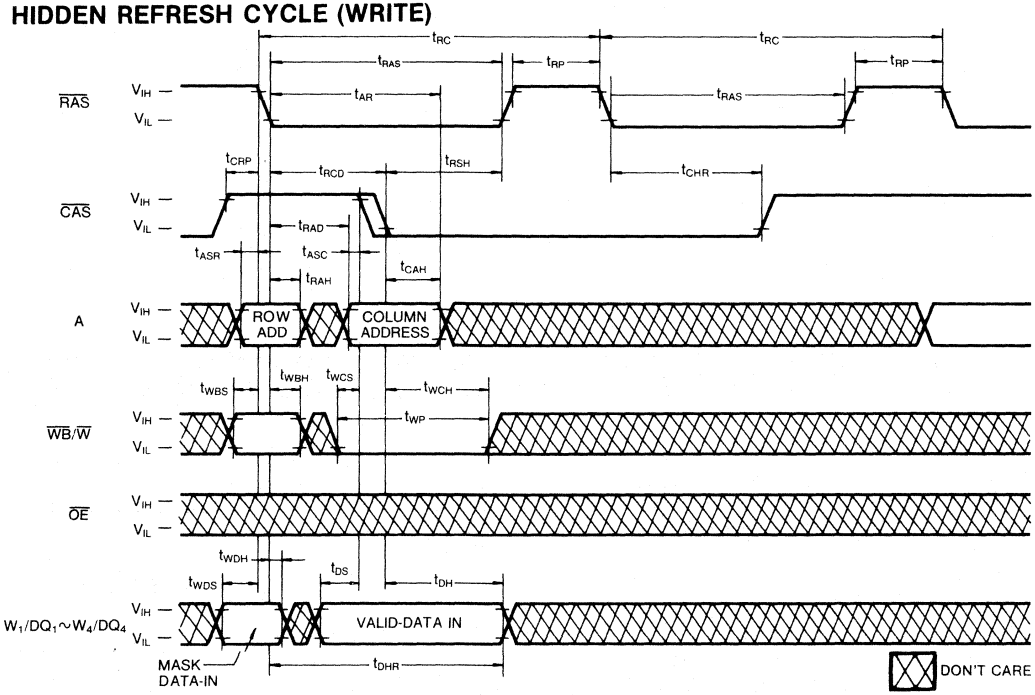


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

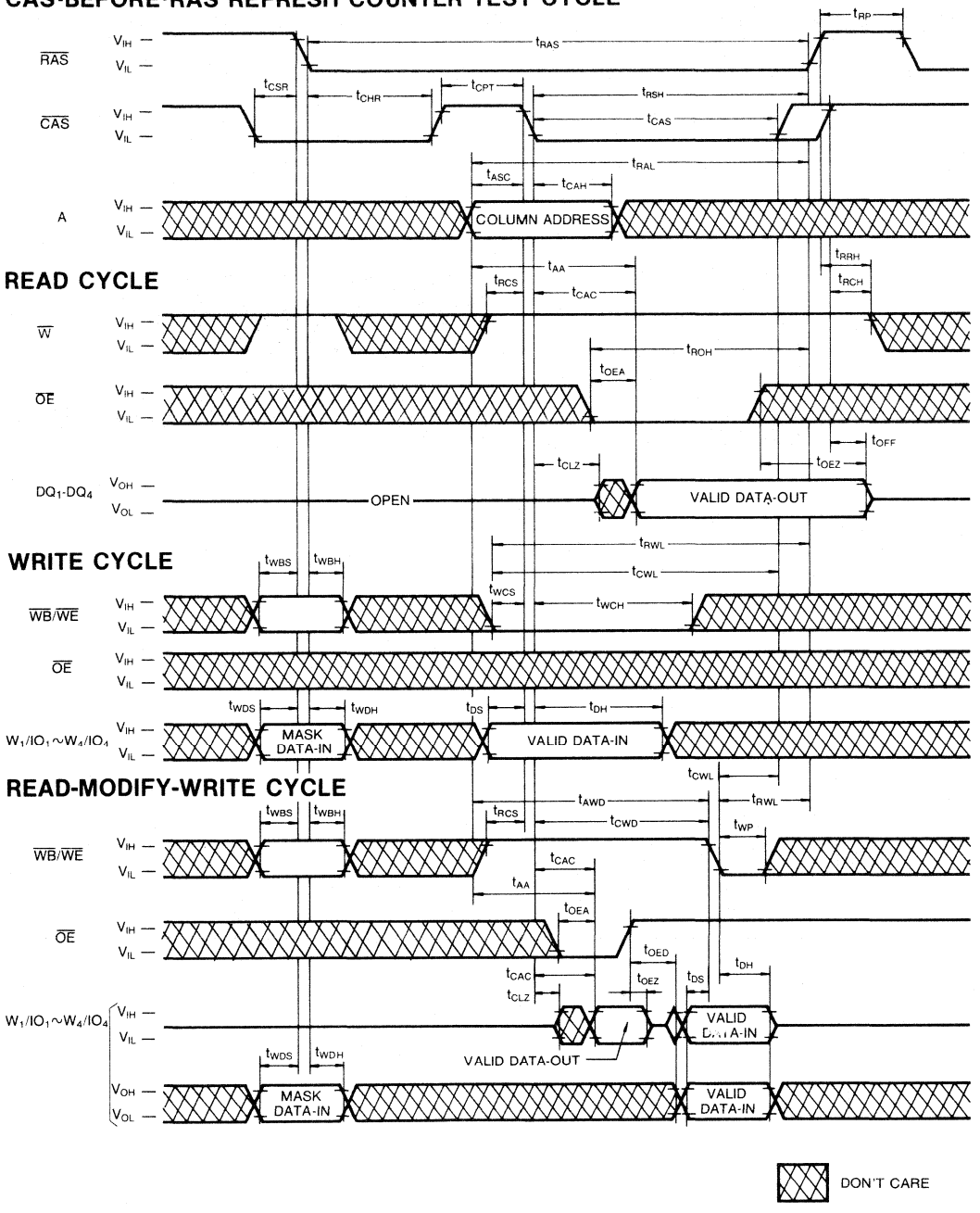


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

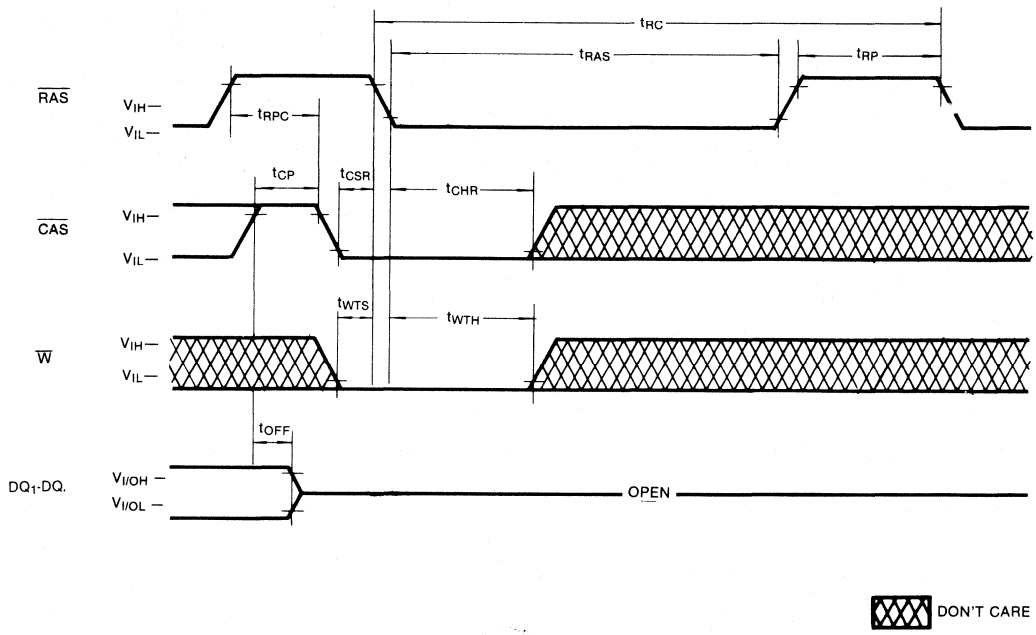


DON'T CARE

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: $\overline{OE}$, Address=Don't Care



TEST MODE DESCRIPTION

The KM44C1010A is the RAM organized 1,048,576 words by 4 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DARM. $\overline{W}$, $\overline{CAS}$-Before-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM44C1010A contains 4,194,304 memory locations. Twenty address bits are required to address a particular memory location. Since the KM44C1010A has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM44C1010A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C1010A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1010A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM44C1010A can perform early write, $\overline{OE}$ controlled write and read-modify-write cycles. Each of these write cycles is achieved by maintaining the write per bit write enable ($\overline{WB}$/$\overline{W}$) input high at the falling edge of $\overline{RAS}$. If write-per bit function is performed, $\overline{WB}$/$\overline{W}$ is kept low at the falling edge of $\overline{RAS}$. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing W low before $\overline{CAS}$. The 4-bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. This output enable input ($\overline{OE}$) must be low during the time defined by t_{OEA} and t_{OEZ} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM44C1010A DQ pins.

Write-Per-Bit

Write-per-bit function is performed in the write cycle, that is early write. $\overline{OE}$ controlled write, read-modify-write. Write-per-bit markes it possible selectively to write one or more of the four I/O pins. To perform write per-bit function at the falling edge of $\overline{RAS}$ the write-per-bit/Write enable ($\overline{WB}$/$\overline{W}$) is kept low and at the same time Mask data of input pins to write among 4 I/O pins must be in high. If I/O pins that Mask data is kept low, write operation is inhibited.

Data Output

The KM44C1010A has a three-state output buffers which are controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in the time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. The is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C1010A operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

DEVICE OPERATION (Continued)

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle, $\overline{OE}$ controlled write.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM44C1010A is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16ms. There are several ways to accomplish this. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C1010A has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C1010A hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1010A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM44C1010A has Fast page mode capability. Fast Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In Fast Page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A Fast Page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page. Up to 2048 memory cells can be accessed with the same row address.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address — Bits A_0 through A_8 are supplied by the on-chip refresh counter. This A_9 bit is set high internally.

Column Address — Bits A_0 through A_9 are strobed-in by the falling edge of CAS as in a normal memory cycle.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

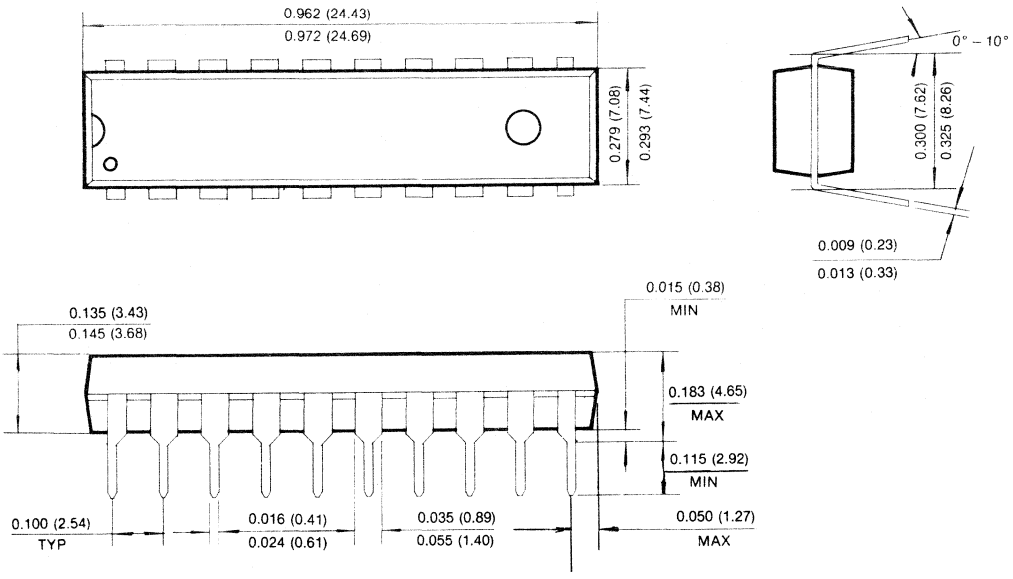
Power-up

If RAS = V_{SS} during power-up, the KM44C1010A could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

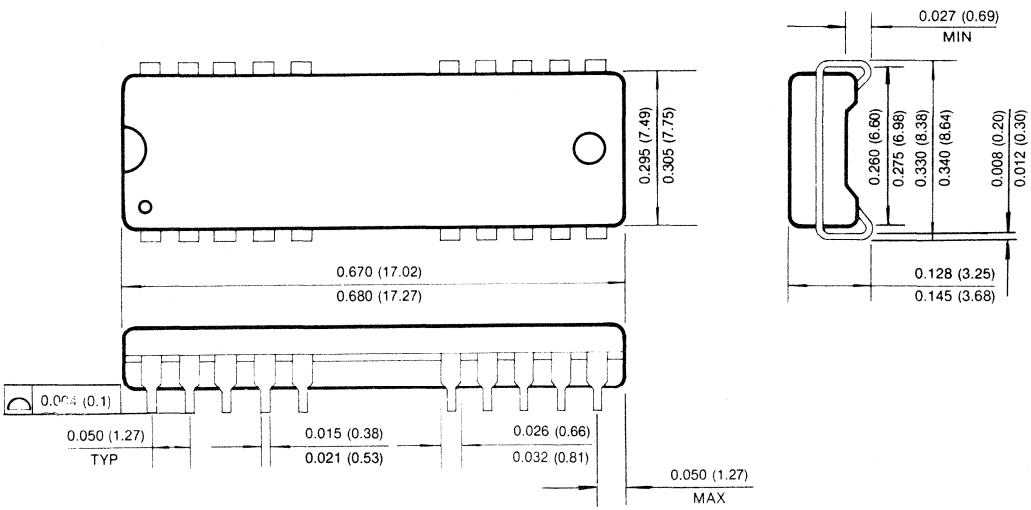
An initial pause of 200 μsec is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE



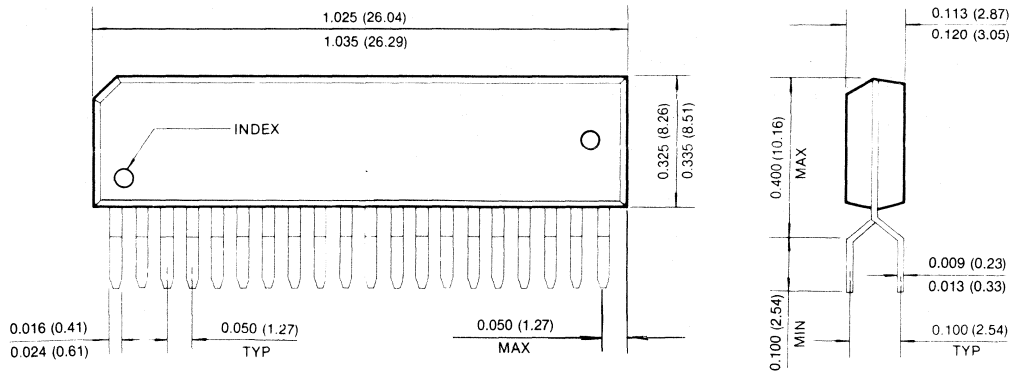
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Unit: Inches (millimeters)



1M×4 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C1002A- 7	70ns	20ns	130ns
KM44C1002A- 8	80ns	20ns	150ns
KM44C1002A-10	100ns	25ns	180ns

- **Static Column Mode operation**
- **$\overline{CS}$-before-$\overline{RAS}$ Refresh Capability**
- **$\overline{RAS}$-only and Hidden Refresh Capability**
- **8-bit fast parallel test mode Capability**
- **TTL compatible inputs and output**
- **Early Write or Output Enable Controlled Write**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, DIP, ZIP**

GENERAL DESCRIPTION

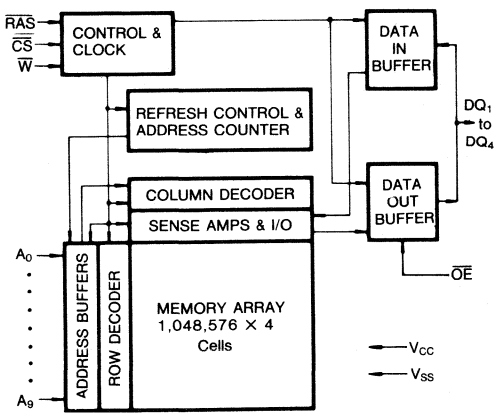
The Samsung KM44C1002A is a high speed CMOS 1,048,576 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C1002A features Static Column Mode operation which allows high speed random or sequential access within a row. Static Column Mode operation offers high performance while relaxing many critical system timing requirements for fast usable speed.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and output are fully TTL compatible.

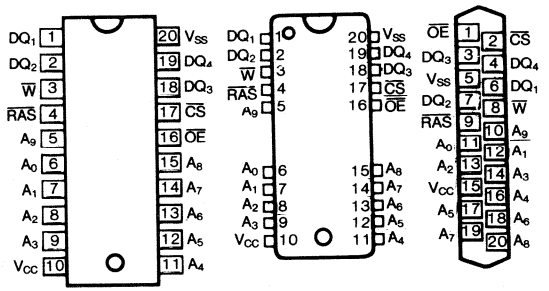
The KM44C1002A is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)

- **KM44C1002AP** - **KM44C1002AJ** - **KM44C1002AZ**



Pin Name	Pin Function
A0-A9	Address Inputs
DQ_1-DQ_4	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, V_{CC}=5.0V±10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CS}$, Address Cycling @ t_{RC}=min)	KM44C1002A- 7	I_{CC1}	—	105	mA
	KM44C1002A- 8		—	95	mA
	KM44C1002A-10		—	85	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}, @ t_{RC}=min)	KM44C1002A- 7	I_{CC3}	—	105	mA
	KM44C1002A- 8		—	95	mA
	KM44C1002A-10		—	85	mA
Static Column Mode Current* ($\overline{RAS}$=$\overline{CS}$=V_{IL}, Address Cycling @t_{SC}=min)	KM44C1002A- 7	I_{CC4}	—	80	mA
	KM44C1002A- 8		—	70	mA
	KM44C1002A-10		—	60	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$≥V_{CC}-0.2V)		I_{CC5}	—	1	mA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @ t_{RC}=min.)	KM44C1002A- 7	I_{CC6}	—	105	mA
	KM44C1002A- 8		—	95	mA
	KM44C1002A-10		—	85	mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CS}$=V_{IL}, D_{OUT}=Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM44C1002A-7		KM44C1002A-8		KM44C1002A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	185		205		245		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3,12
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CS}$ pulse width	t_{CS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	

AC CHARACTERISTICS (Continued)

Standard Operation	Symbol	KM44C1002A-7		KM44C1002A-8		KM44C1002A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CS}$ to write enable delay time	t_{CWD}	50		50		60		ns	8
$\overline{RAS}$ to write enable delay time	t_{RWD}	100		110		135		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	65		70		85		ns	8
$\overline{CS}$ setup time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	
Static column mode cycle time	t_{SC}	40		45		55		ns	
Static column mode read-write cycle time	t_{SRWC}	100		110		135		ns	
Access time from last write	t_{ALW}		65		75		95	ns	3,12
Output data hold time from column address	t_{AOH}	5		5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		45		50		70	ns	
$\overline{RAS}$ pulse width (static column mode)	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CS}$ precharge time (static column mode)	t_{CP}	10		10		10		ns	
Write address hold time reference to $\overline{RAS}$	t_{AWR}	55		60		75		ns	6
Column address hold time referenced to $\overline{RAS}$ rise	t_{AH}	5		5		10		ns	
Last write to column address delay time	t_{LWAD}	20	30	20	35	25	45	ns	
Last write to column address hold time	t_{AHLW}	65		75		95		ns	
Write command inactive time	t_{WI}	10		10		10		ns	
Write command set-up time (Test mode In)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode In)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

TEST MODE CYCLE

(Note. 13)

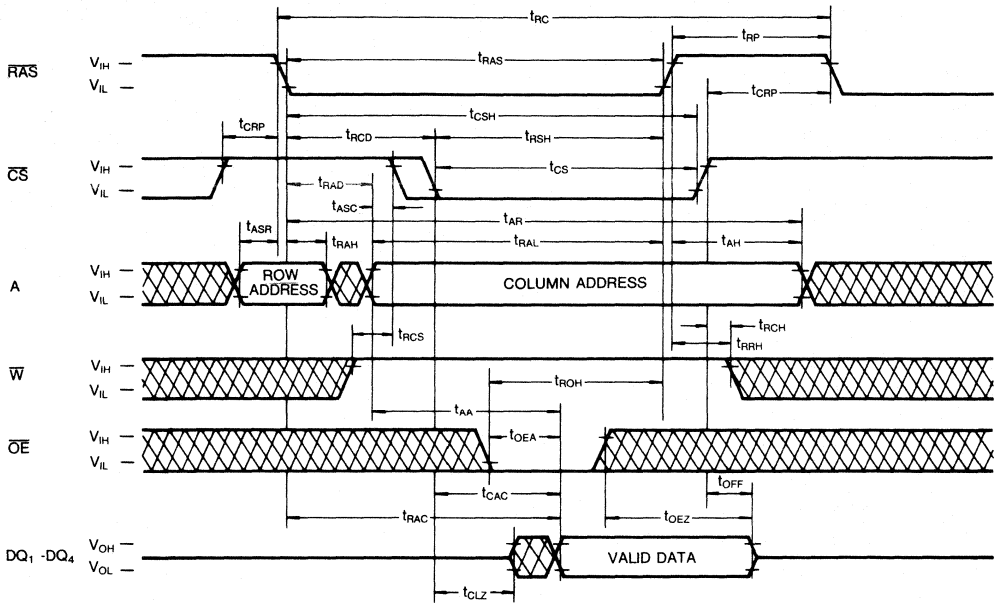
Standard Operation	Symbol	KM44C1002A-7		KM44C1002A-8		KM44C1002A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	135		155		185		ns	
Read-modify-write cycle time	t_{RWC}	185		210		250		ns	
Access time from $\overline{RAS}$	t_{RAC}		75		85		105	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		25		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		45		55	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	75	10,000	85	10,000	105	10,000	ns	
$\overline{CS}$ pulse width	t_{CS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{CS}$ hold time	t_{CSH}	75		85		105		ns	
Column Address to $\overline{RAS}$ lead time	t_{RAL}	40		45		55		ns	
$\overline{CS}$ to write enable delay	t_{CWD}	55		55		65		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	105		115		140		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	70		75		90		ns	8
Static column mode cycle time	t_{SC}	45		50		60		ns	
Static column mode read-modefy-write	t_{SRWC}	105		115		135		ns	
$\overline{RAS}$ pulse width (static column mode)	t_{RASC}	75	100,000	85	100,000	105	100,000	ns	
Access time from last write	t_{ALW}		70		80		100	ns	3,12
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	25	100,000	25	100,000	30	100,000	ns	
$\overline{OE}$ access time	t_{OEA}		25		25		30	ns	
$\overline{OE}$ to data delay	t_{OED}	25		25		30		ns	
$\overline{OE}$ command hold time	t_{OEH}	25		25		30		ns	

NOTES

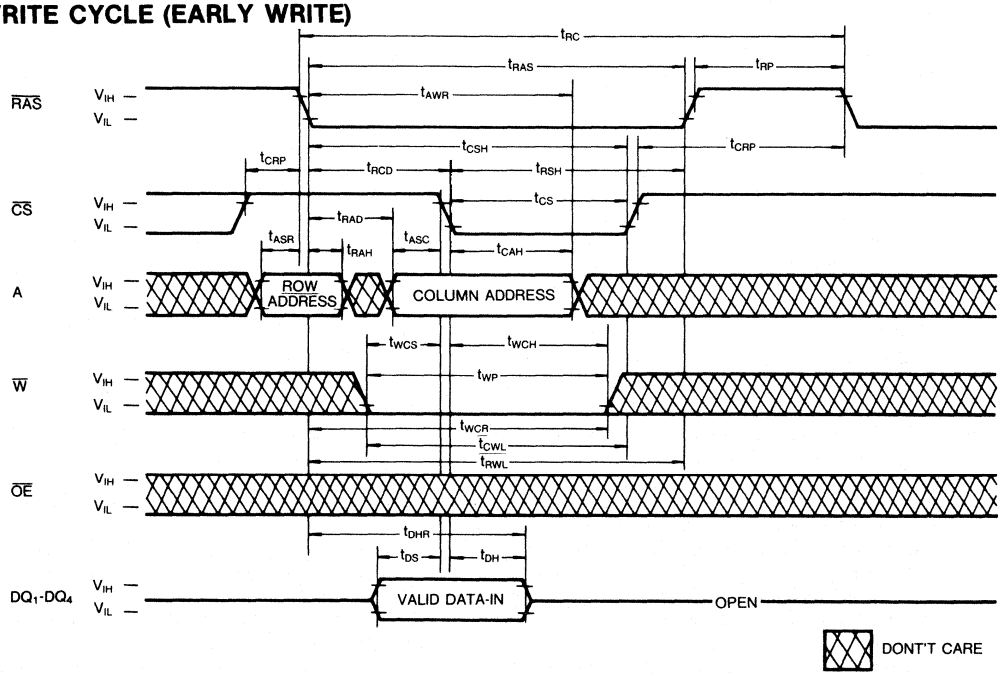
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AWR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. Operation within the $t_{LWAD(max)}$ limit insures that $t_{ALW(max)}$ can be met. $t_{LWAD(max)}$ is specified as a reference point only. t_{LWAD} is greater than the specified $t_{LWAD(max)}$ limit, then access time is controlled by t_{AA}.
13. These specifications are applied in the test mode.

TIMING DIAGRAMS

READ CYCLE

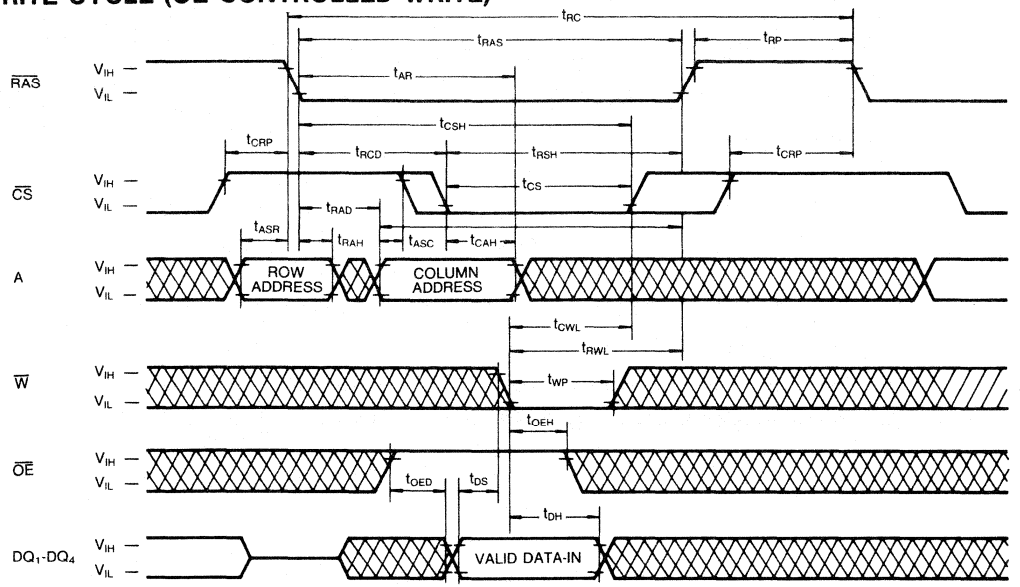


WRITE CYCLE (EARLY WRITE)

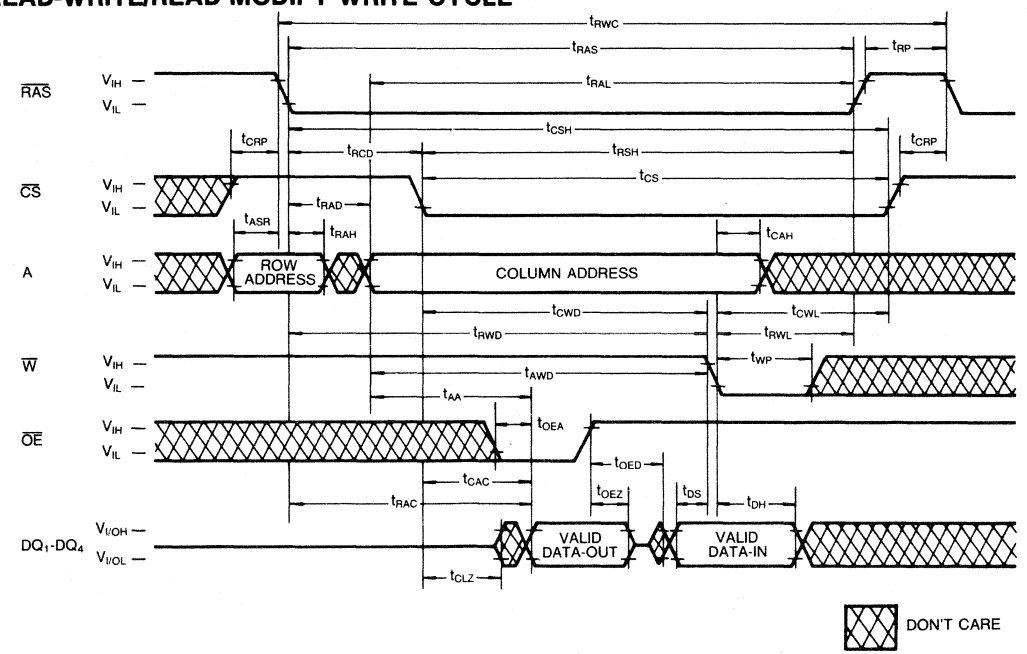


TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

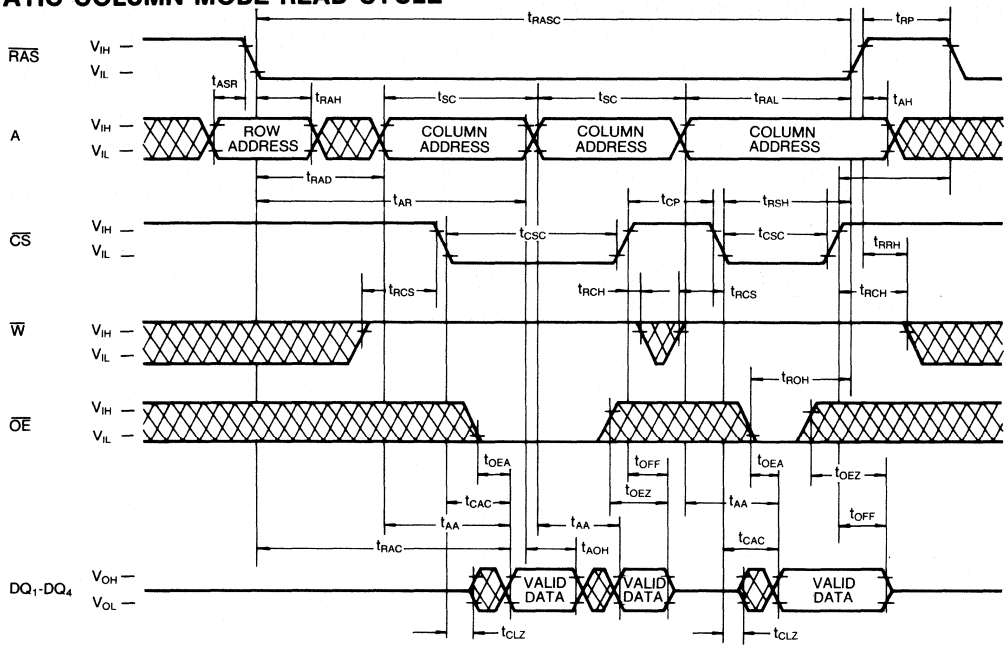


READ-WRITE/READ-MODIFY-WRITE CYCLE

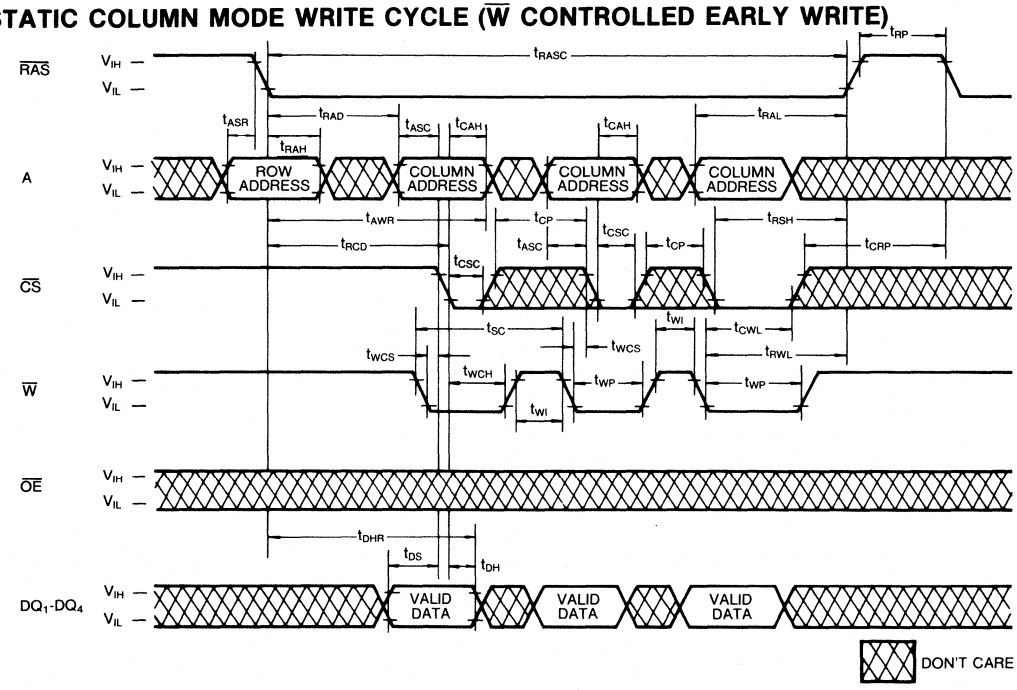


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ CYCLE

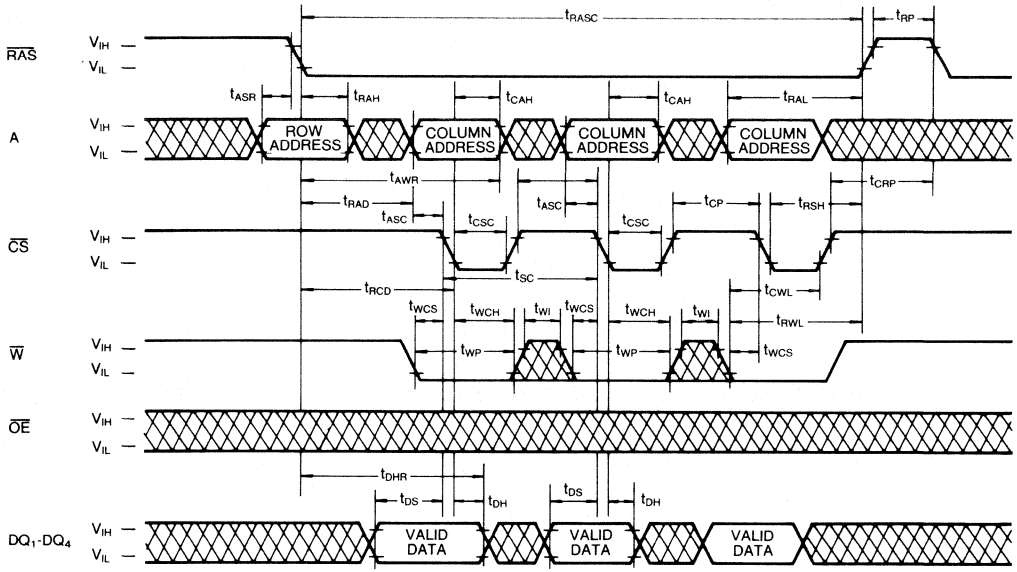


STATIC COLUMN MODE WRITE CYCLE (W CONTROLLED EARLY WRITE)

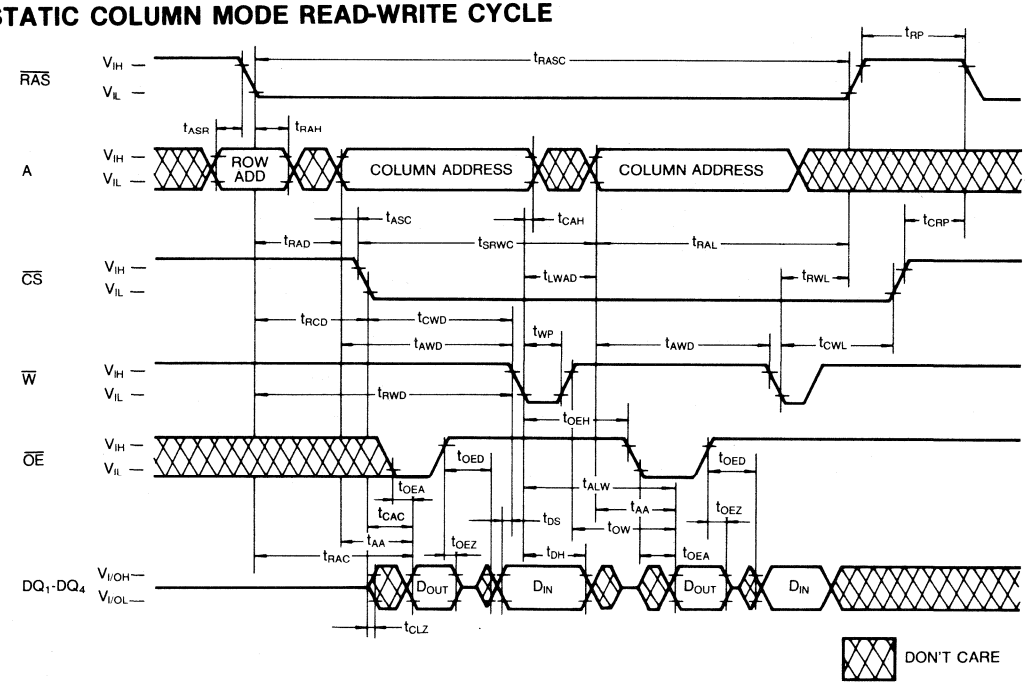


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ CONTROLLED EARLY WRITE)

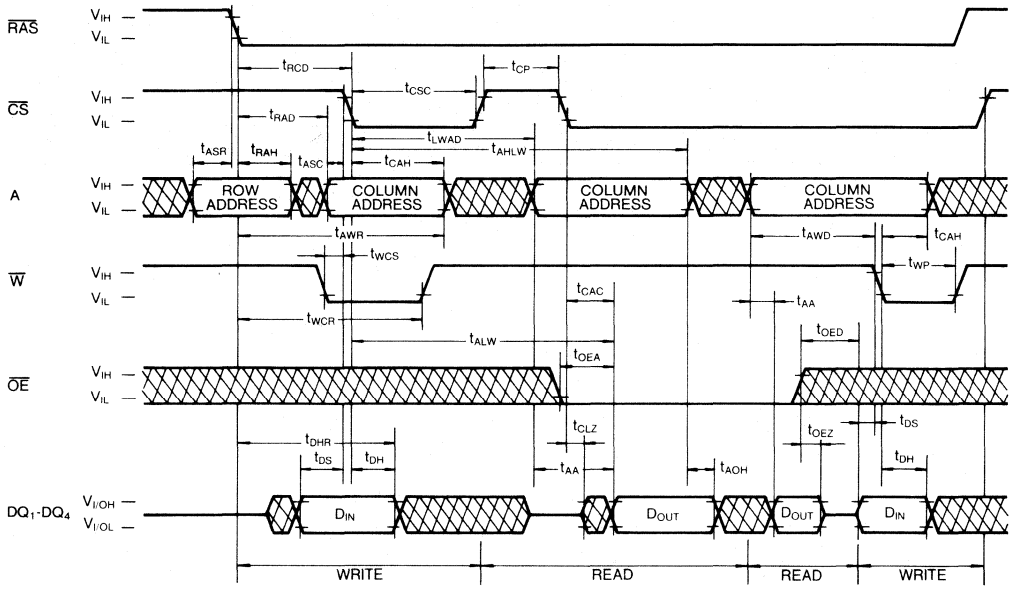


STATIC COLUMN MODE READ-WRITE CYCLE



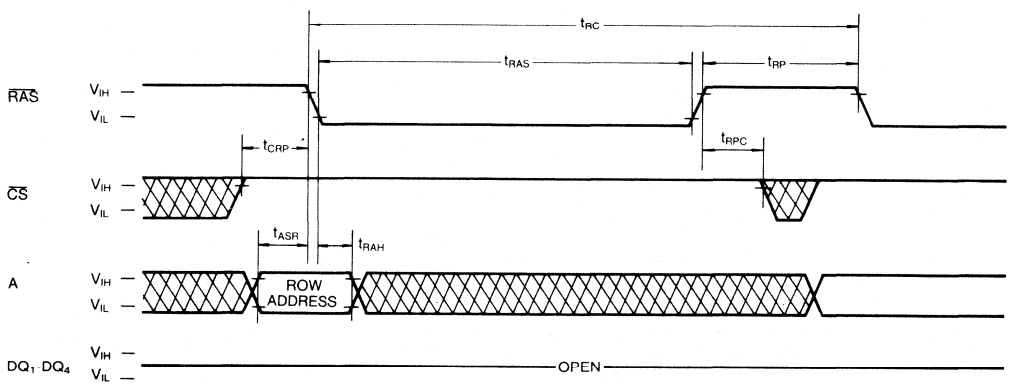
TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE MIXED CYCLE



RAS-ONLY REFRESH CYCLE

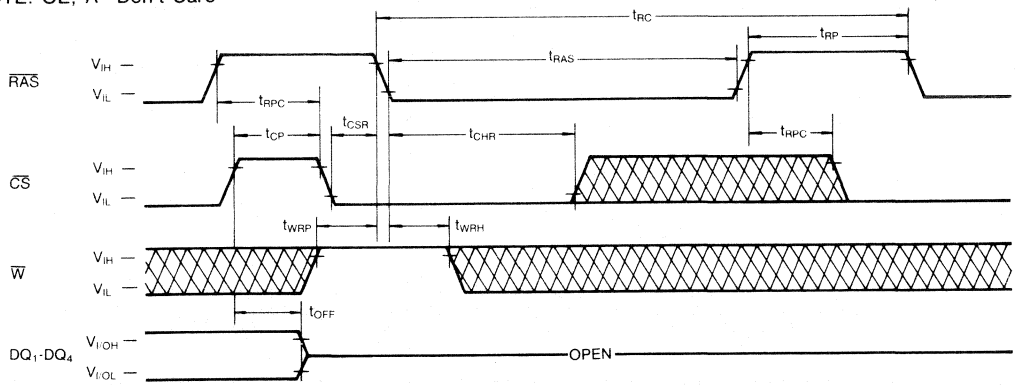
NOTE: W, OE==Don't Care



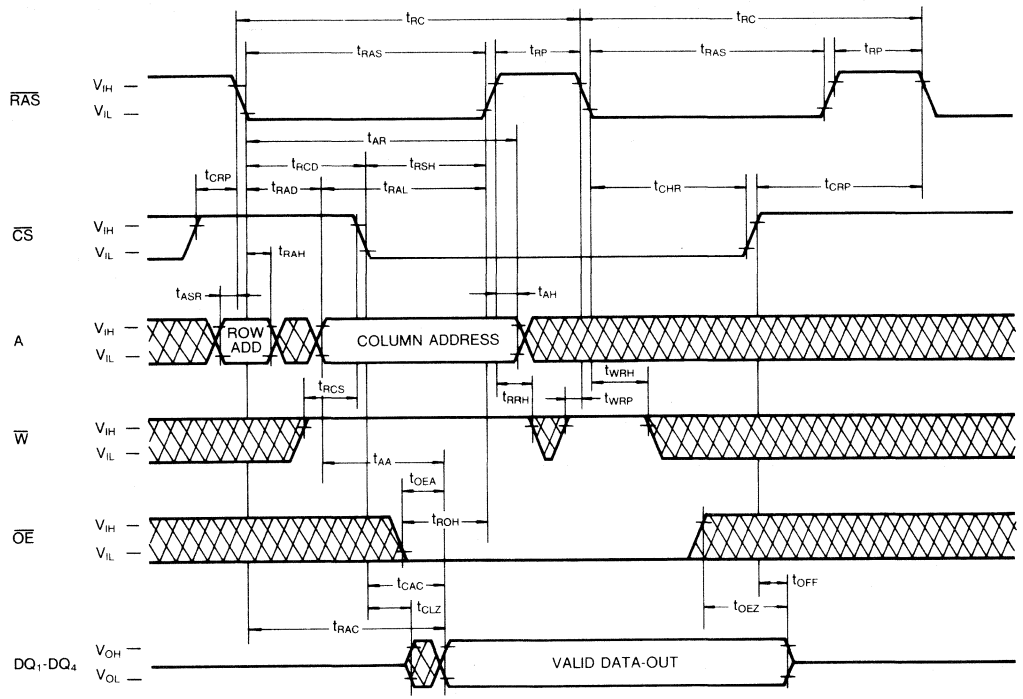
TIMING DIAGRAMS (Continued)

$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{OE}$, A=Don't Care

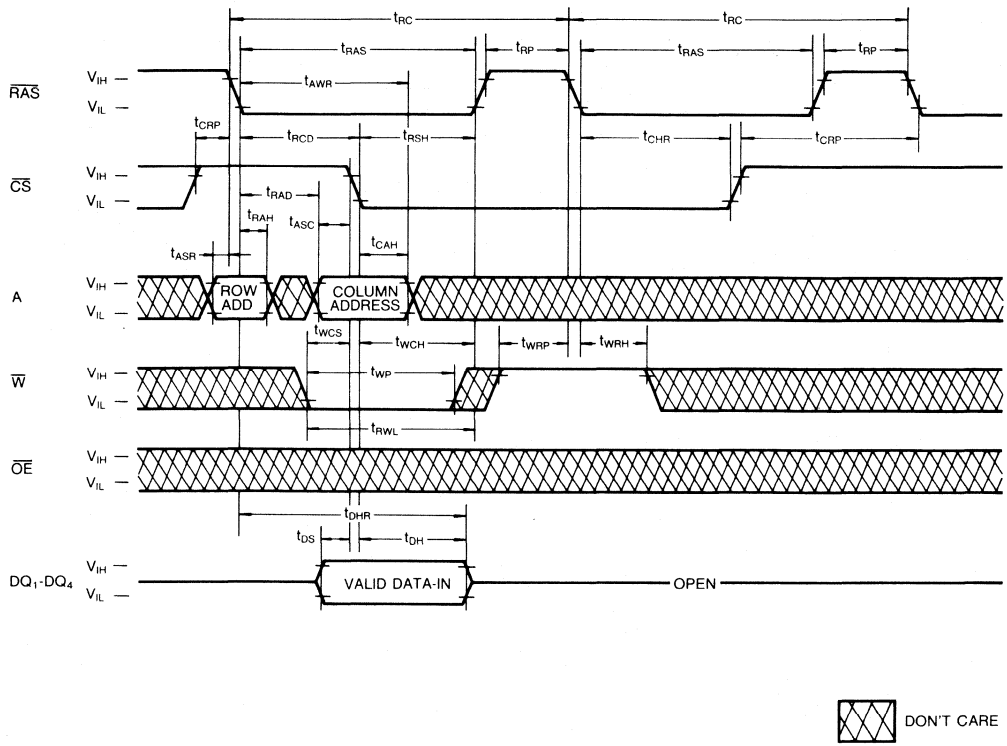


HIDDEN REFRESH CYCLE (READ)



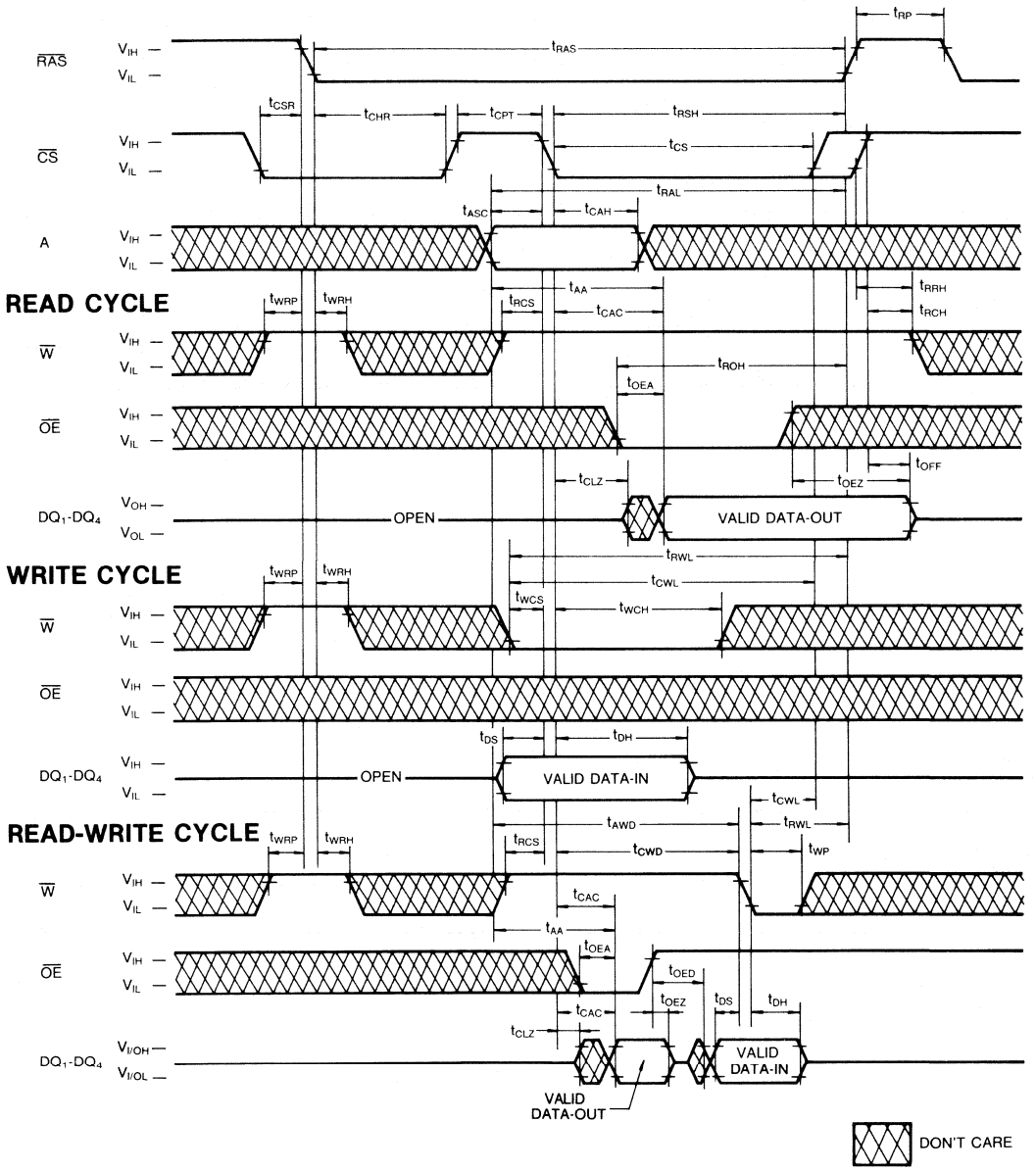
TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

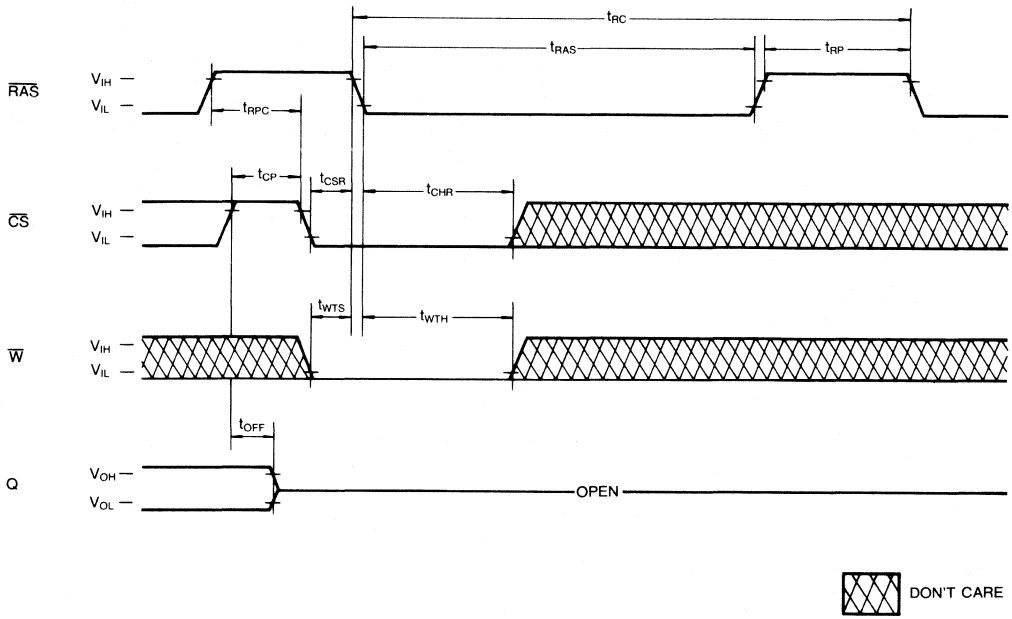
$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address=Don't Care



TEST MODE DESCRIPTION

The KM44C1002A is the RAM organized 1,048,576 words by 4 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM. $\overline{W}$, $\overline{CS}$ Before $\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATIONS

Device Operation

The KM44C1002A contains 4,194,304 memory locations organized as 1,048,576 four-bit words. Twenty address bits are required to address a particular 4-bit word in the memory location. Since the KM44C1002A has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the chip select input ($\overline{CS}$) and the valid row and column address inputs.

Operating of the KM44C1002A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CS}$. This is the beginning of any KM44C1002A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths are specified by t_{RAS}(min) and t_{CS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1002A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CS}$ and on the valid column address transition.

If $\overline{CS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

The KM44C1002A has common data I/O pins. For this reason and output enable control input ($\overline{OE}$) has been proviced so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44C1002A can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CS}$ and meeting the data sheet read-modify-write cycle timing requirements. The output enable input ($\overline{OE}$) must be low during the time defined by t_{OEA} and t_{OEZ} for data to appear at the output. If t_{CWD} and t_{RWD} are not met the output may contain invalid data. Conforming to the $\overline{OE}$ timing equirement prevents bus contention on the KM44C1002A's DQ pins.

Data Output

The KM44C1002A has a three-state output buffer which is controlled by $\overline{CS}$ and $\overline{OE}$. Whenever $\overline{CS}$ or $\overline{OE}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C1002A operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Static Column Read, Static Column Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Static Column Mode Write, $\overline{CS}$-before-$\overline{RAS}$ Refresh, $\overline{CS}$-only cycle. $\overline{OE}$ Controlled write.
Indeterminate Output State: Delayed Write

DEVICE OPERATIONS (Continued)

Refresh

The data in the KM44C1002A is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CS}$ remains high. This cycle must be repeated for each row.

$\overline{CS}$-before-$\overline{RAS}$ Refresh: The KM44C1002A has $\overline{CS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CS}$ active time and cycling $\overline{RAS}$. The KM44C1002A hidden refresh cycle is actually a $\overline{CS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1002A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CS}$-before-$\overline{RAS}$ refresh is the preferred method.

Static Column Mode

Static Column Mode allows high speed read, write or read-modity-write random access to all the memory cells within a selected row. Operation within a selected row is similar to a static RAM. The read, write or readmodify-write cycles may be mixed in any order.

A Static Column mode read cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{W}=V_{IH}$ and $\overline{RAS}=V_{IL}$.

A Static Column mode write cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{RAS}=V_{IL}$ and toggiling either $\overline{W}$ or $\overline{CS}$. The data is written into the cell trigered by the latter fallin edge of $\overline{W}$ or $\overline{CS}$.

$\overline{CS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{CS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter.

Column Address—Bits A_0 through A_9 are strobed-in by the falling edge of $\overline{CS}$ as in a normal memory cycle.

Suggested $\overline{CS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 512 times so that highs are written into the 512 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

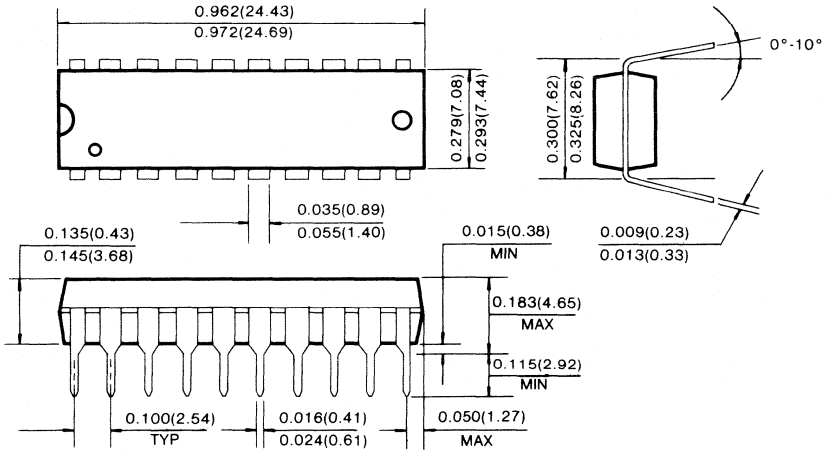
If $\overline{RAS}=V_{SS}$ during power-up, the KM44C1002A could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycle before proper device operation is achieved.

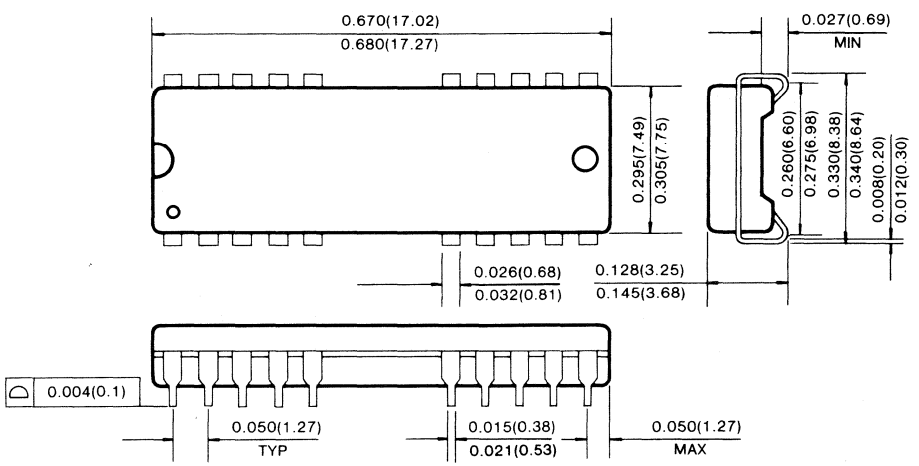
PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

Unit: Inches (Millimeters)



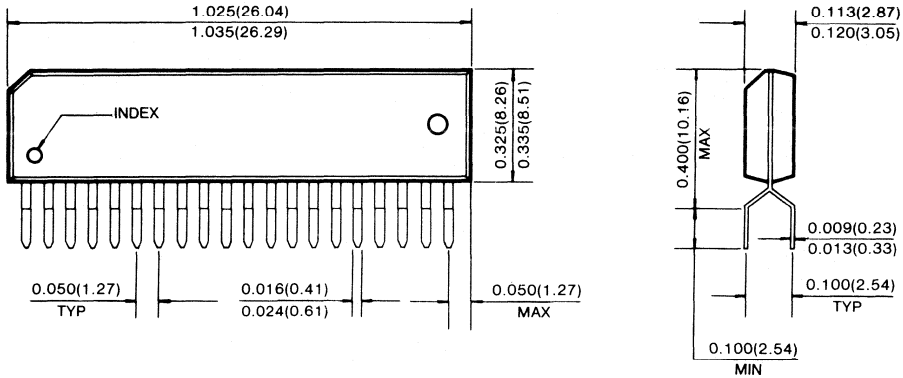
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)



1M x 4 Bit CMOS Dynamic RAM with Static Column Mode (Write Per Bit Mode)

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C1012A-7	70ns	20ns	130ns
KM44C1012A-8	80ns	20ns	150ns
KM44C1012A-10	100ns	25ns	180ns

- **Static Column Mode operation**
- **Write Per Bit Mode capability**
- **$\overline{CS}$-before-$\overline{RAS}$ Refresh Capability**
- **$\overline{RAS}$-only and Hidden Refresh Capability**
- **8-bit fast parallel test mode Capability**
- **TTL compatible inputs and output**
- **Early Write or Output Enable Controlled Write**
- **Single +5V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in Plastic SOJ, DIP and ZIP**

GENERAL DESCRIPTION

The Samsung KM44C1012A is a CMOS high speed 1,048,576 bit x 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

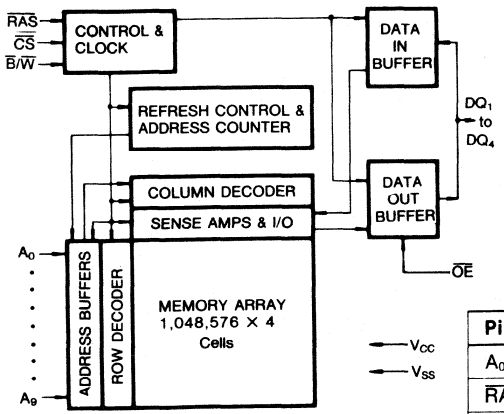
The KM44C1012A features Static Column Mode operation which allows high speed random or sequential access within a row. Static Column Mode operation offers high performance while relaxing many critical system timing requirements for fast usable speed.

$\overline{CS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM44C1012A is fabricated using Samsung's advanced CMOS process.

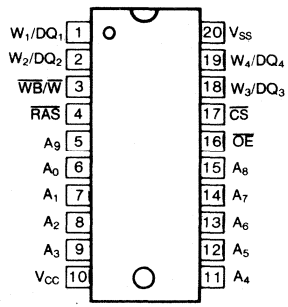
2

FUNCTIONAL BLOCK DIAGRAM

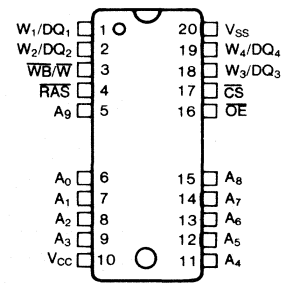


PIN CONFIGURATION (Top Views)

- **KM44C1002AP**

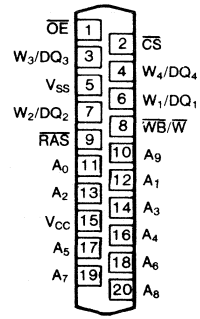


- **KM44C1002AJ**



Pin Name	Pin Function
A_0-A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
$\overline{WB}/\overline{W}$	Write Per Bit/Read/Write Input
$\overline{OE}$	Data Output Enable
W_1/DQ_1~ W_4/DQ_4	Write Select/Data In, Out
V_{CC}	Power (+5V)
V_{SS}	Ground

- **KM44C1002AZ**



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, V_{CC}=5.0V±10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CS}$, Address Cycling @ t_{RC}=min)	KM44C1012A-7	I_{CC1}	—	105	mA
	KM44C1012A-8		—	95	mA
	KM44C1012A-10		—	85	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}, @ t_{RC}=min)	KM44C1012A-7	I_{CC3}	—	105	mA
	KM44C1012A-8		—	95	mA
	KM44C1012A-10		—	85	mA
Static Column Mode Current* ($\overline{RAS}$=$\overline{CS}$=V_{IL}, Address Cycling @t_{SC}=min)	KM44C1012A-7	I_{CC4}	—	80	mA
	KM44C1012A-8		—	70	mA
	KM44C1012A-10		—	60	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$≥V_{CC}-0.2V)		I_{CC5}	—	1	mA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @ t_{RC}=min.)	KM44C1012A-7	I_{CC6}	—	105	mA
	KM44C1012A-8		—	95	mA
	KM44C1012A-10		—	85	mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CS}$=V_{IL}, D_{OUT}=Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test=0 volts.)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Standard Operation	Symbol	KM44C1002A-7		KM44C1002A-8		KM44C1002A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	185		205		245		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3,12
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CS}$ pulse width	t_{CS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	KM44C1012A-7		KM44C1012A-8		KM44C1012A-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CS}$ to write enable delay	t_{CWD}	50		50		60		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	100		110		135		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	60		70		85		ns	8
$\overline{CS}$ setup time ($\overline{CS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10		10		10		ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter test)	t_{CPT}	35		40		50		ns	
Static column mode cycle time	t_{SC}	40		45		55		ns	
Static column mode read-write cycle time	t_{SRWC}	100		110		135		ns	
Access time from last write	t_{ALW}		65		75		95	ns	3,12
Output data hold time from column address	t_{AOH}	5		5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		45		50		70	ns	
$\overline{RAS}$ pulse width (static column mode)	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CS}$ precharge time (static column mode)	t_{CP}	10		10		10		ns	
Write address hold time reference to $\overline{RAS}$	t_{AWR}	55		60		75		ns	6
Column address hold time referenced to $\overline{RAS}$ rise	t_{AH}	5		5		10		ns	
Last write to column address delay time	t_{LWAD}	20	30	20	35	25	45	ns	
Last write to column address hold time	t_{AHLW}	65		75		95		ns	
Write command inactive time	t_{WI}	10		10		10		ns	
Write command set-up time (test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (testt mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	
Write per bit set-up time	t_{WBS}	0		0		0		ns	
Write per bit hold time	t_{WBH}	10		15		15		ns	
Write per bit selection set-up time	t_{WDS}	0		0		0		ns	
Write per bit selection hold time	t_{WDH}	10		15		15		ns	

TEST MODE CYCLE

(Note. 13)

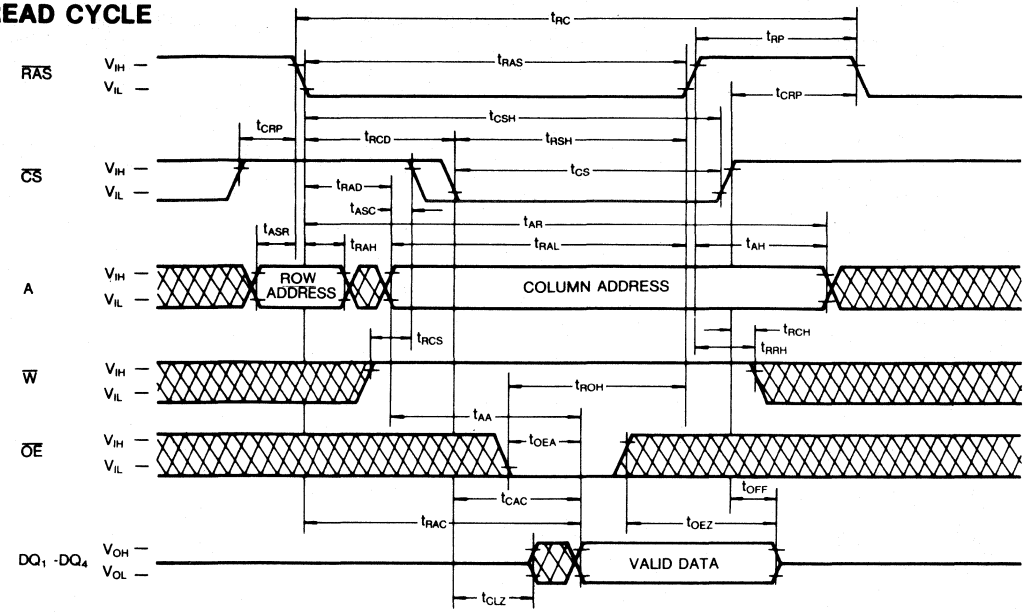
Standard Operation	Symbol	KM44C1002A-7		KM44C1002A-8		KM44C1002A-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	135		155		185		ns	
Read-modify-write cycle time	t_{RWC}	185		210		250		ns	
Access time from $\overline{RAS}$	t_{RAC}		75		85		105	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		25		25		30	ns	3,4,5
Access time from column address	t_{AA}		40		45		55	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	75	10,000	85	10,000	105	10,000	ns	
$\overline{CS}$ pulse width	t_{CS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		25		30		ns	
$\overline{CS}$ hold time	t_{CSH}	75		85		105		ns	
Column Address to $\overline{RAS}$ lead time	t_{RAL}	40		45		55		ns	
$\overline{CS}$ to write enable delay	t_{CWD}	55		55		65		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	105		115		140		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	70		75		90		ns	8
Static column mode cycle time	t_{SC}	45		50		60		ns	
Static column mode read-modefy-write	t_{SRWC}	105		115		135		ns	
$\overline{RAS}$ pulse width (static column mode)	t_{RASC}	75	100,000	85	100,000	105	100,000	ns	
Access time from last write	t_{ALW}		70		80		100	ns	3,12
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	25	100,000	25	100,000	30	100,000	ns	
$\overline{OE}$ access time	t_{OEA}		25		25		30	ns	
$\overline{OE}$ to data delay	t_{OED}	25		25		30		ns	
$\overline{OE}$ command hold time	t_{OEH}	25		25		30		ns	

NOTES

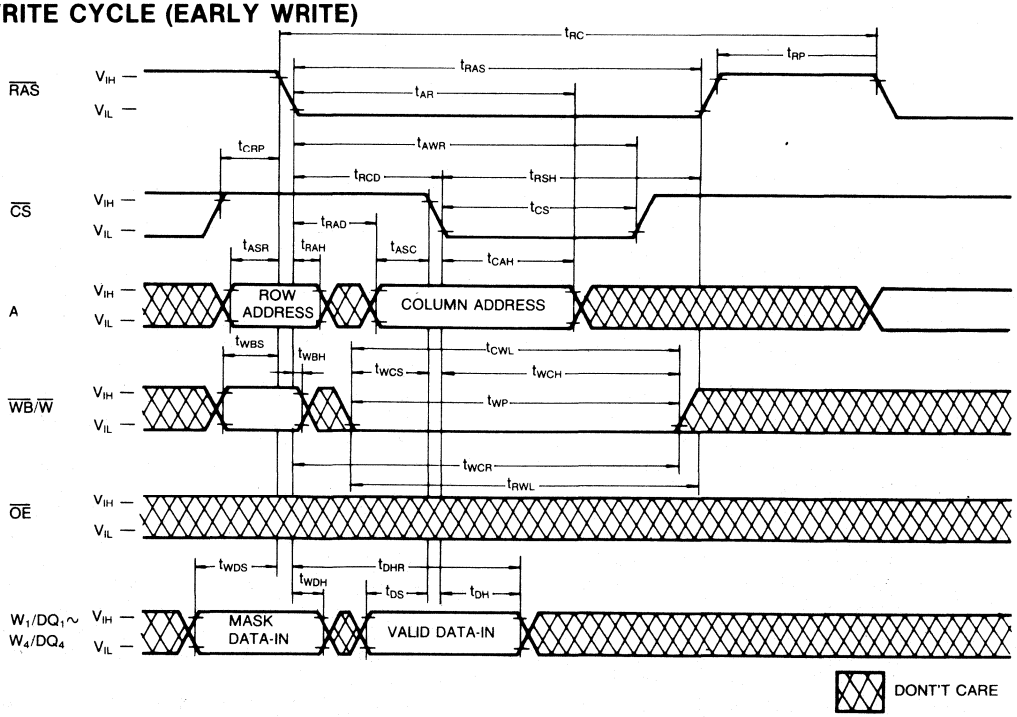
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AWR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. Operation within the $t_{LWAD(max)}$ limit insures that $t_{ALW(max)}$ can be met. $t_{LWAD(max)}$ is specified as a reference point only. t_{LWAD} is greater than the specified $t_{LWAD(max)}$ limit, then access time is controlled by t_{AA}.
13. These specifications are applied in the test mode.

TIMING DIAGRAMS

READ CYCLE

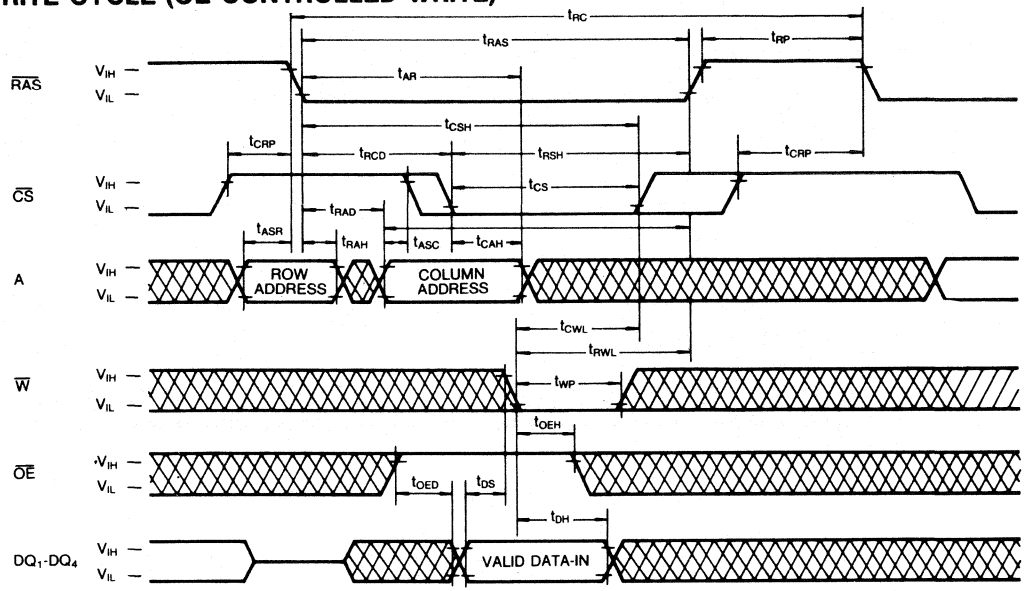


WRITE CYCLE (EARLY WRITE)

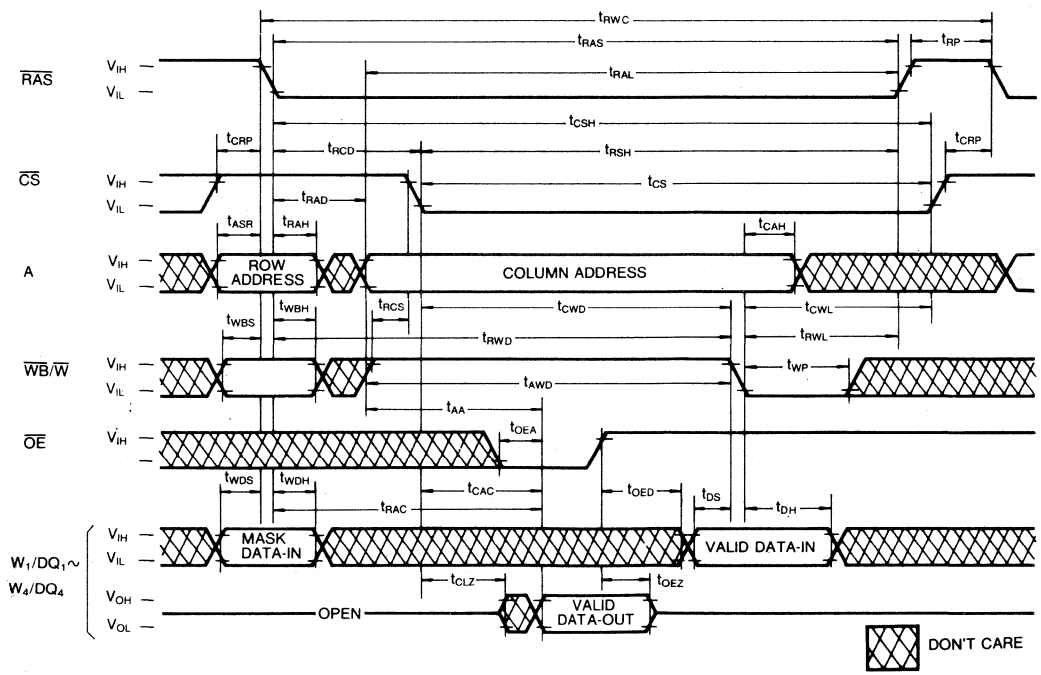


TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

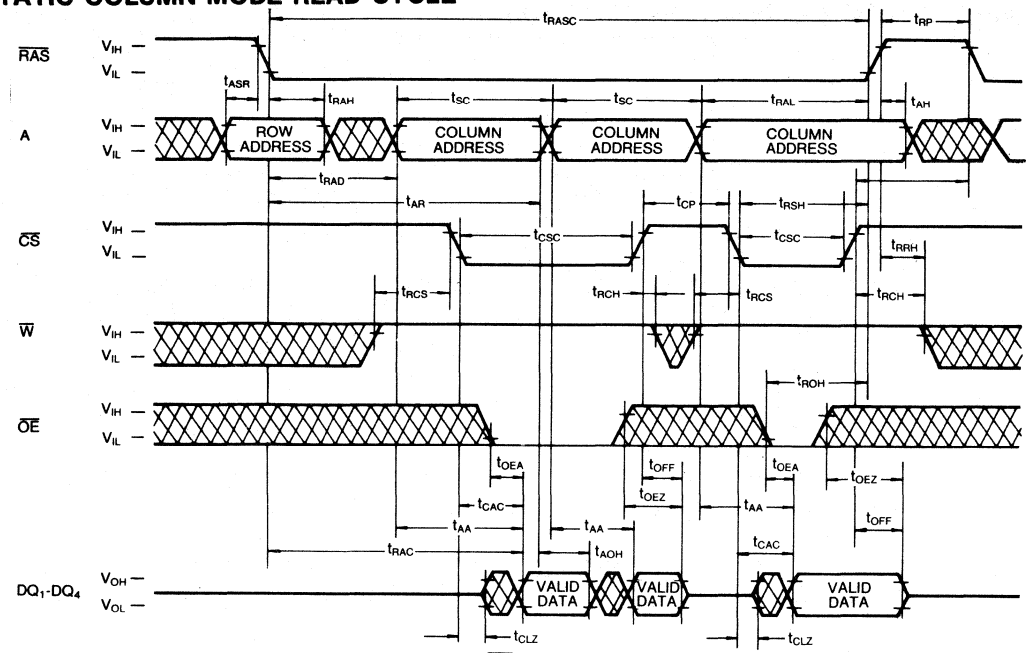


READ-WRITE/READ-MODIFY-WRITE CYCLE

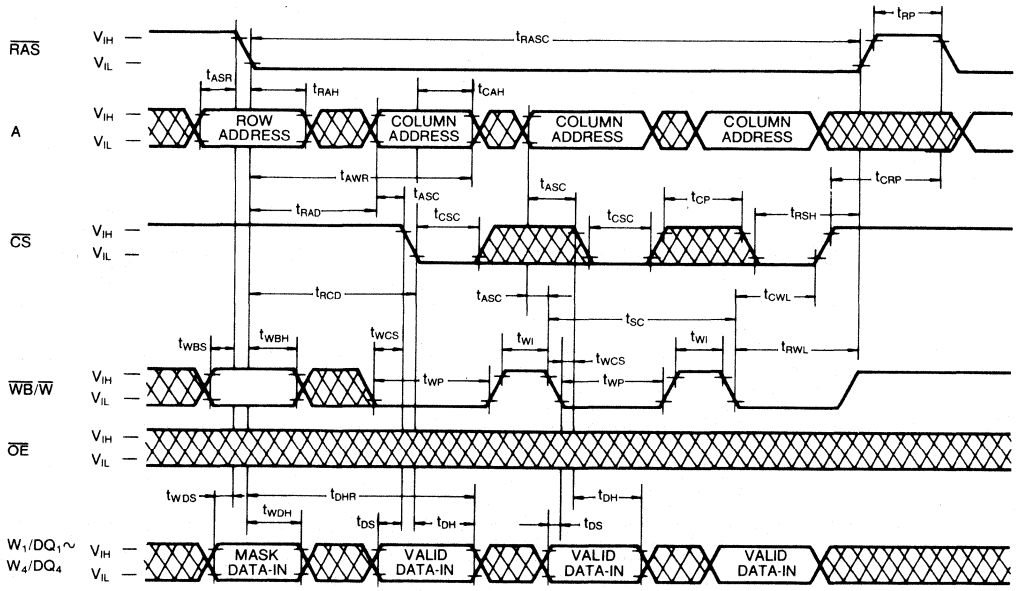


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ CYCLE

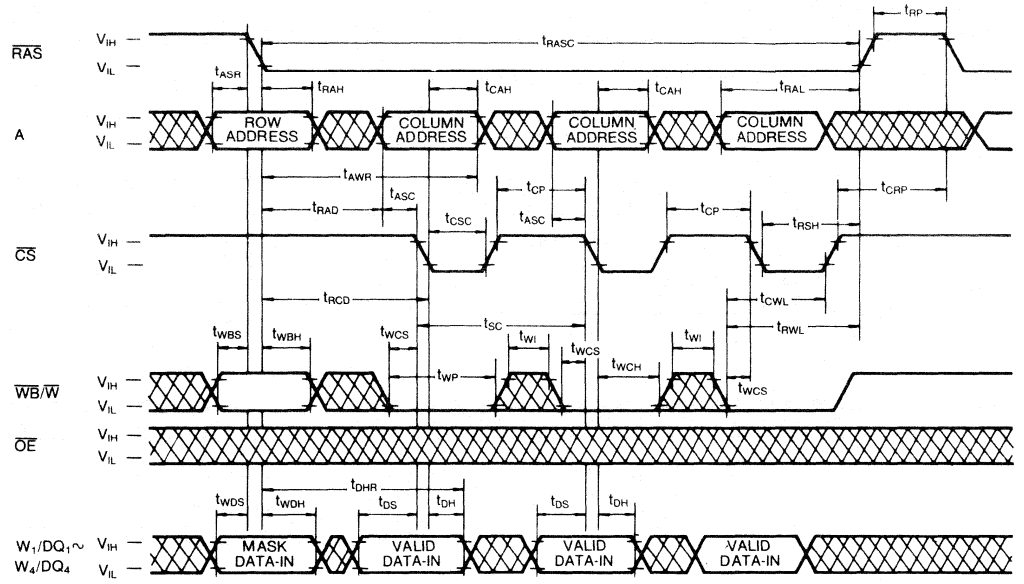


STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ CONTROLLED EARLY WRITE)

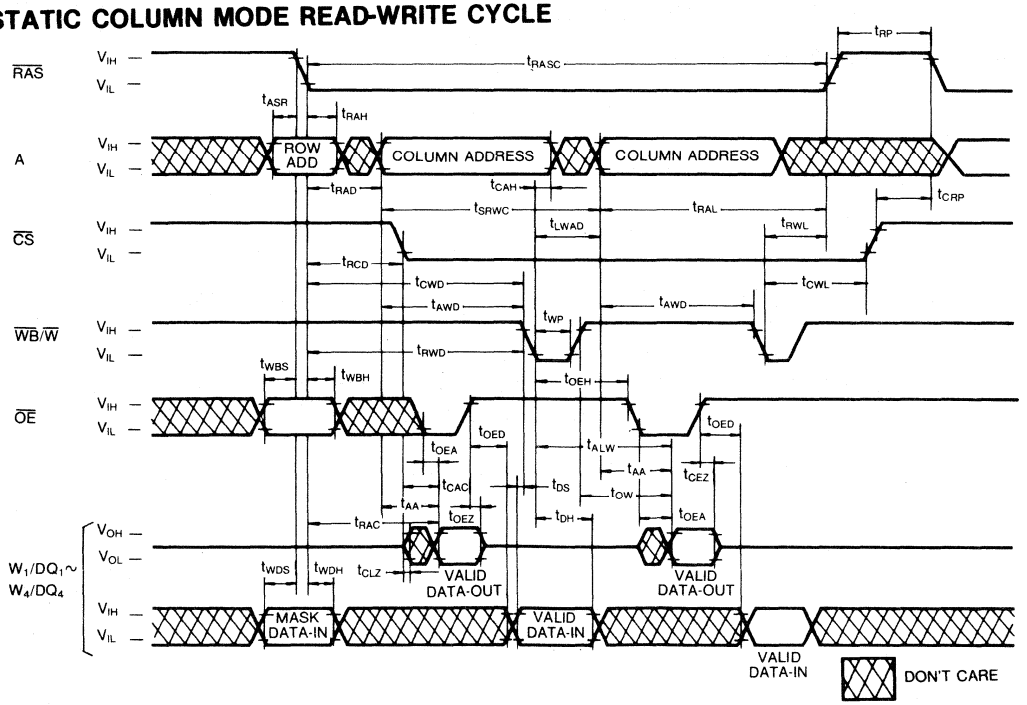


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ CONTROLLED EARLY WRITE)

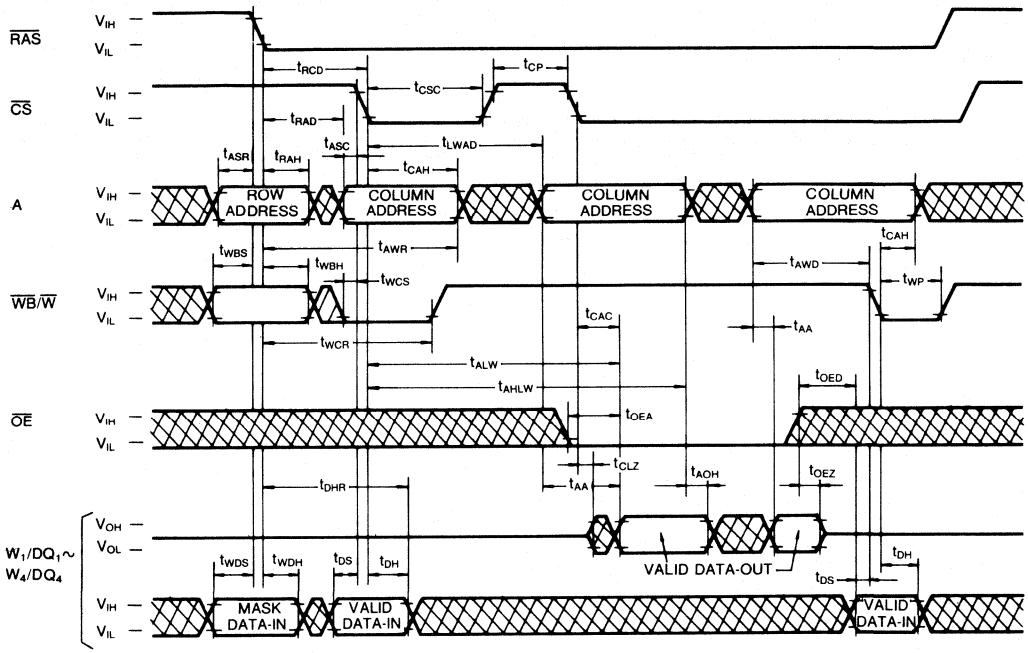


STATIC COLUMN MODE READ-WRITE CYCLE



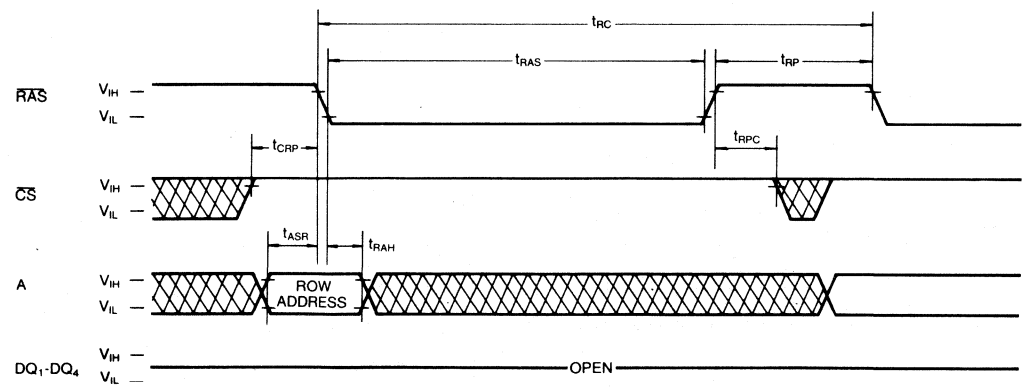
TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE MIXED CYCLE



RAS-ONLY REFRESH CYCLE

NOTE: W, OE==Don't Care

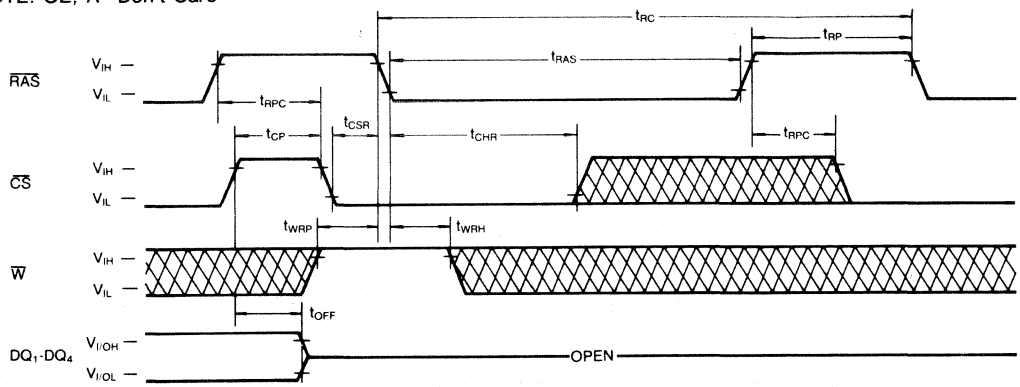


DON'T CARE

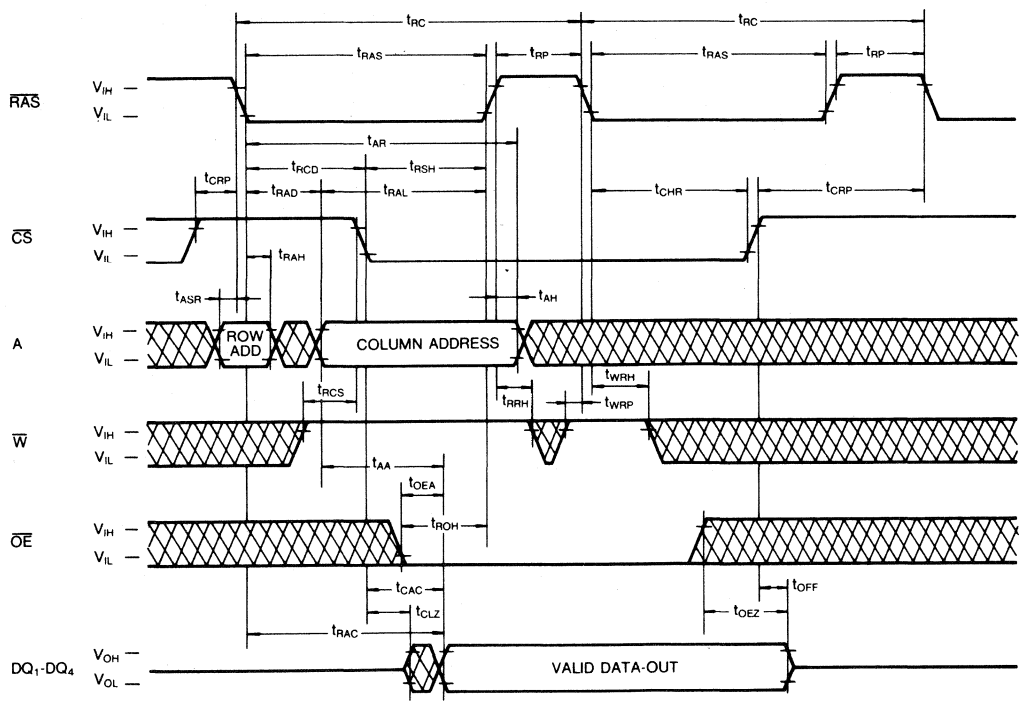
TIMING DIAGRAMS (Continued)

$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{OE}$, A=Don't Care

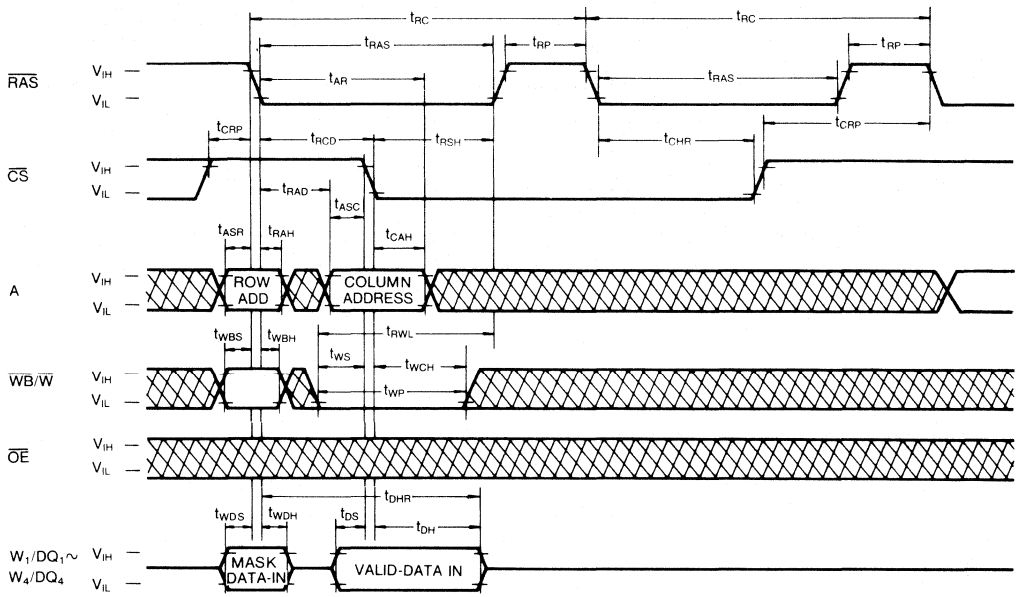


HIDDEN REFRESH CYCLE (READ)



TIMING DIAGRAMS (Continued)

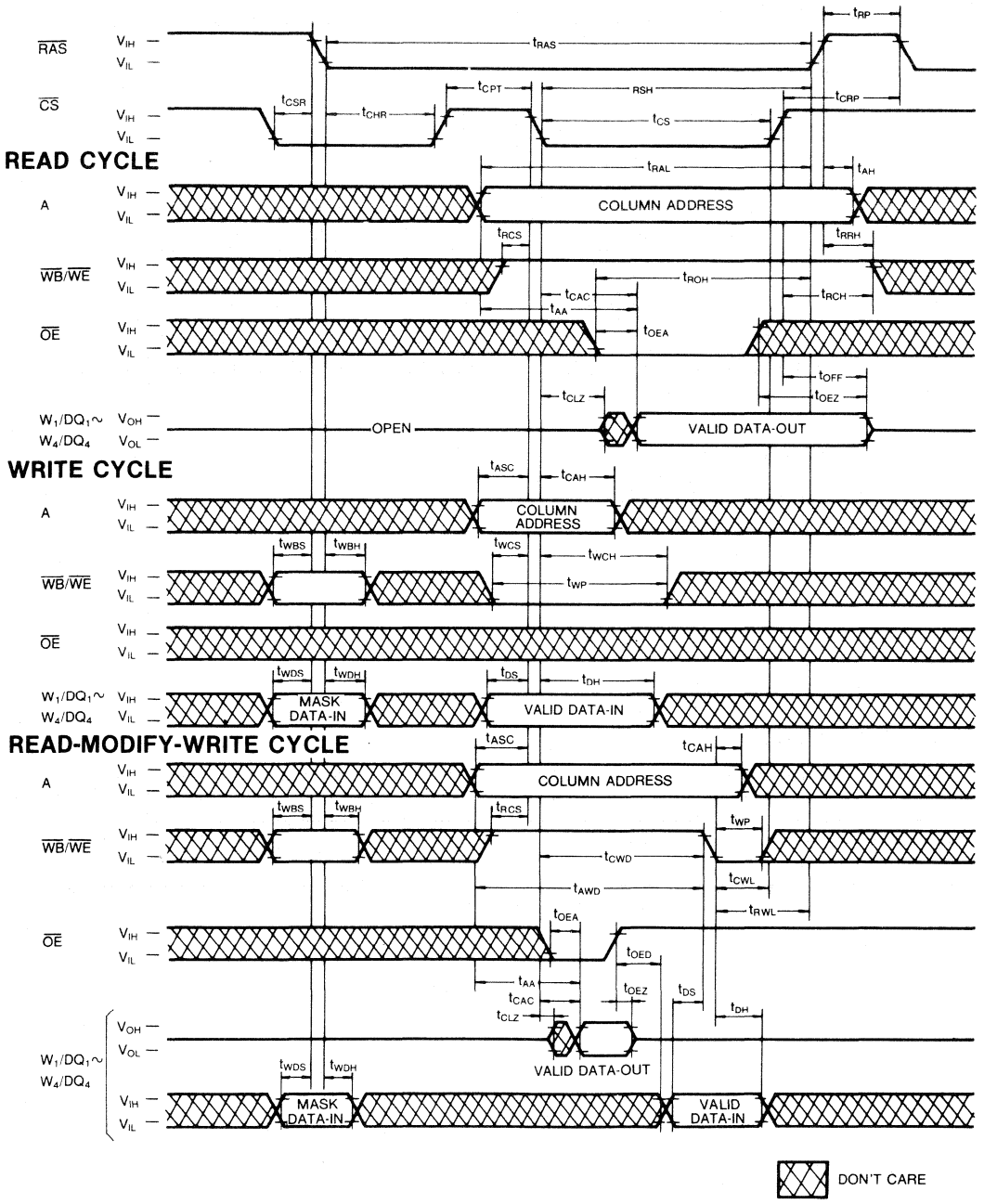
HIDDEN REFRESH CYCLE (WRITE)



DON'T CARE

TIMING DIAGRAMS (Continued)

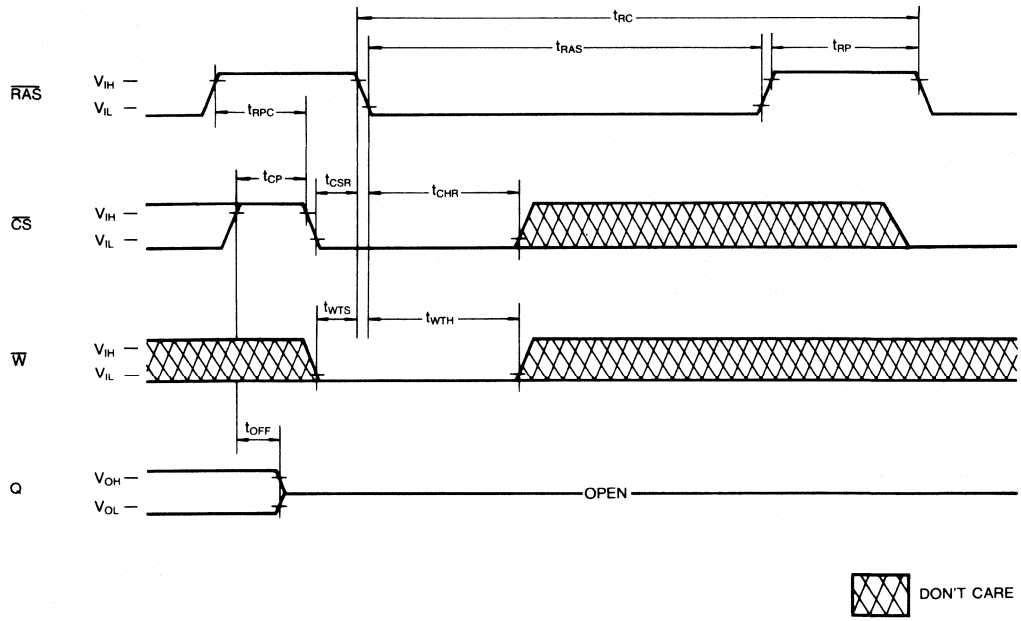
$\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address=Don't Care



TEST MODE DESCRIPTION

The KM44C1012A is the RAM organized 1,048,576 words by 4 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM. $\overline{W}$, $\overline{CS}$ Before $\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATIONS

Device Operation

The KM44C1012A contains 4,194,304 memory locations. Twenty address bits are required to address a particular memory location. Since the KM44C1012A has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CS}$) and the valid row and column address inputs.

Operation of the KM44C1012A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CS}$. This is the beginning of any KM44C1012A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths are specified by t_{RAS}(min) and t_{CS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1012A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CS}$ and on the valid column address transition.

If $\overline{CS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, If $\overline{CS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access ttime, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).
The KM44C1012A has common data I/O pins. For this reason and output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44C1012A can perform early write, $\overline{OE}$ controlled write and read-modify-write cycles. Each of these write cycles is achieved by maintaining the write per bit write enable ($\overline{WB}$/$\overline{W}$) input high at the falling edge of $\overline{RAS}$. If write-per bit function is performed, $\overline{WB}$/$\overline{W}$ is kept low at the falling edge of $\overline{RAS}$. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CS}$, whichever is later.

Early Write: An early write cycle is performed by bringing W low before $\overline{CS}$. The 4-bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CS}$ and meeting the data sheet read-modify-write timing requirements. This output enable input ($\overline{OE}$) must be low during the time defined by t_{OEA} and t_{OEZ} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM44C1012A DQ pins.

Write-Per-Bit

Write-per-bit function is performed in the write cycle, that is early write. $\overline{OE}$ controlled write, read-modify-write. Write-per-bit markes it possible selectively to write one or more of the four I/O pins. To perform write per-bit function at the falling edge of $\overline{RAS}$ the write-per-bit/Write enable ($\overline{WB}$/$\overline{W}$) is kept low and at the same time Mask data of input pins to write among 4 I/O pins must be in high. If I/O pins that Mask data is kept low, write operation is inhibited.

Data Output

The KM44C1012A has a three-state output buffers which are controlled by $\overline{CS}$ and $\overline{OE}$. Whenever $\overline{CS}$ or $\overline{OE}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output

DEVICE OPERATIONS (Continued)

the output goes into the low impedance state in the time specified by t_{CLZ} after the falling edge of $\overline{CS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CS}$ returns high. The is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C1012A operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Static Column Read, Static Column Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CS}$-before-$\overline{RAS}$ Refresh, $\overline{CS}$-only cycle, $\overline{OE}$ controlled write.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM44C1012A is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16ms. There are several ways to accomplish this. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CS}$ remains high. This cycle must be repeated for each row.

$\overline{CS}$-before-$\overline{RAS}$ Refresh: The KM44C1012A has $\overline{CS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CS}$ active time and cycling $\overline{RAS}$. The KM44C1012A hidden refresh cycle is actually a $\overline{CS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1012A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CS}$-before-$\overline{RAS}$ refresh is the preferred method.

Static Column Mode

Static Column Mode allows high speed read, write or read-modify-write random access to all the memory cells within a selected row. Operation within a selected row is similar to a static RAM. The read, write or readmodify-write cycles may be mixed in any order.

A Static Column mode read cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{W} = V_{IH}$ and $\overline{RAS} = V_{IL}$.

A Static Column mode write cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{RAS} = V_{IL}$ and toggling either $\overline{W}$ or $\overline{CS}$. The data is written into the cell trigered by the latter fallin edge of $\overline{W}$ or $\overline{CS}$.

$\overline{CS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address — Bits A_0 through A_9 are supplied by the on-chip refresh counter.

Column Address — Bits A_0 through A_9 are strobed-in by the falling edge of CS as in a normal memory cycle.

Suggested $\overline{CS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into the memory cells

DEVICE OPERATION (Continued)

at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).

3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 512 times so that highs are written into the 512 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM44C1012A could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

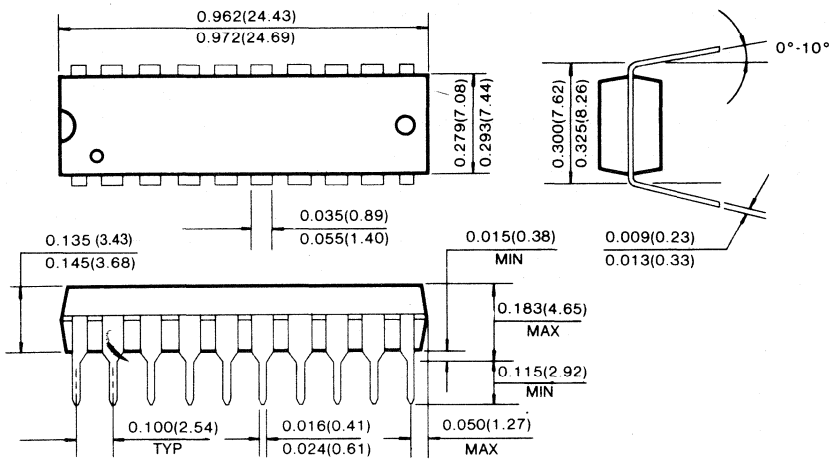
An initial pause of 200 μsec is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

2

PACKAGE DIMENSIONS

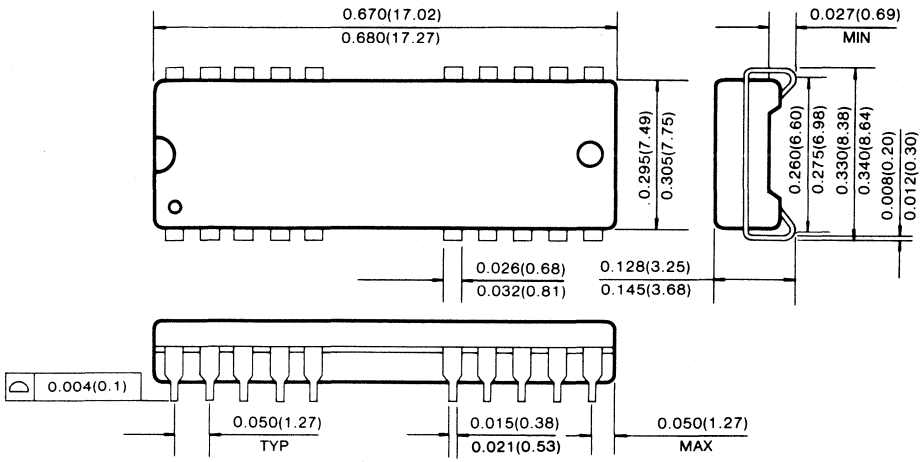
20-LEAD PLASTIC DUAL IN-LINE PACKAGE

Unit: Inches (Millimeters)



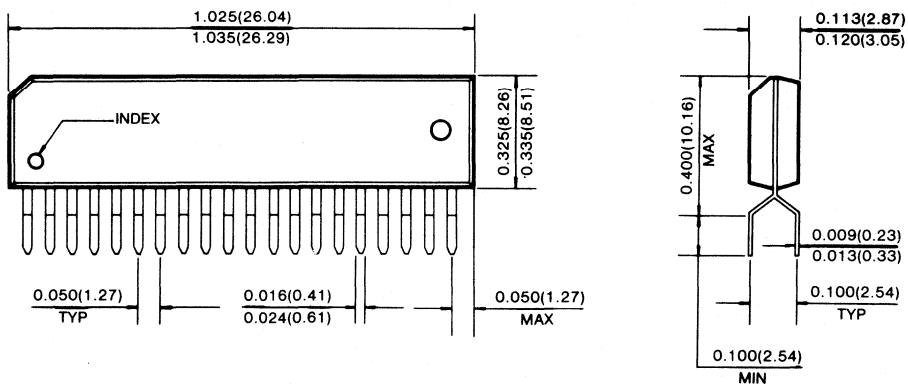
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

Units: Inches (millimeters)



1M x 4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C1000B-6	60ns	15ns	110ns
KM44C1000B-7	70ns	20ns	130ns
KM44C1000B-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single +5V ± 10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in plastic DIP, SOJ, ZIP and TSOP packages**

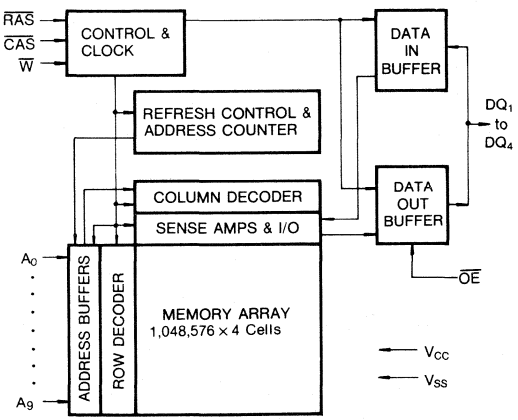
GENERAL DESCRIPTION

The Samsung KM44C1000B is a high speed CMOS 1,048,516 x 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C1000B features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

The KM44C1000B is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

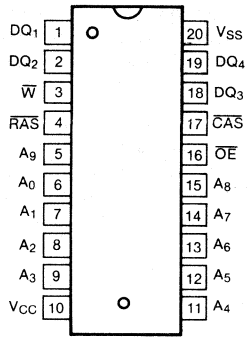


ORDERING INFORMATION

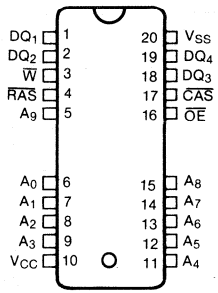
Part No.	Access Time	Package
KM44C1000BP-6	60 ns	300 mil, 20 DIP
KM44C1000BP-7	70 ns	
KM44C1000BP-8	80 ns	
KM44C1000BJ-6	60 ns	300 mil, 20 SOJ
KM44C1000BJ-7	70 ns	
KM44C1000BJ-8	80 ns	
KM44C1000BZ-6	60 ns	400 mil, 20 ZIP
KM44C1000BZ-7	70 ns	
KM44C1000BZ-8	80 ns	
KM44C1000BV-6	60 ns	20 TSOP (I) (Forward)
KM44C1000BV-7	70 ns	
KM44C1000BV-8	80 ns	
KM44C1000BVR-6	60 ns	20 TSOP (I) (Reverse)
KM44C1000BVR-7	70 ns	
KM44C1000BVR-8	80 ns	
KM44C1000BT-6	60 ns	20 TSOP (II) (Forward)
KM44C1000BT-7	70 ns	
KM44C1000BT-8	80 ns	
KM44C1000BTR-6	60 ns	20 TSOP (II) (Reverse)
KM44C1000BTR-7	70 ns	
KM44C1000BTR-8	80 ns	

PIN CONFIGURATION (Top Views)

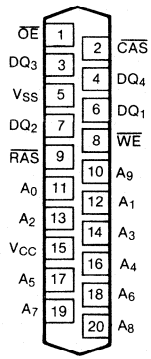
• KM44C1000BP



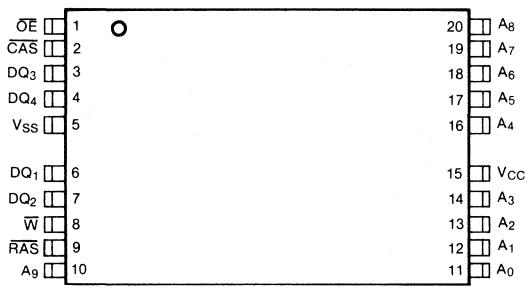
• KM44C1000BJ



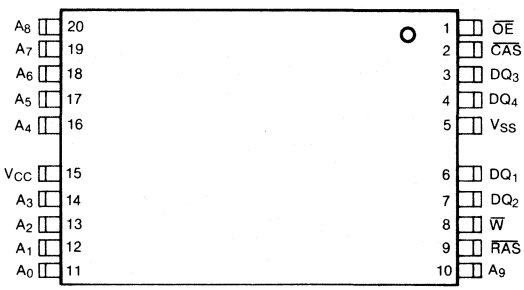
• KM44C1000BZ



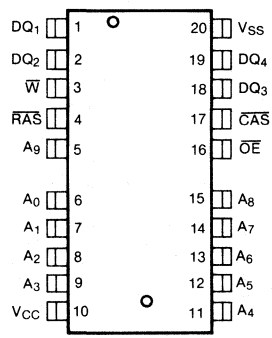
• KM44C1000BV



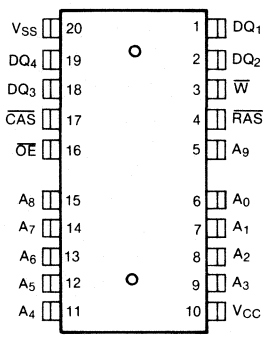
• KM44C1000BVR



• KM44C1000BT



• KM44C1000BTR



Pin Names	Pin Function
A_0-A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
DQ_1/DQ_4	Data In/Data Out
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM44C1000B-6	I_{CC1}	—	90	mA
	KM44C1000B-7		—	80	mA
	KM44C1000B-8		—	70	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @ t_{RC}=min.)	KM44C1000B-6	I_{CC3}	—	90	mA
	KM44C1000B-7		—	80	mA
	KM44C1000B-8		—	70	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @ t_{PC}=min.)	KM44C1000B-6	I_{CC4}	—	70	mA
	KM44C1000B-7		—	60	mA
	KM44C1000B-8		—	50	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM44C1000B-6	I_{CC6}	—	90	mA
	KM44C1000B-7		—	80	mA
	KM44C1000B-8		—	70	mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL}, D_{OUT} Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} address transition should be changed maximum two while $\overline{RAS}$=V_{IL}. In I_{CC4}, address transition should be changed only once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	KM44C1000B-6		KM44C1000B-7		KM44C1000B-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

Parameter	Symbol	KM44C1000B-6		KM44C1000B-7		KM44C1000B-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (1,024 cycles)	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	80		95		100		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	15		20		20		ns	
Write command set-up time (test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ cycle)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ cycle)	t_{WRH}	10		10		10		ns	

TEST MODE CYCLE

(Note. 12)

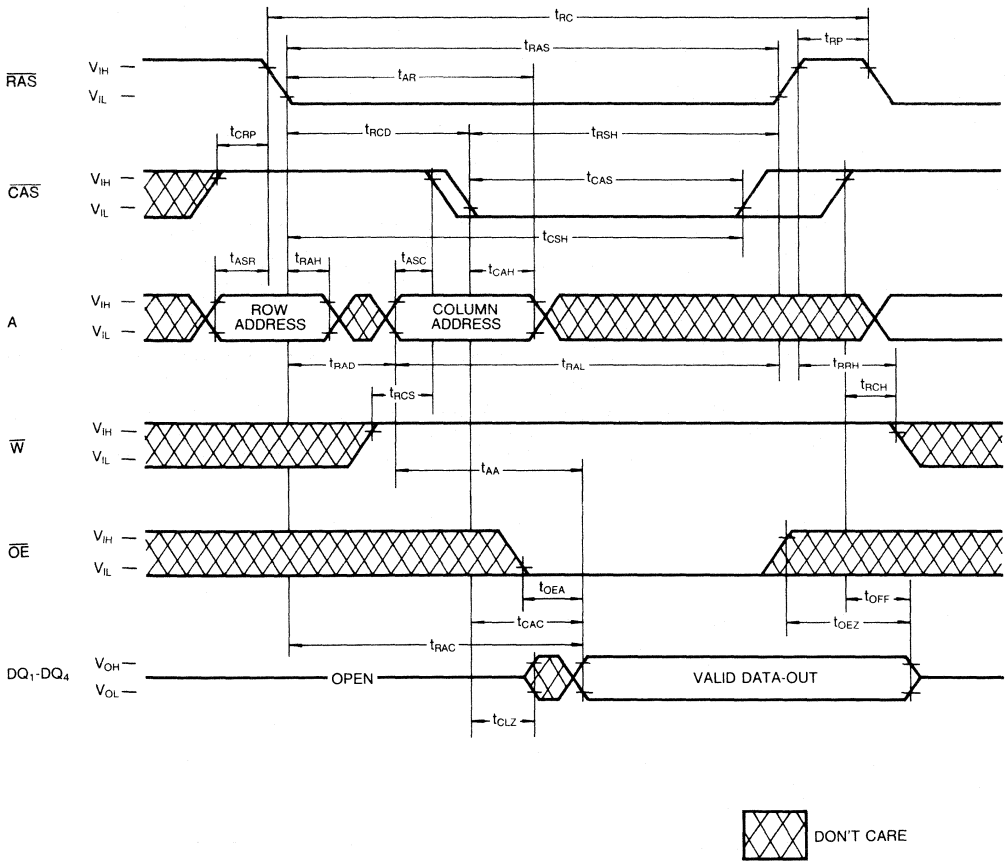
Parameter	Symbol	KM44C1000B-6		KM44C1000B-7		KM44C1000B-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	160		190		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		45		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	45		55		55		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	90		105		115		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	60		70		75		ns	8
Fast mode cycle time	t_{PC}	45		50		55		ns	
Fast page mode read-modefy-write	t_{PRWC}	85		100		105		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3
$\overline{OE}$ access time	t_{OEA}		20		25		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		25		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only Refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF(max)}$ and $t_{OEZ(max)}$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

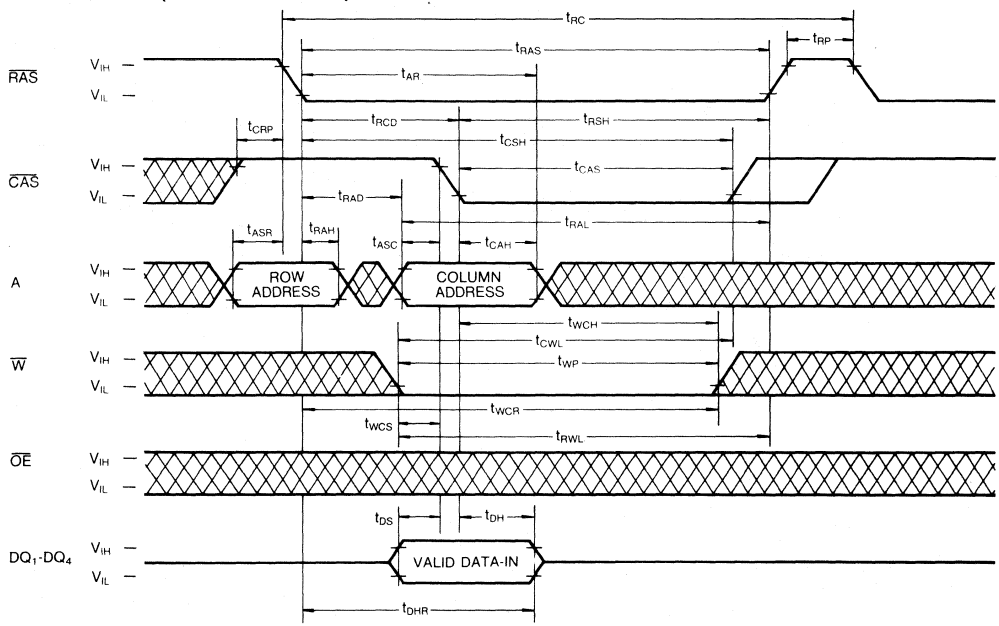
TIMING DIAGRAMS

READ CYCLE

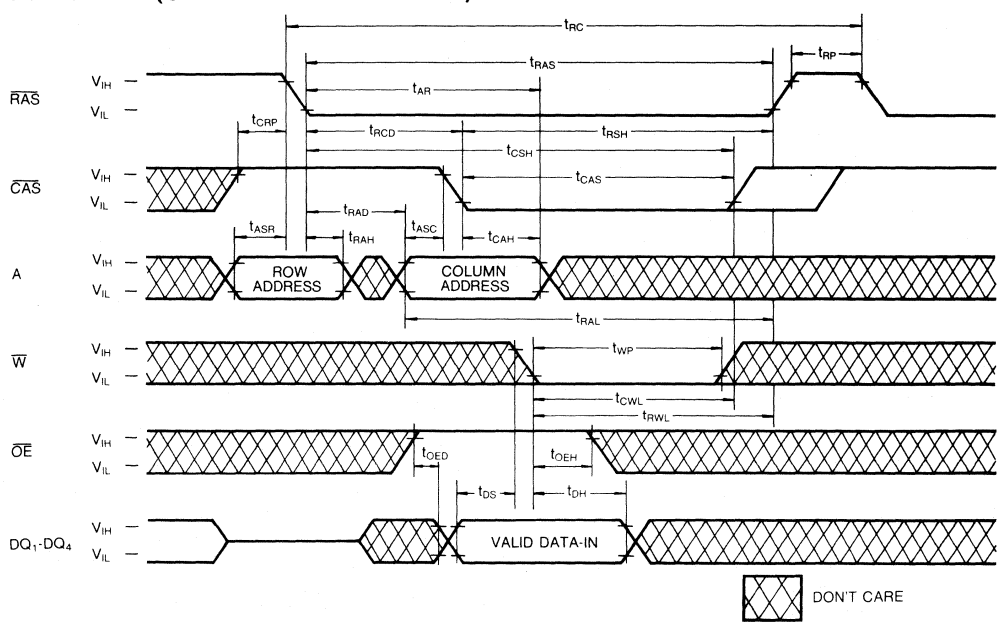


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)

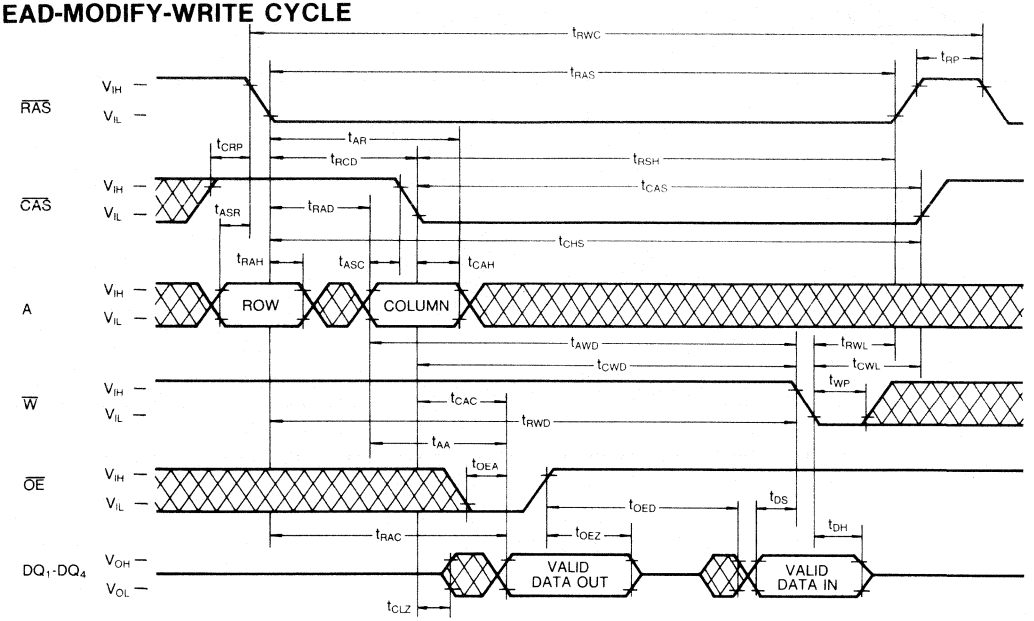


WRITE CYCLE (OE CONTROLLED WRITE)

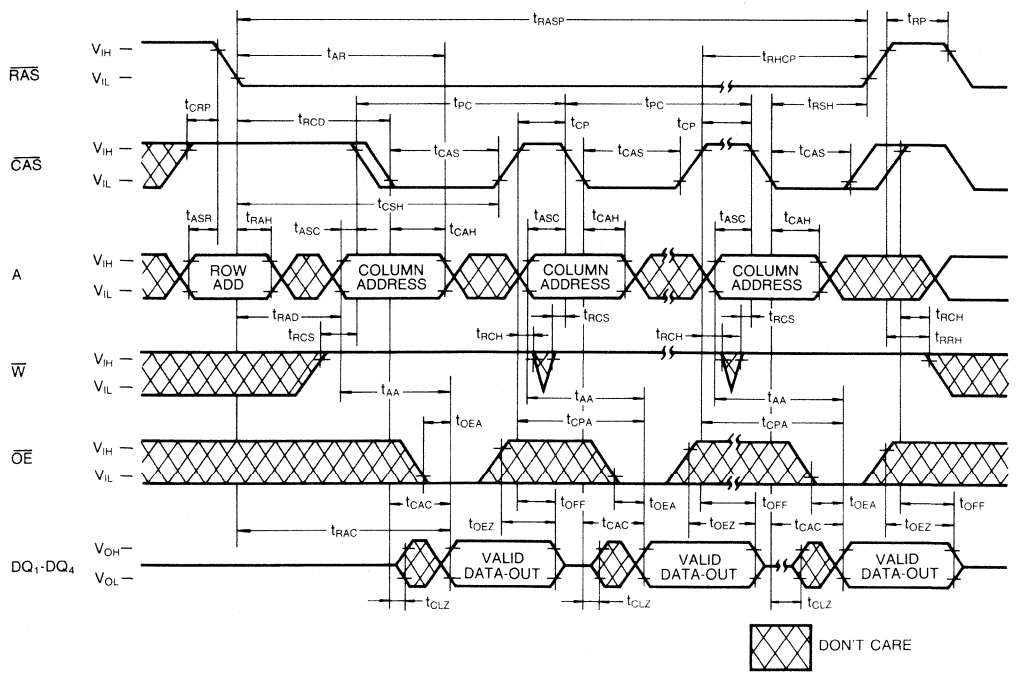


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE

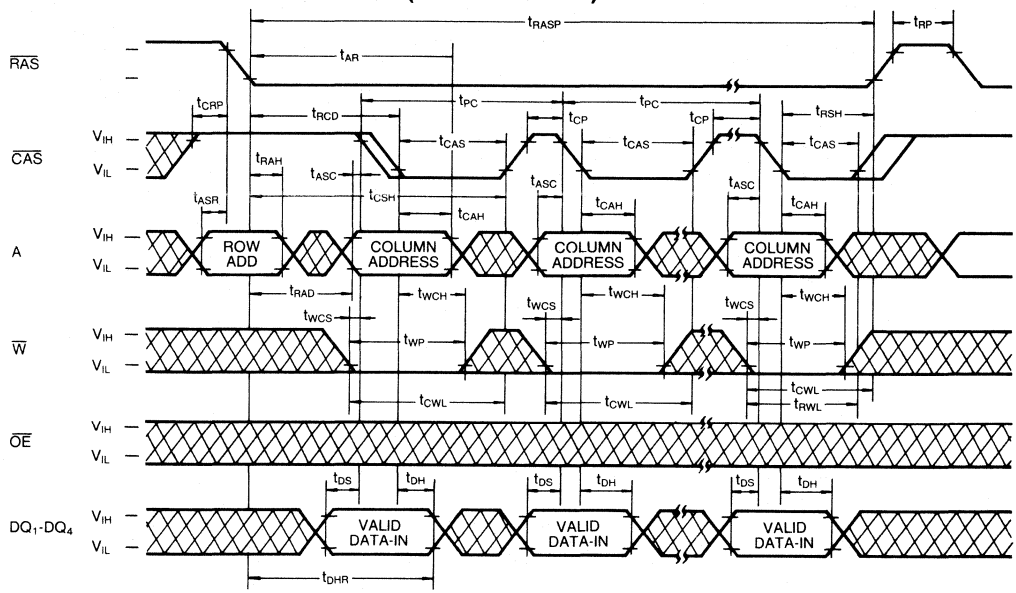


FAST PAGE MODE READ CYCLE

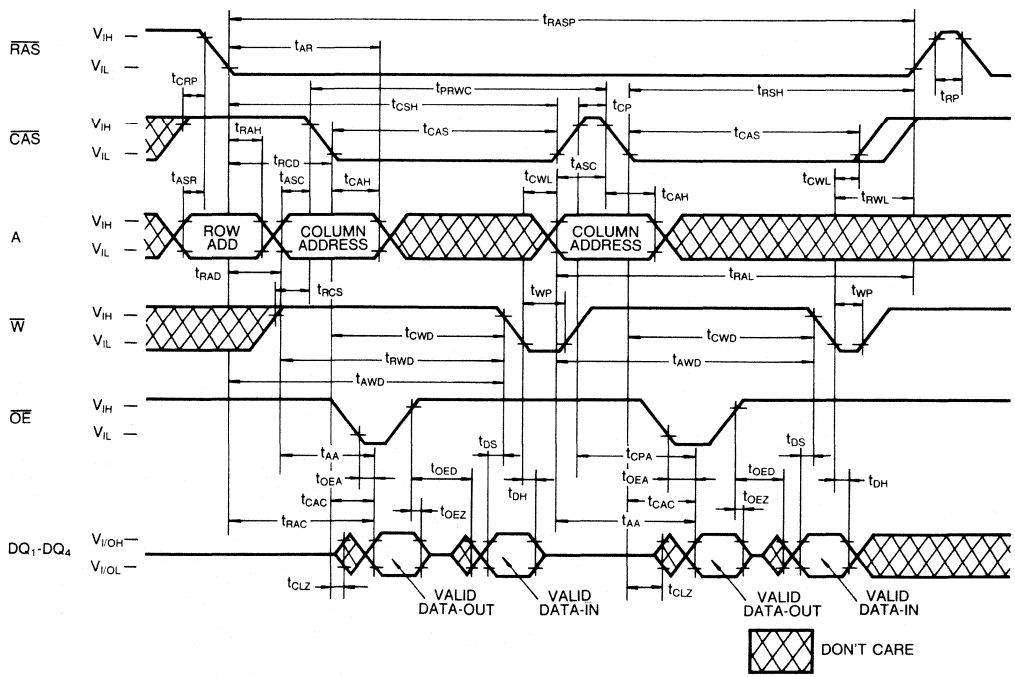


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



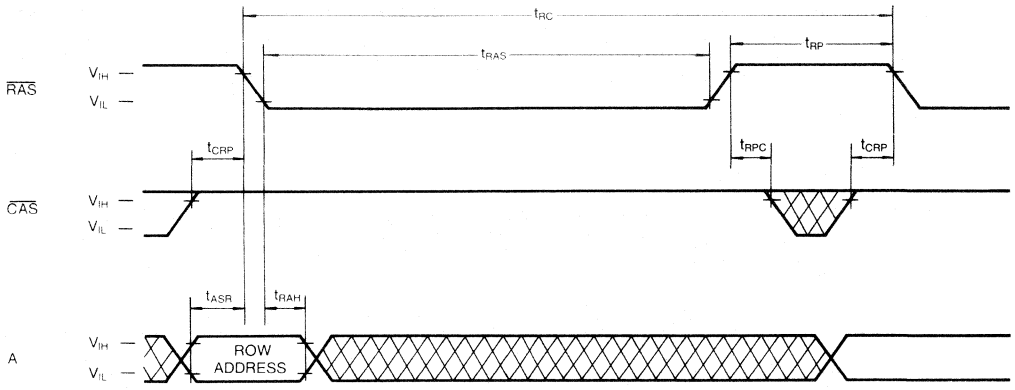
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

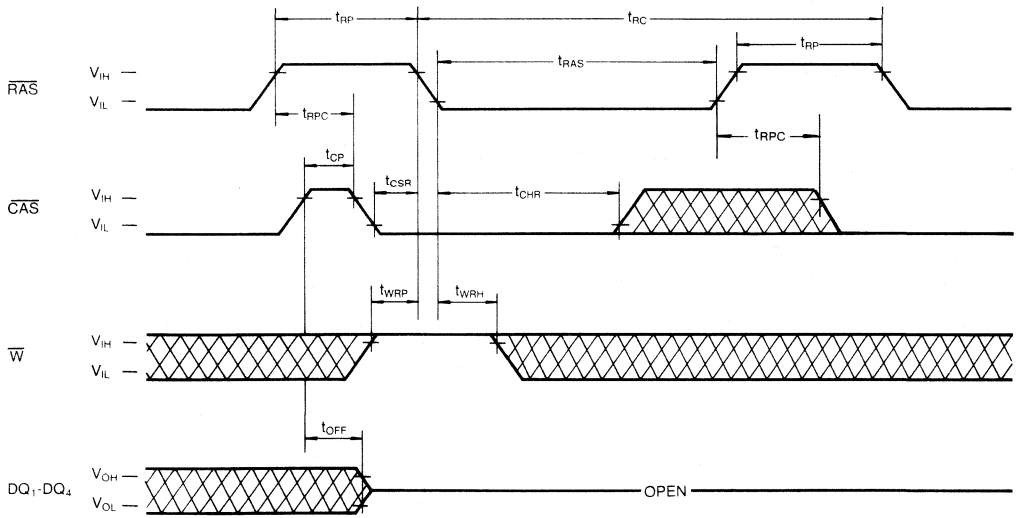
$\overline{RAS}$ ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



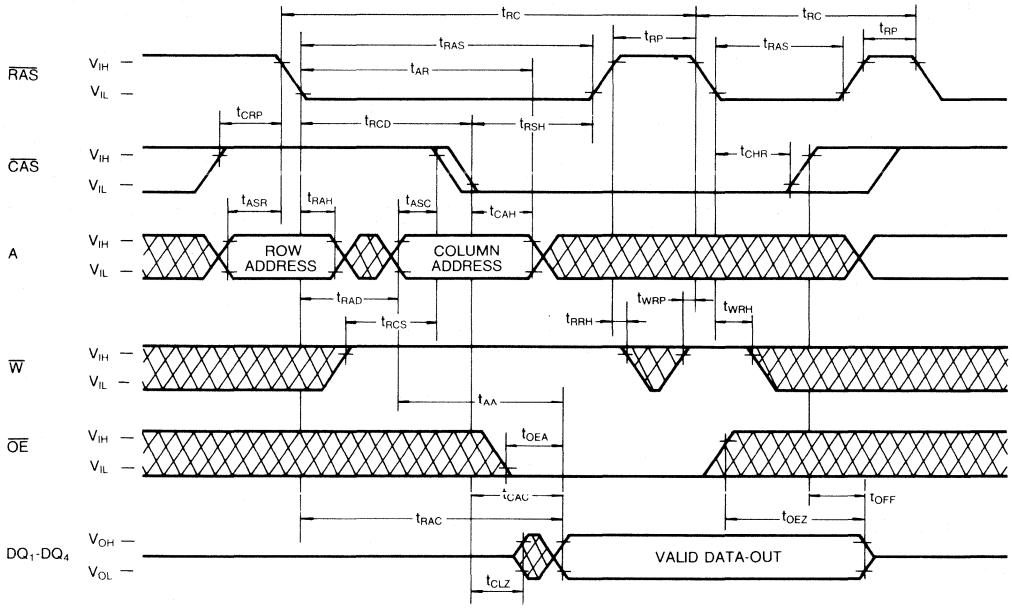
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: $\overline{OE}$, Address=Don't Care

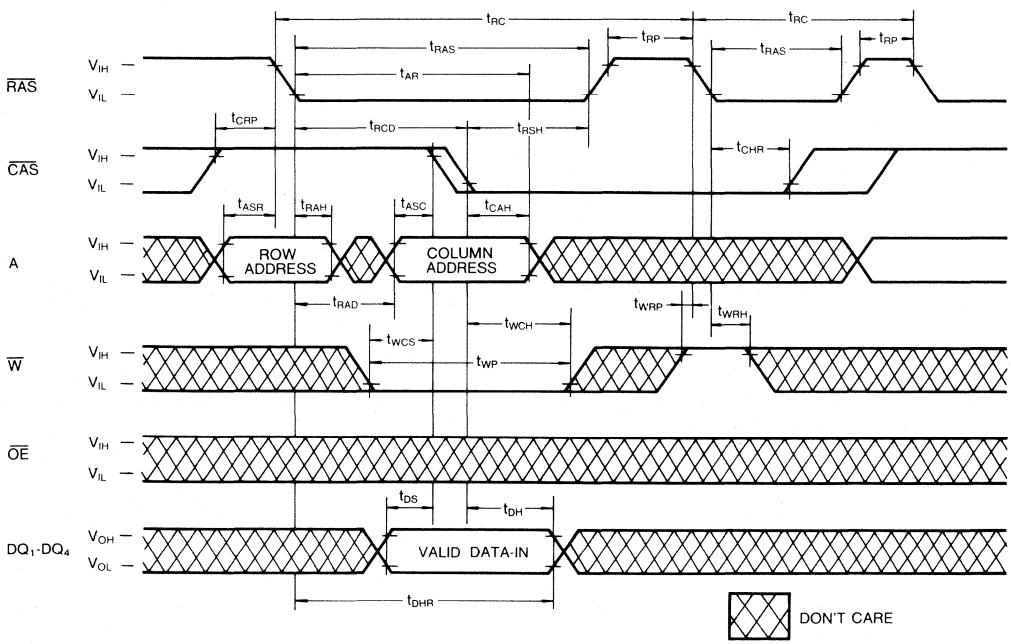


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

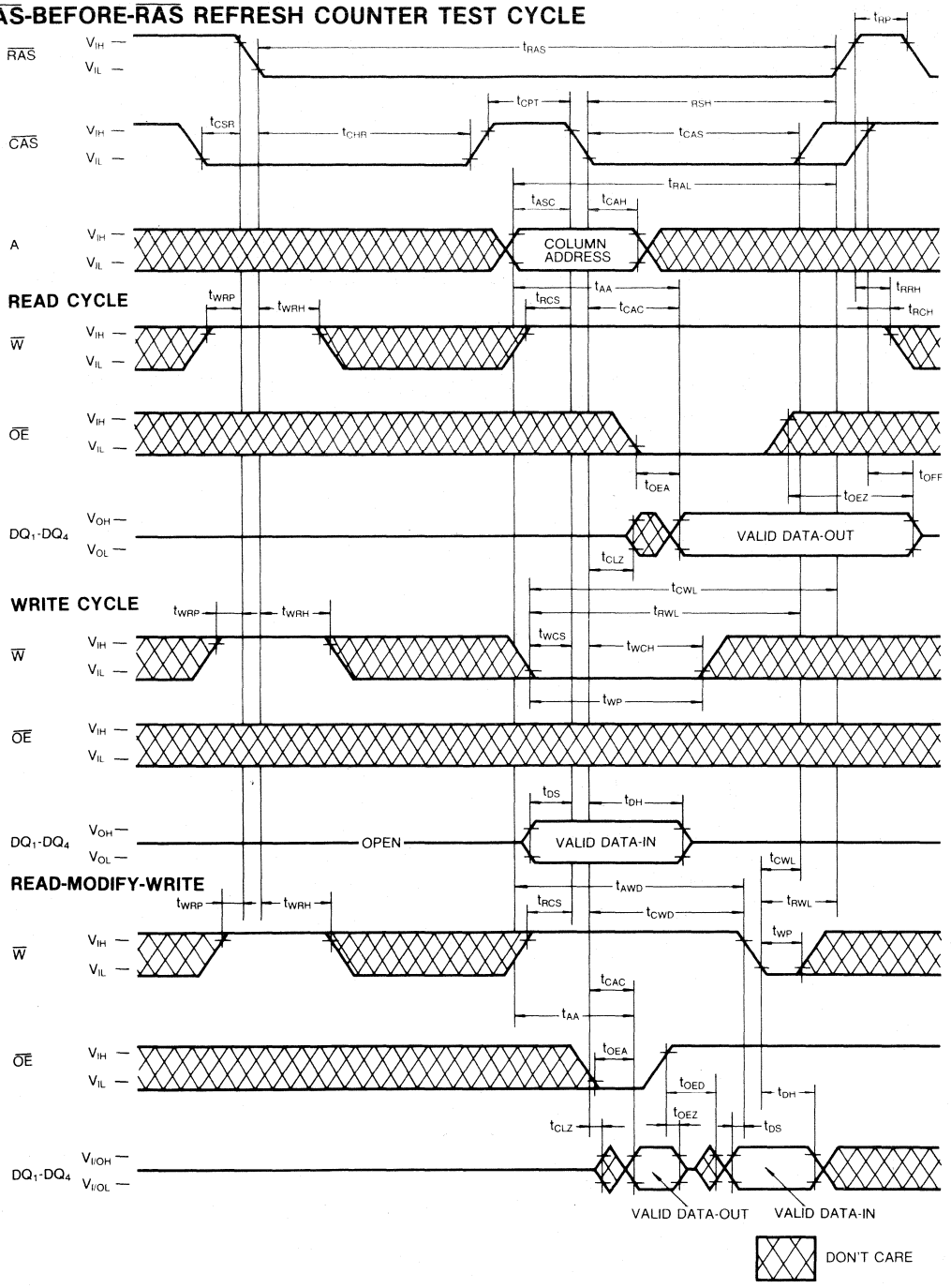


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

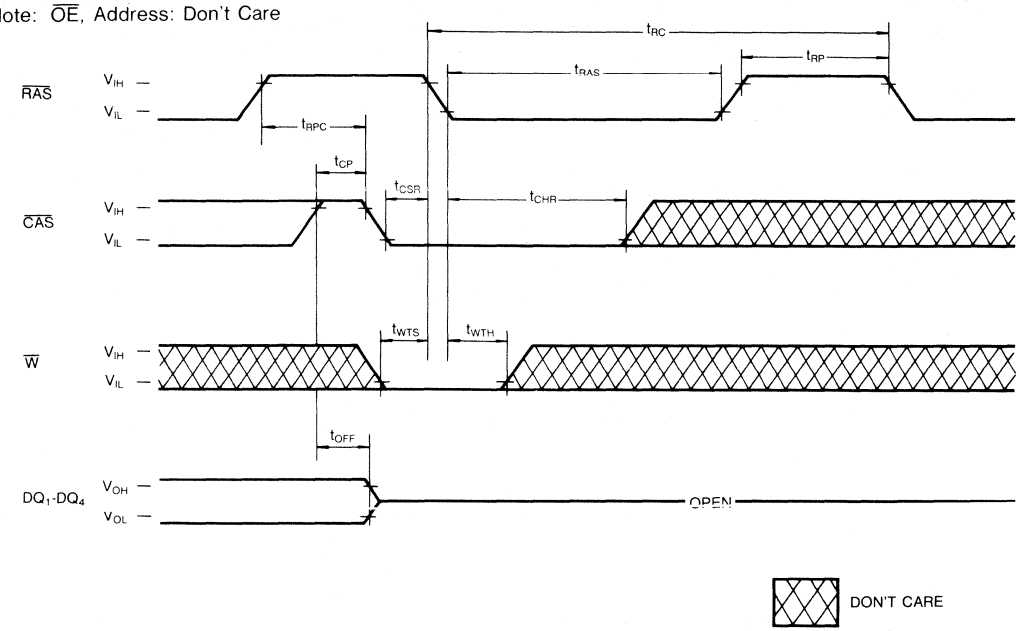
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



TEST MODE DESCRIPTION

The KM44C1000B is the RAM organized 1,048,576 words by 4 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode," data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. if, upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1." If they were not equal, the I/O pin would indicate a "0." In "Test Mode," the 1M x 4 DRAM can be tested as if it were a 512K x 4 DRAM. W, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode." And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE" or "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode." The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATION

The KM44C1000B contains 4,194,304 memory locations. Twenty address bit are required to address a particular 4-bit word in the memory array. Since the KM44C1000B has only 10 address input pins, time multiplexed addressing is used to input 10 row (A_0-A_9) and 10 column (A_0-A_9) addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM44C1000B begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins (A_0-A_9) is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C1000B cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1000B begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAC}(max), then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max). The KM44C1000B has common data I/O pins. The this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44C1000B can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the three state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44C1000B has a three-state output buffer which is controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever $\overline{CAS}$ and $\overline{OE}$ are high (V_{IH}), the outputs are in the high impedance state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C1000B operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} are not met)

Refresh

The data in the KM44C1000B is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C1000B has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C1000B hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1000B by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address—Bits A_0 through A_9 are supplied by the on-chip refresh counter.

Column Address — Bits A_0 through A_9 are supplied by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM44C1000B could possibly begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

DEVICE OPERATION (Continued)

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 16 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C1000B inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C1000B input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

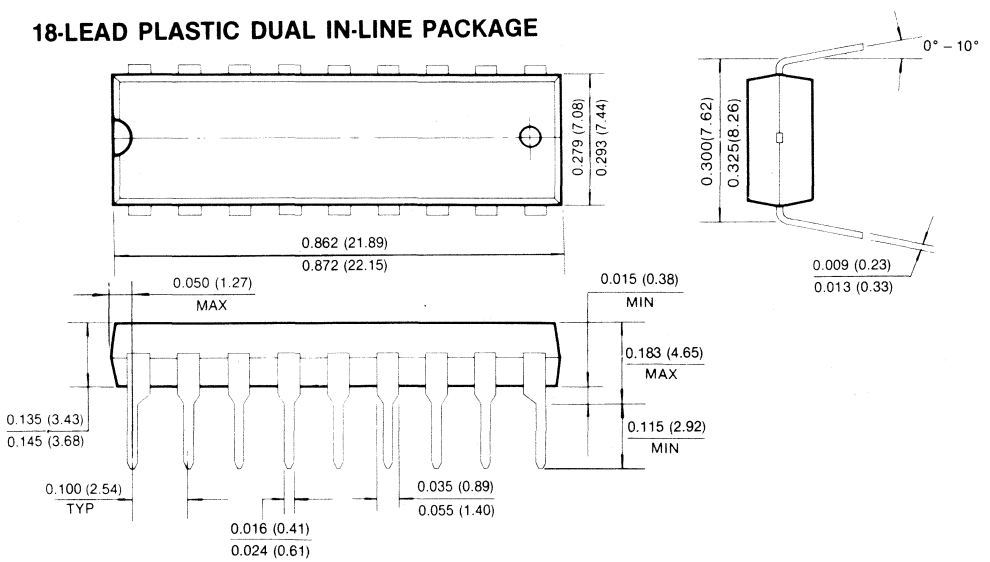
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM44C1000B using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C1000B and they supply much of the current used by the KM44C1000B during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

Units: Inches (Millimeters)

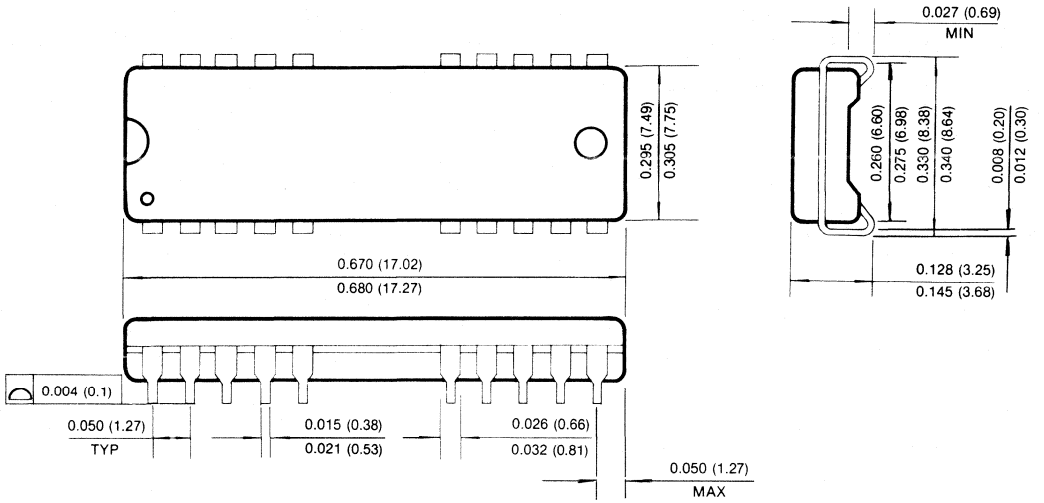
18-LEAD PLASTIC DUAL IN-LINE PACKAGE



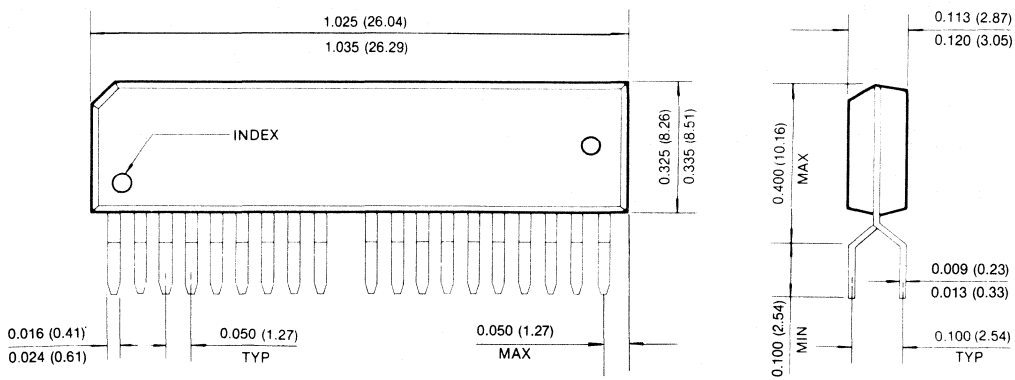
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



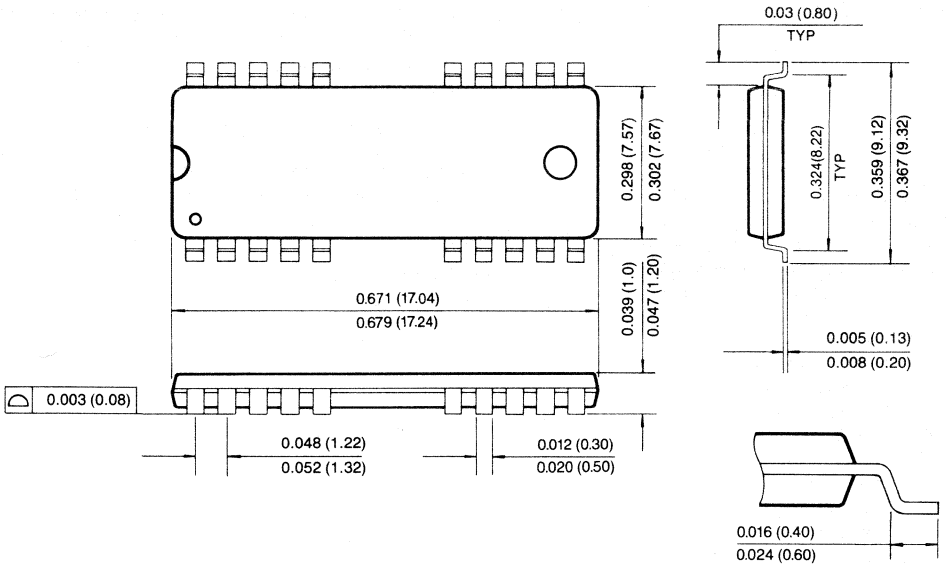
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



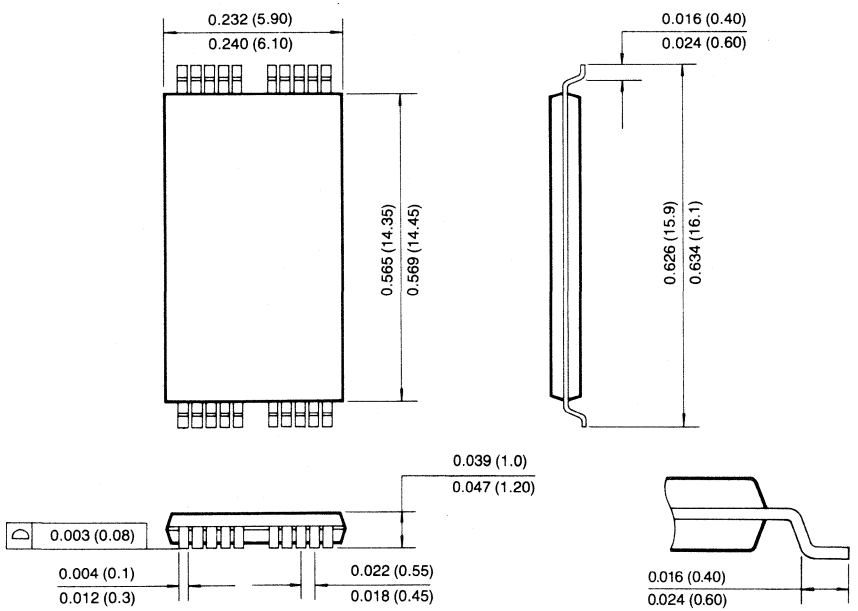
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (I) (Forward and Reverse Type)



512K x 8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM48C512/L/SL-7	70ns	20ns	130ns
KM48C512/L/SL-8	80ns	20ns	150ns
KM48C512/L/SL-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Dual +5V±10% power supply**
- **Refresh Cycle**
  - **— 1024 cycle/16ms (Normal)**
  - **— 1024 cycle/128ms (L-version)**
  - **— 1024 cycle/256ms (SL-version)**
- **Power Dissipation**
  - **— Standby: 11mW (Normal)**
    1.1mW (L-version)
    0.55mW (SL-version)
  - **— Active (70/80/100): 578/495/413mW**
- **JEDEC Standard pinout**
- **Available in Plastic SOJ, ZIP and TSOP II**

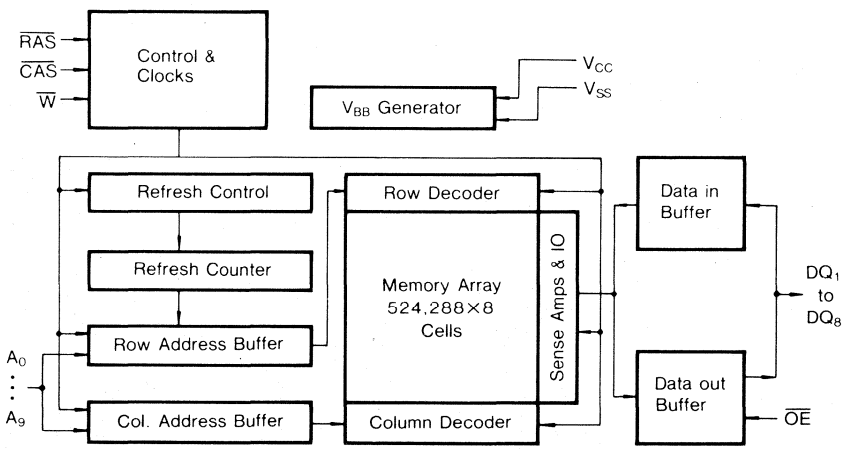
GENERAL DESCRIPTION

The Samsung KM48C512/L/SL is a CMOS high speed 524,288 bit x 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM48C512/L/SL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

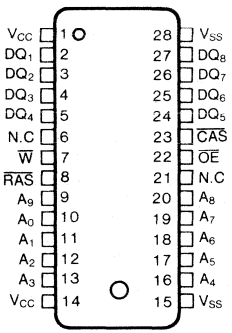
The KM48C512/L/SL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



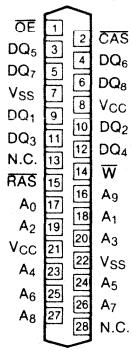
PIN CONFIGURATION (Top Views)

• KM48C512J/LJ/SLJ



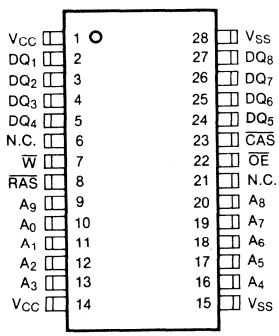
(SOJ)

• KM48C512Z/LZ/SLZ



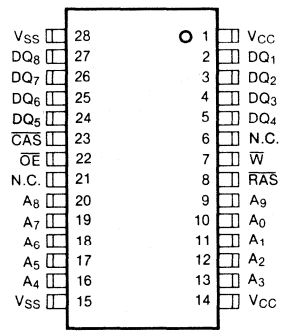
(ZIP)

• KM48C512T/LT/SLT



(TSOP(II)-Forward Type)

• KM48C512TR/LTR/SLTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A_0-A_9	Address Input
DQ_{1-8}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe

Pin Name	Pin Function
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power(+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC} = min.)	KM48C512/L/SL-7	I_{CC1}	—	105	mA
	KM48C512/L/SL-8		—	90	mA
	KM48C512/L/SL-10		—	75	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM48C512/L/SL-7	I_{CC3}	—	105	mA
	KM48C512/L/SL-8		—	90	mA
	KM48C512/L/SL-10		—	75	mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC} = min.)	KM48C512/L/SL-7	I_{CC4}	—	85	mA
	KM48C512/L/SL-8		—	75	mA
	KM48C512/L/SL-10		—	65	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)	KM48C512	I_{CC5}	—	1	mA
	KM48C512L		—	200	μA
	KM48C512SL		—	100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min.)	KM48C512/L/SL-7	I_{CC6}	—	105	mA
	KM48C512/L/SL-8		—	90	mA
	KM48C512/L/SL-10		—	75	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode Input High Voltage (V_{IH}) = V_{CC}-0.2V Input Low Voltage (V_{IL}) = 0.2V $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V D_{IN} = Don't Care T_{RC}=125 μS(L-ver), T_{RC}=250 μS(SL-ver), T_{RAS}=T_{RAS}min.~1μS.	KM48C512L	I_{CC7}	—	300	μA
	KM48C512SL		—	150	μA

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any Input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test=0V)	I_{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	I_{OL}	-10	10	μA
Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	—	V
Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS} = V_{IL}$. In I_{CC4}, Address can be changed maximum once while $\overline{CAS} = V_{IH}$.

2

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_8)	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC} = 5.0V ± 10%, See notes 1, 2)

Parameter	Symbol	KM48C512/L/SL-7		KM48C512/L/SL-8		KM48C512/L/SL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	180		200		240		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to CAS delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	55	ns	11
$\overline{CAS}$ to RAS precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	

AC CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC}=5.0V \pm 10\%$, See notes 1,2)

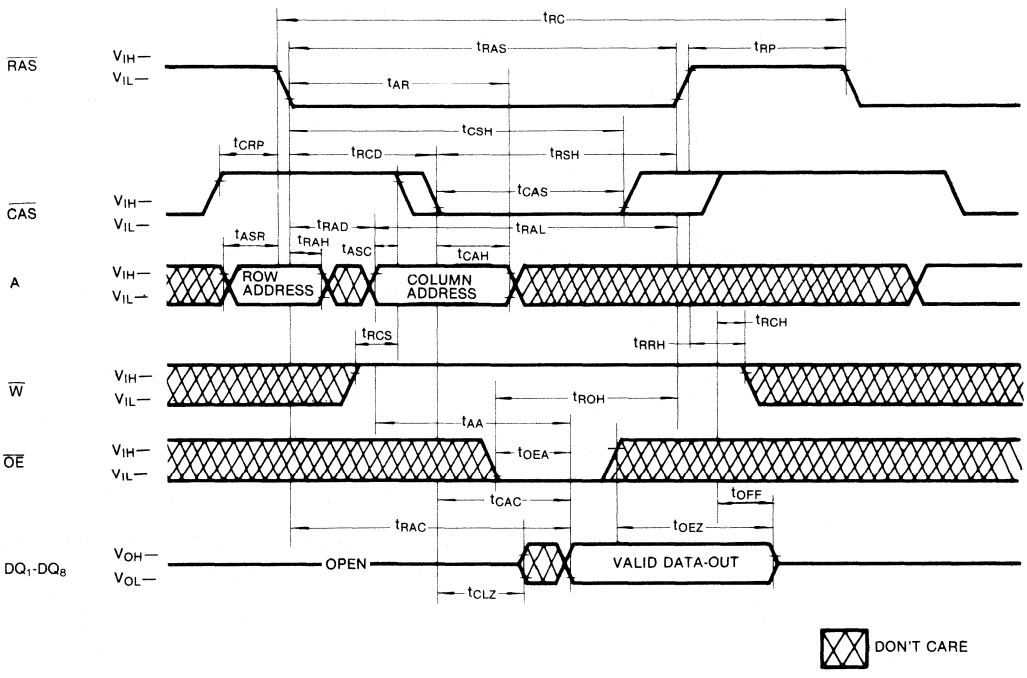
Parameter	Symbol	KM48C512/L/SL-7		KM48C512/L/SL-8		KM48C512/L/SL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command set-up time	t_{WCS}	0		0		0		ns	8
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Refresh period (L-version)	t_{REF}		128		128		128	ms	
Refresh period (SL-version)	t_{REF}		256		256		256	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	45		45		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	95		105		130		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	60		65		75		ns	8
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3
Fast page mode cycle time	t_{PC}	45		50		55		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	95		100		115		ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
Access time from $\overline{OE}$	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data-in delay time	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} to V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or r_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point ony. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

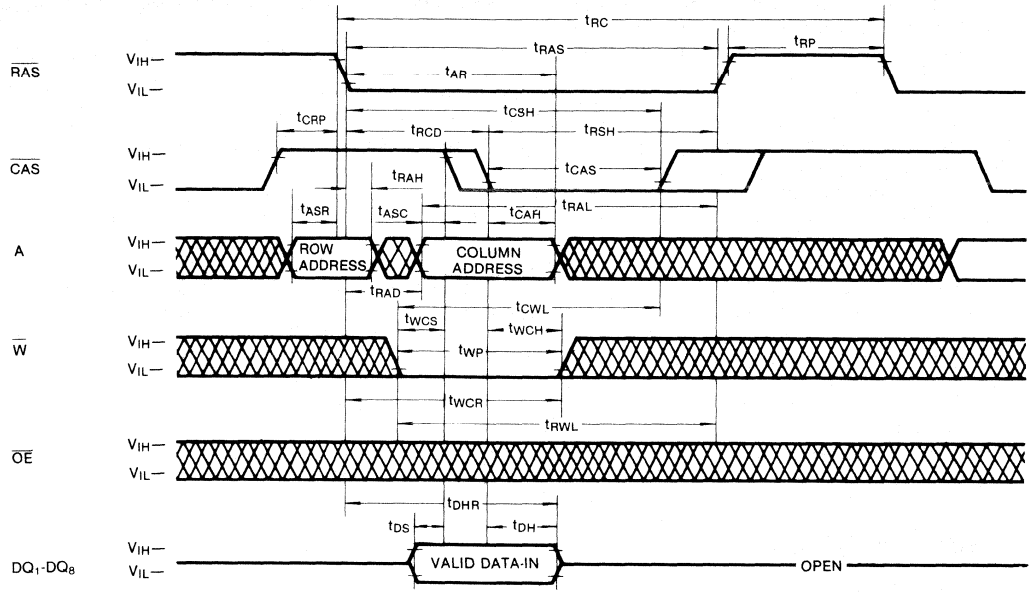
TIMING DIAGRAMS

READ CYCLE

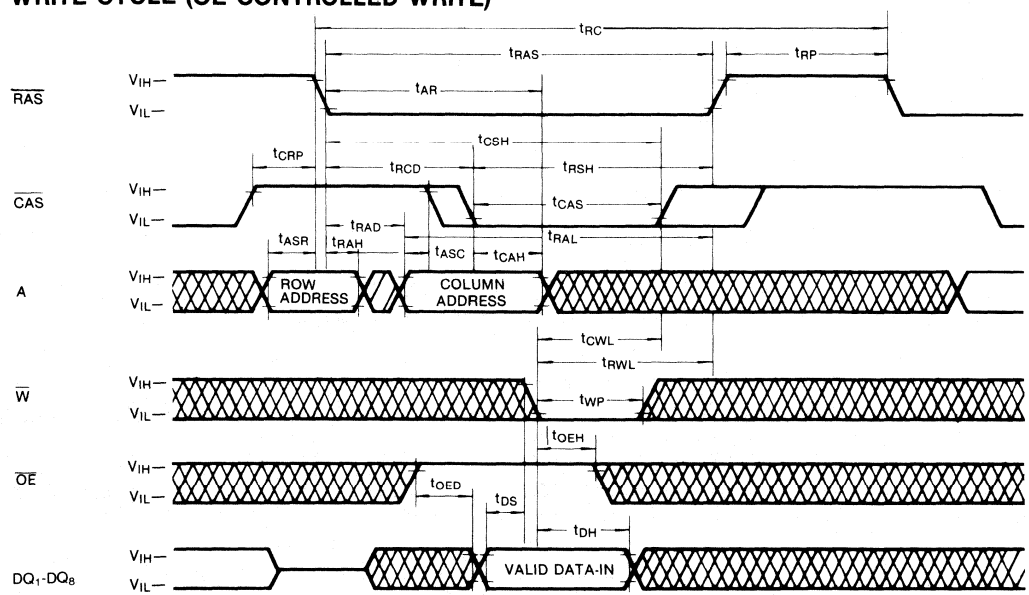


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



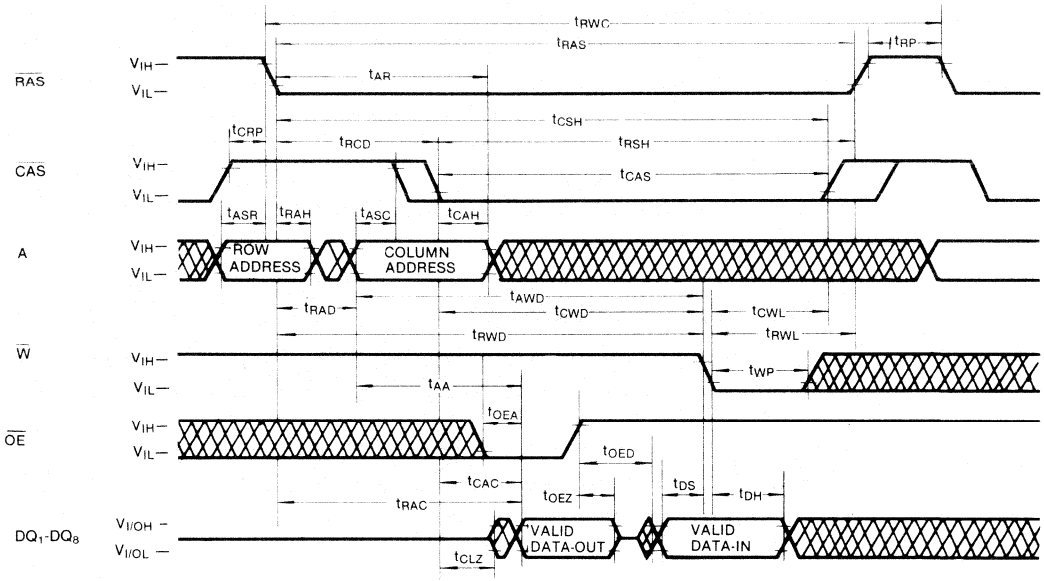
WRITE CYCLE (OE CONTROLLED WRITE)



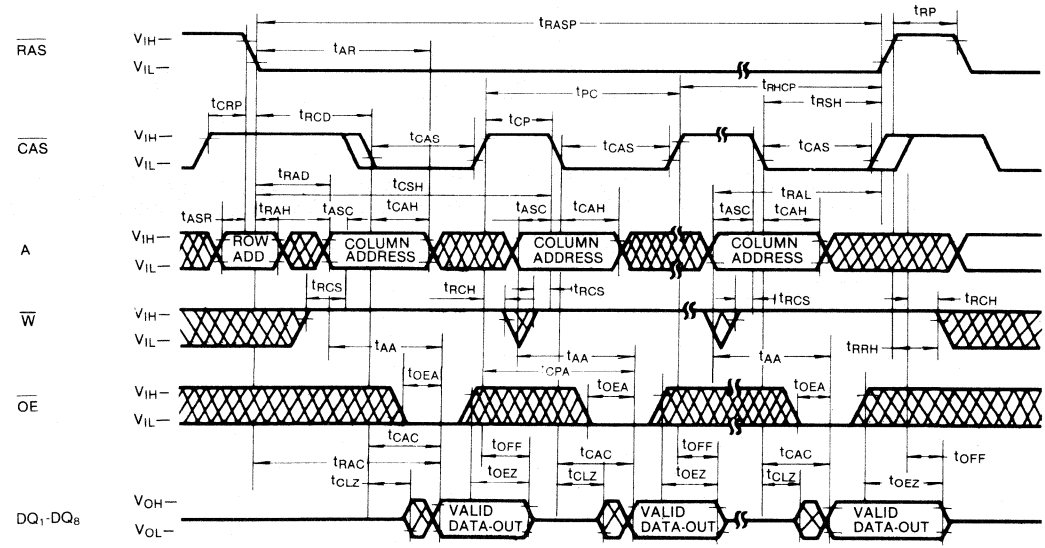
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



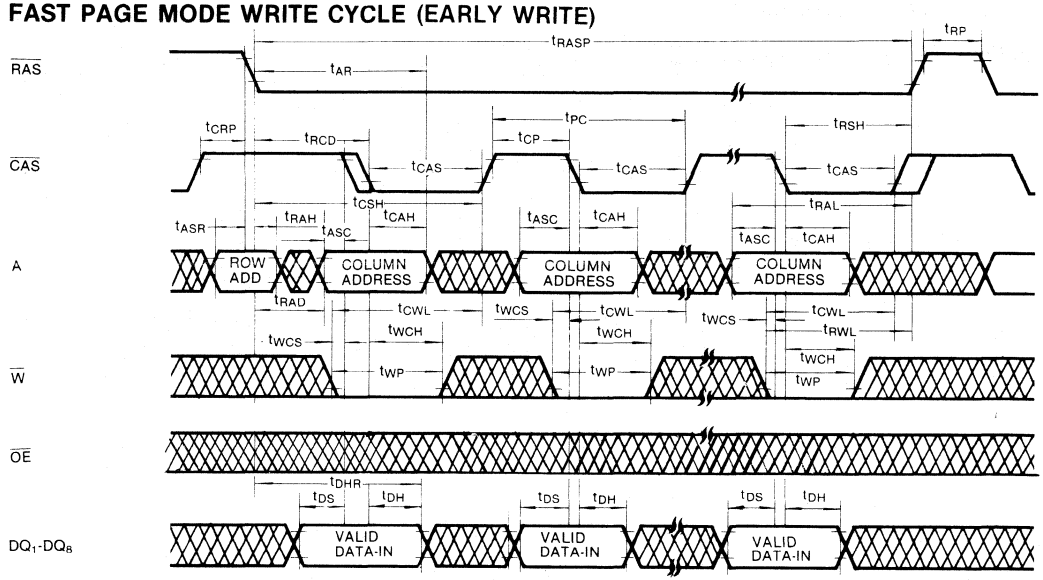
FAST PAGE MODE READ CYCLE



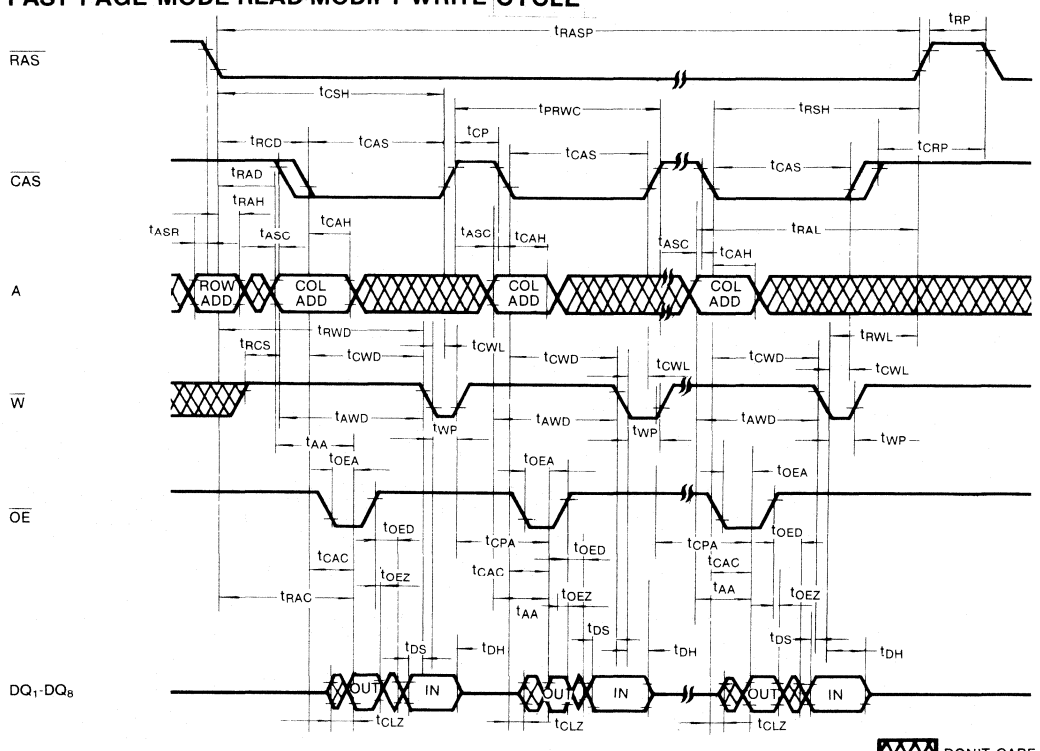
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



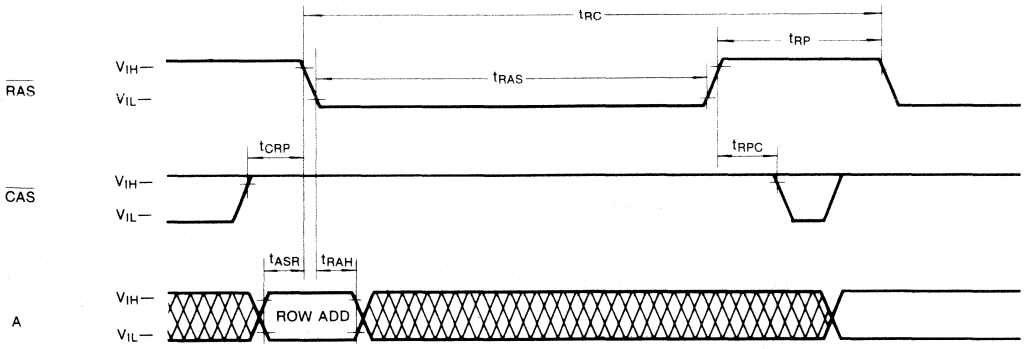
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

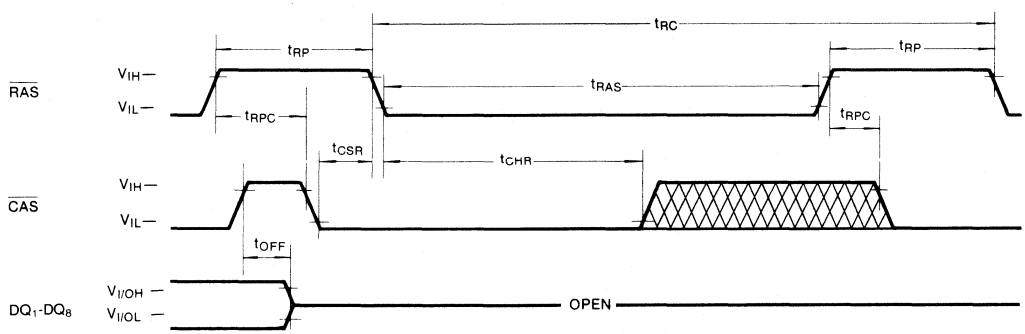
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

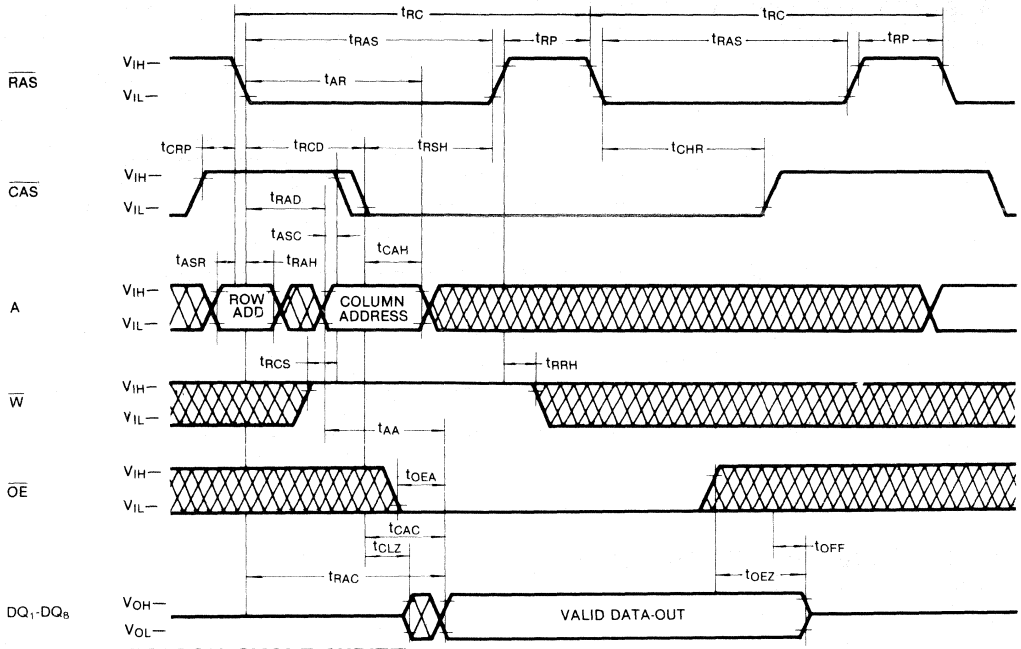
NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care



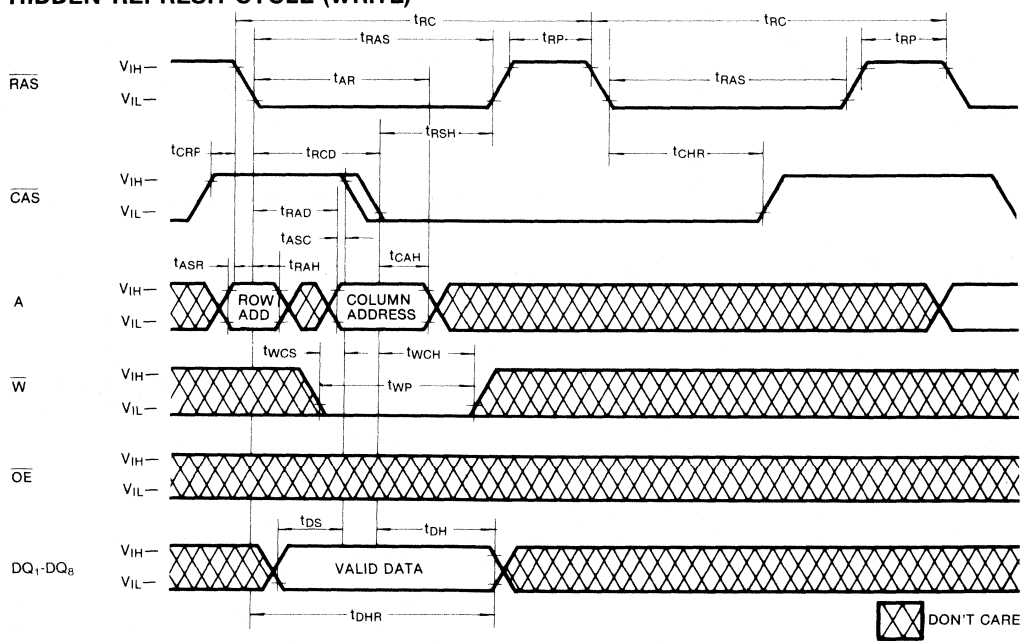
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

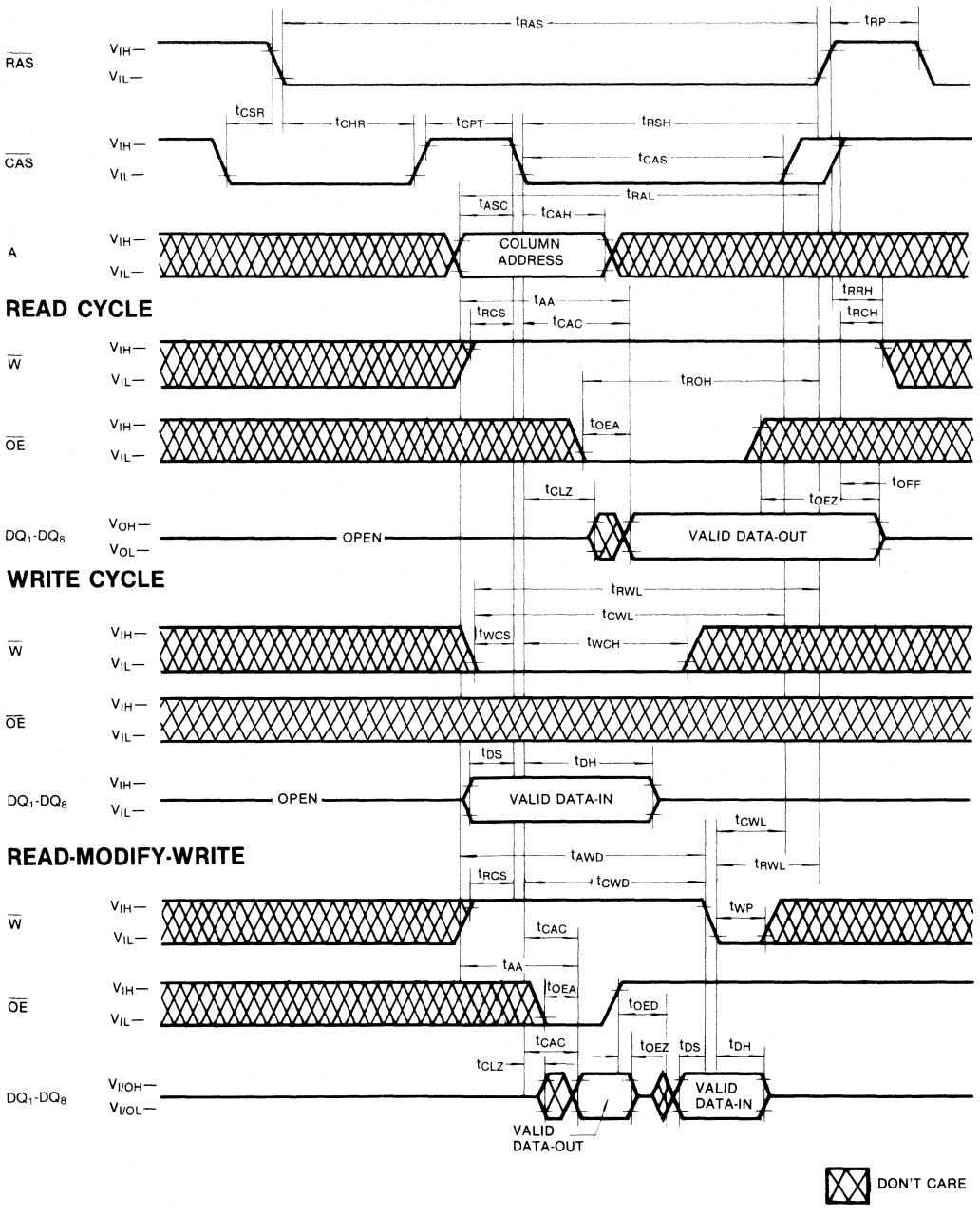


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM48C512/L/SL contains 4,194,304 memory locations arranged in 8 groups of 524,288 × 1 bit each. Ninteen address bits are required to address a particular memory location. Since the KM48C512/L/SL has only 10 address input pins, time multiplexed addressing is used to input 10 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM48C512/L/SL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM48C512/L/SL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM48C512/L/SL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM48C512/L/SL can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$, $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 8-bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cells. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The $\overline{OE}$ input must be low during the time defined by t_{OEA} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM48C512/L/SL DQ pins.

Data Output

The KM48C512/L/SL has a three-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}), the outputs are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs enter into the low impedance state in the time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM48C512/L/SL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} times are not met)

DEVICE OPERATION (Continued)

Refresh

The data in the KM48C512/L/SL is stored as a charge on microscopic capacitor within each memory cell. The stored charge tends to dissipate over time and will affect data integrity if the charge is not periodically refreshed. Refresh of the individual storage cells is accomplished by accessing all rows within the refresh period (t_{REF}) off within 16ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 1024 row address (A0-A9).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM48C512/L/SL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ transitions low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending either input active time and cycling $\overline{RAS}$. The hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM48C512/L/SL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM48C512/L/SL has Fast page mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is asserted high and then low again while $\overline{RAS}$ is asserted low, the read and write operations are enabled. In this method, the row address bits A0 through A9 are supplied by on chip refresh counter.

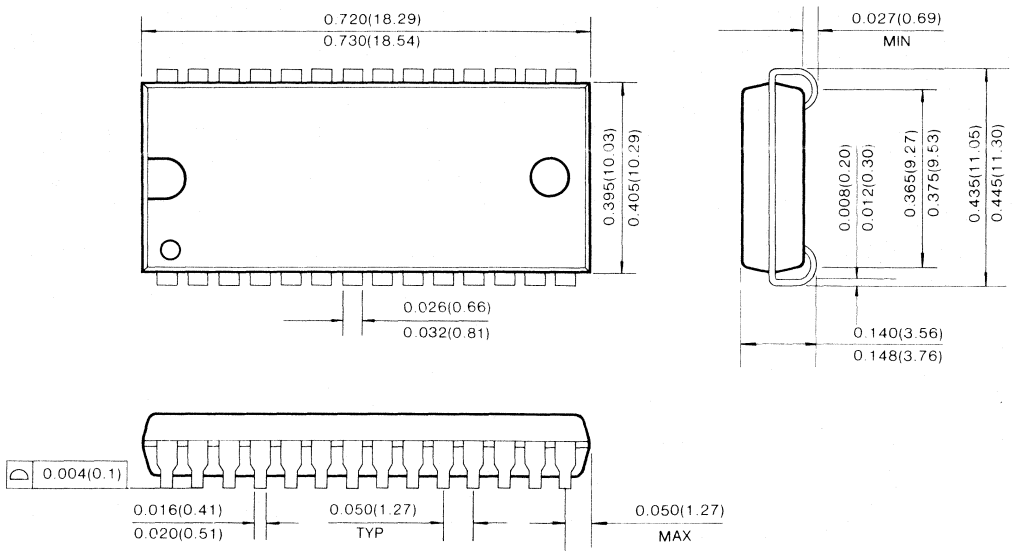
Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM48C512/L/SL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held a valid V_{IH} in order to minimize the power-up current.

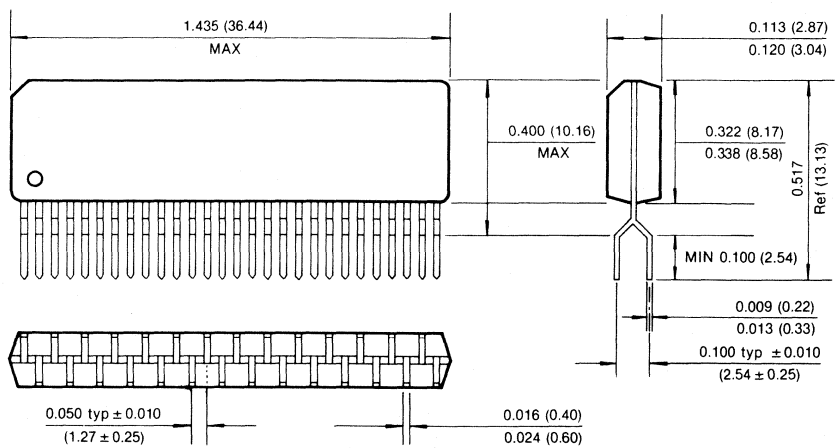
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)

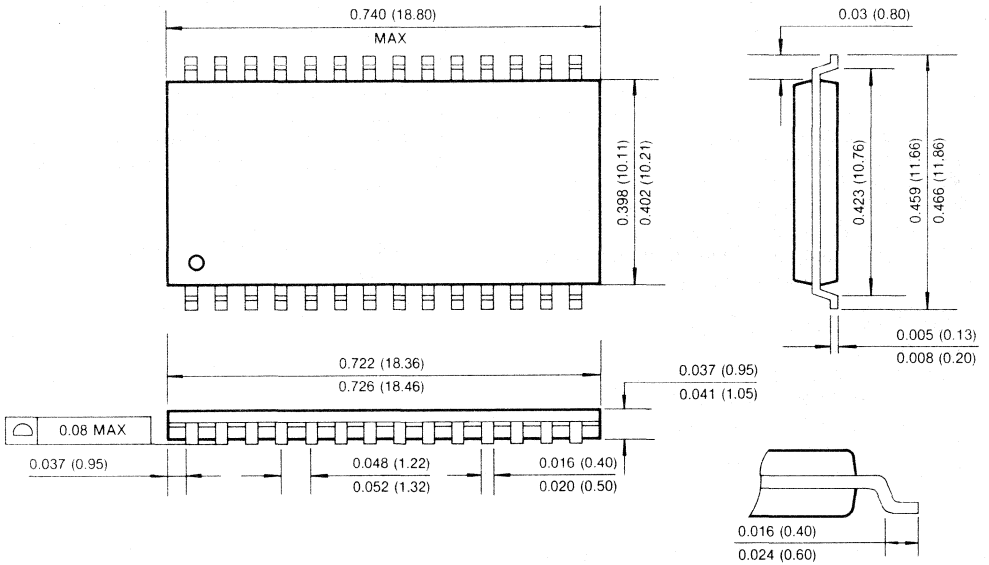


28-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

Units: Inches (millimeters)



512K x 8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM48C512LL-7	70ns	20ns	130ns
KM48C512LL-8	80ns	20ns	150ns
KM48C512LL-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Dual +5V±10% power supply**
- **Refresh Cycle**
  - **— 1024 cycle/128ms (self-refresh)**
- **Power Dissipation**
  - **— Standby: 11mW (Normal)**
    0.55mW (self-refresh)
  - **— Active (70/80/100): 578/495/413mW**
- **JEDEC Standard pinout**
- **Available in Plastic SOJ, ZIP and TSOP II**

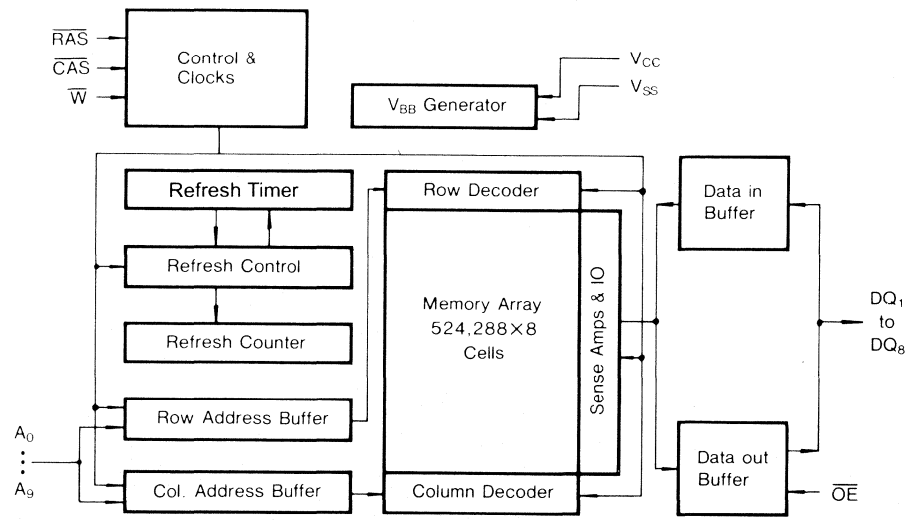
GENERAL DESCRIPTION

The Samsung KM48C512LL is a CMOS high speed 524,288 bit x 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM48C512LL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

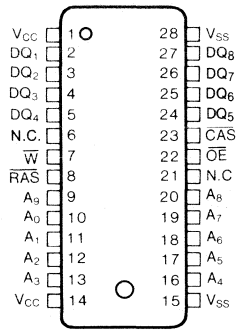
The KM48C512LL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



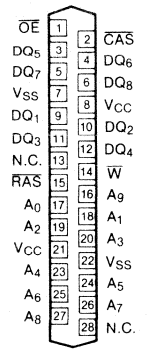
PIN CONFIGURATION (Top Views)

• KM48C512LLJ



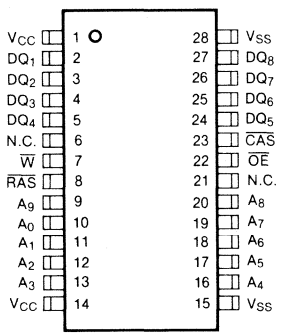
(SOJ)

• KM48C512LLZ



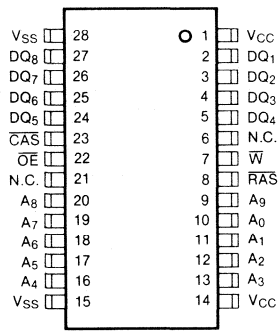
(ZIP)

• KM48C512LLT



(TSOP(II)-Forward Type)

• KM48C512LLTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A_0-A_9	Address Input
DQ_{1-8}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe

Pin Name	Pin Function
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power(+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC} = min.)	KM48C512LL-7	I_{CC1}	—	105	mA
	KM48C512LL-8		—	90	mA
	KM48C512LL-10		—	75	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM48C512LL-7	I_{CC3}	—	105	mA
	KM48C512LL-8		—	90	mA
	KM48C512LL-10		—	75	mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC} = min.)	KM48C512LL-7	I_{CC4}	—	85	mA
	KM48C512LL-8		—	75	mA
	KM48C512LL-10		—	65	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		I_{CC5}	—	100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min.)	KM48C512LL-7	I_{CC6}	—	105	mA
	KM48C512LL-8		—	90	mA
	KM48C512LL-10		—	75	mA
Self Refresh Current $\overline{RAS}$ = $\overline{CAS}$ = V_{IL} $\overline{WE}$ = $\overline{OE}$ = A0 ~ A9: V_{CC}-0.2V or 0.2V DQ1 ~ 8 = V_{CC}-0.2V, 0.2V or OPEN		I_{CC8}	—	200	μA

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any Input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test=0V)	I_{LL}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	I_{OL}	-10	10	μA
Output High Voltage Level(I_{OH}= -5mA)	V_{OH}	2.4	—	V
Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS} = V_{IL}$. In I_{CC4}, Address can be changed maximum once while $\overline{CAS} = V_{IH}$.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_8)	C_{DQ}	—	7	pF

AC CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, V_{CC} = 5.0V ± 10%, See notes 1, 2)

Parameter	Symbol	KM48C512LL-7		KM48C512LL-8		KM48C512LL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	180		200		240		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	55	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any Input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test=0V)	I_{LL}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	I_{OL}	-10	10	μA
Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS} = V_{IL}$. In I_{CC4}, Address can be changed maximum once while $\overline{CAS} = V_{IH}$.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	-	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1-DQ_9)	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC} = 5.0V ± 10%, See notes 1, 2)

Parameter	Symbol	KM48C512LL-7		KM48C512LL-8		KM48C512LL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	180		200		240		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	55	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	

AC CHARACTERISTICS (Continued)

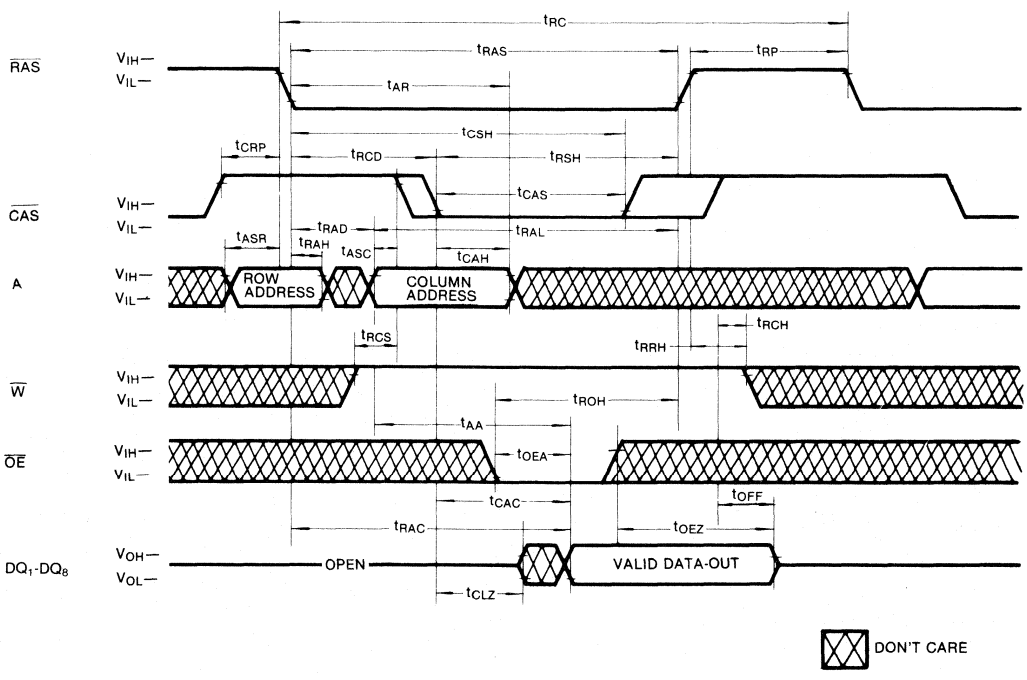
Parameter	Symbol	KM48C512LL-7		KM48C512LL-8		KM48C512LL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command set-up time	t_{WCS}	0		0		0		ns	8
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RASS}	100		100		100		μs	
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RPS}	130		150		180		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{CHS}	0		0		0		ns	
Refresh period (self-refresh)	t_{REF}		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	45		45		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	95		105		130		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	60		65		75		ns	8
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3
Fast page mode cycle time	t_{PC}	45		50		55		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	95		100		115		ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
Access time from $\overline{OE}$	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data-in delay time	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} to V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min),the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

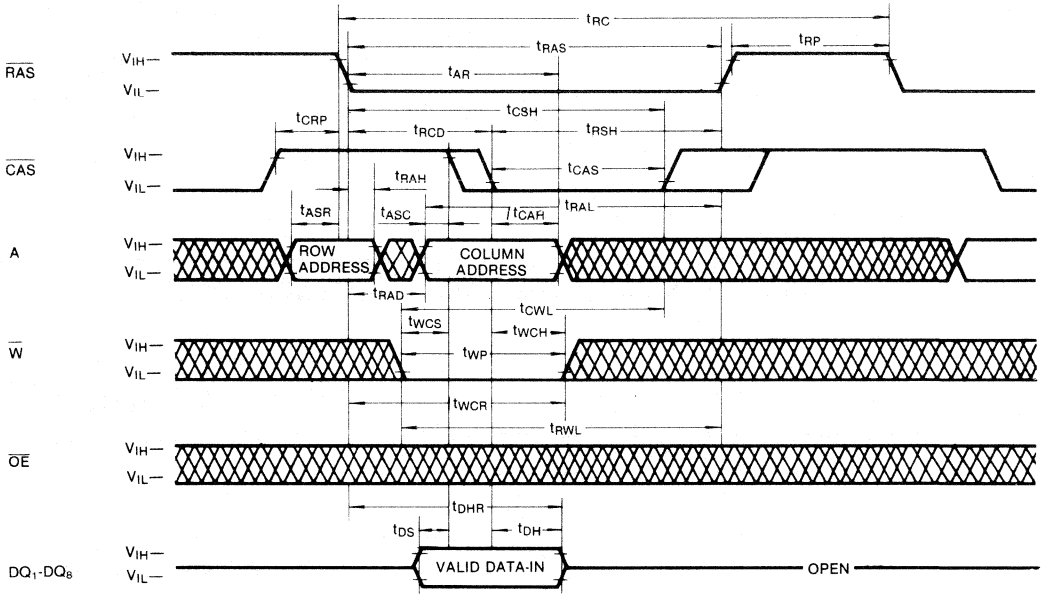
TIMING DIAGRAMS

READ CYCLE

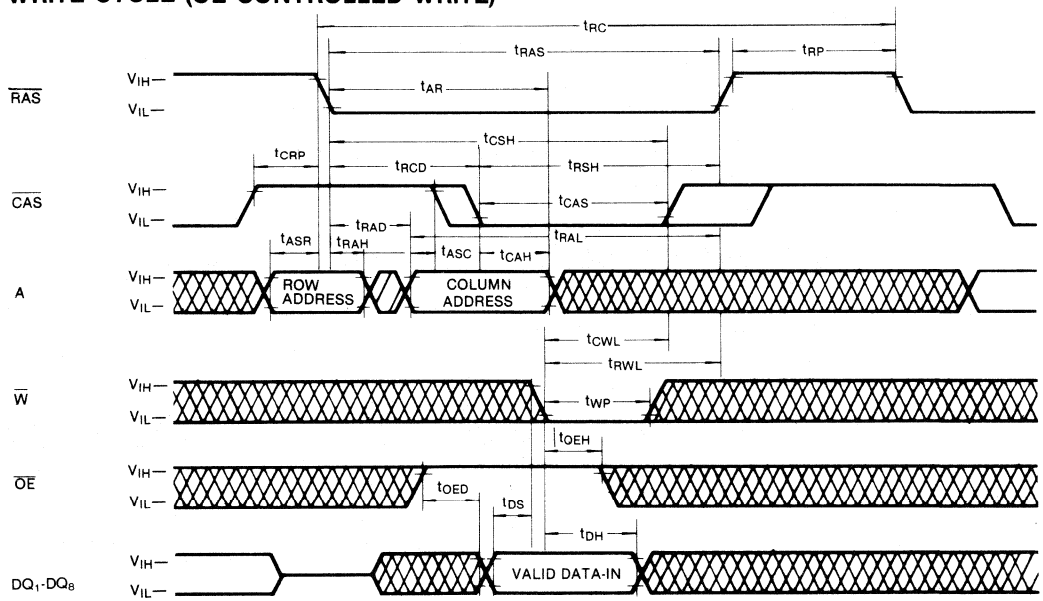


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

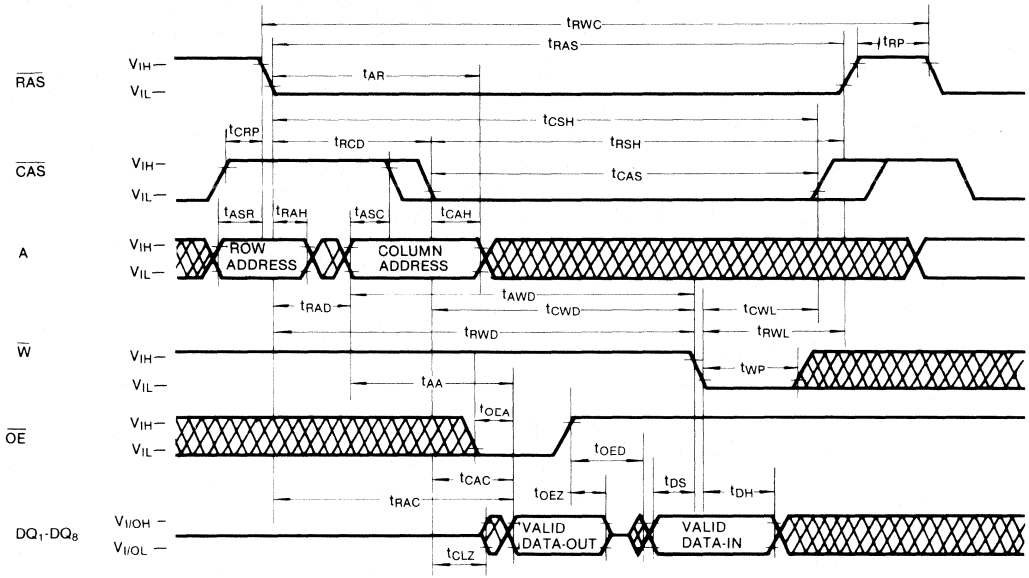


WRITE CYCLE (OE CONTROLLED WRITE)

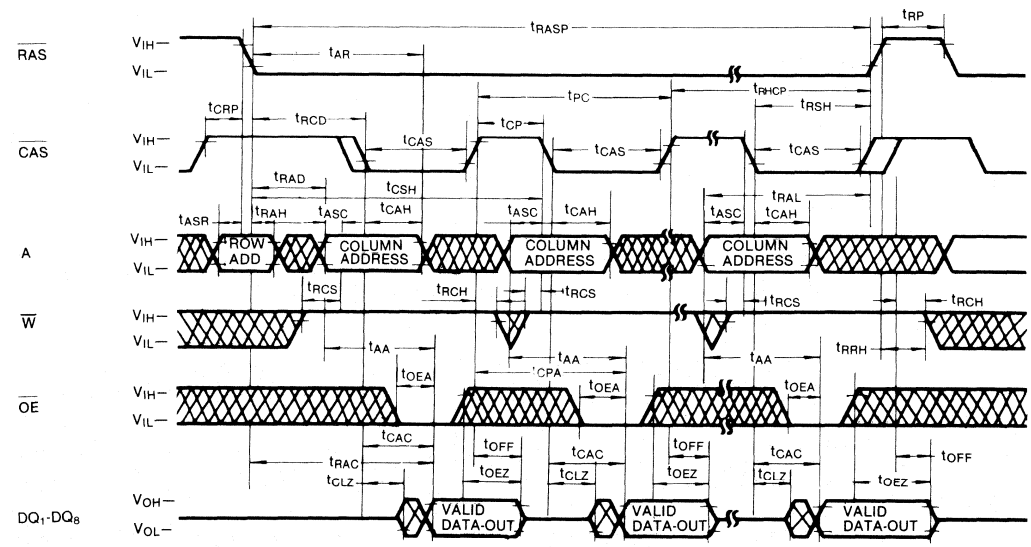


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



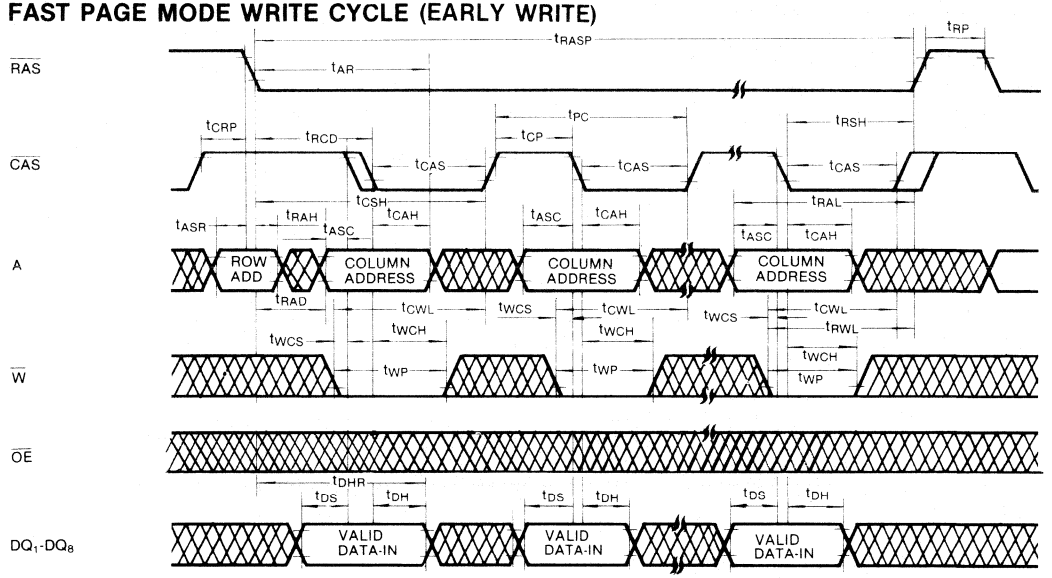
FAST PAGE MODE READ CYCLE



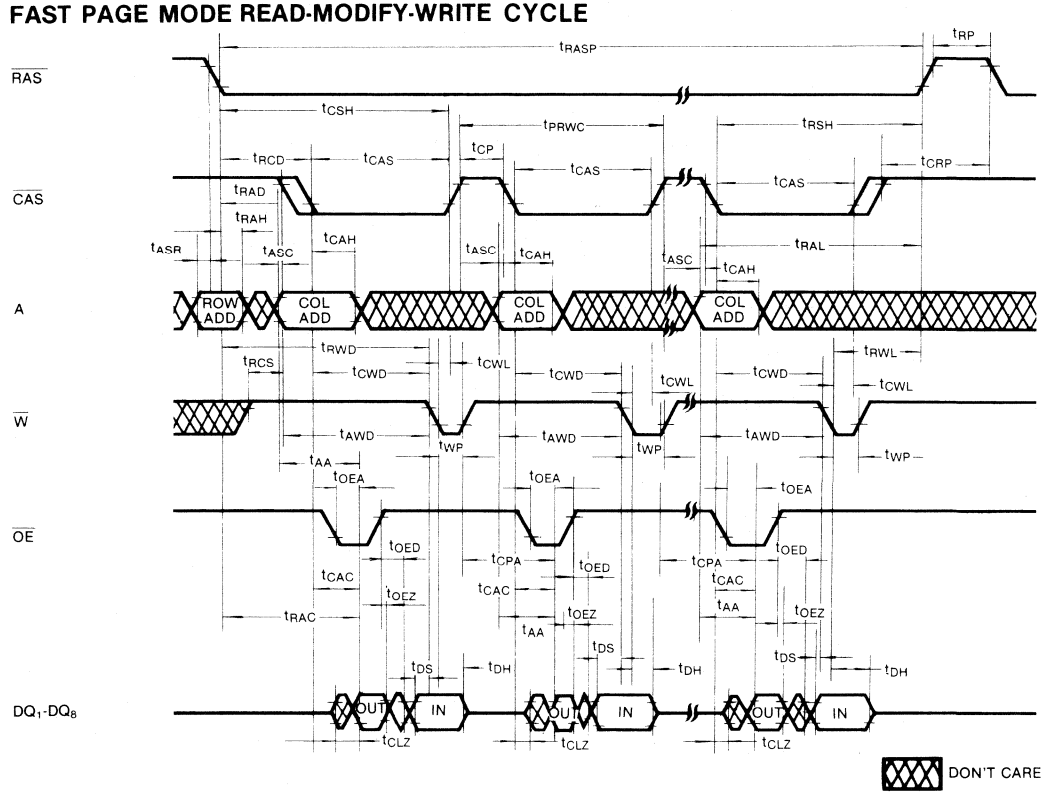
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



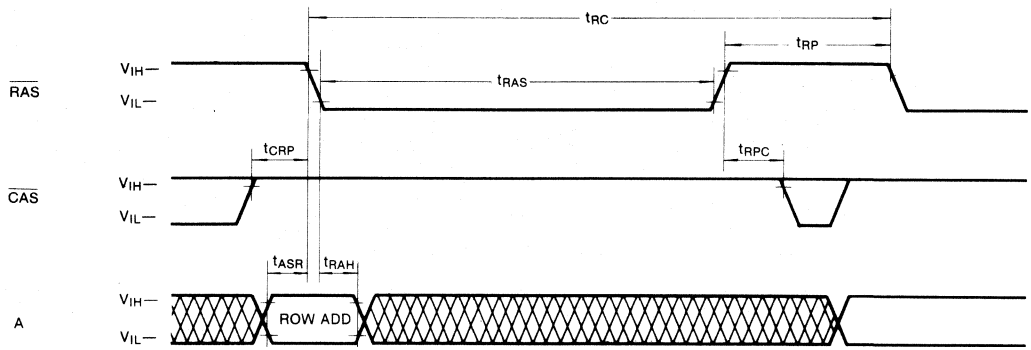
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

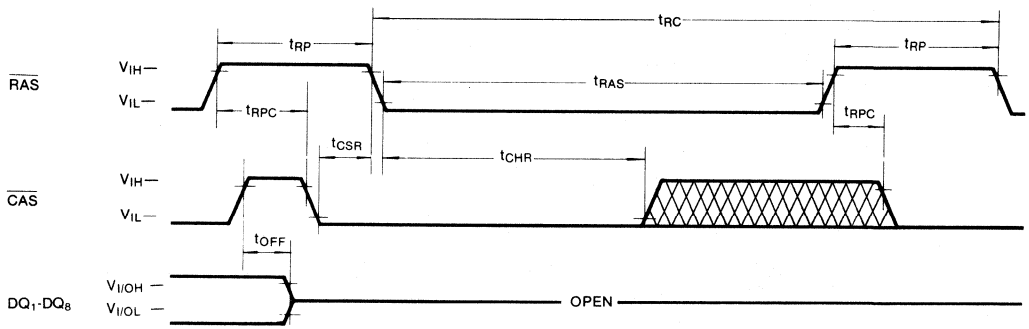
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



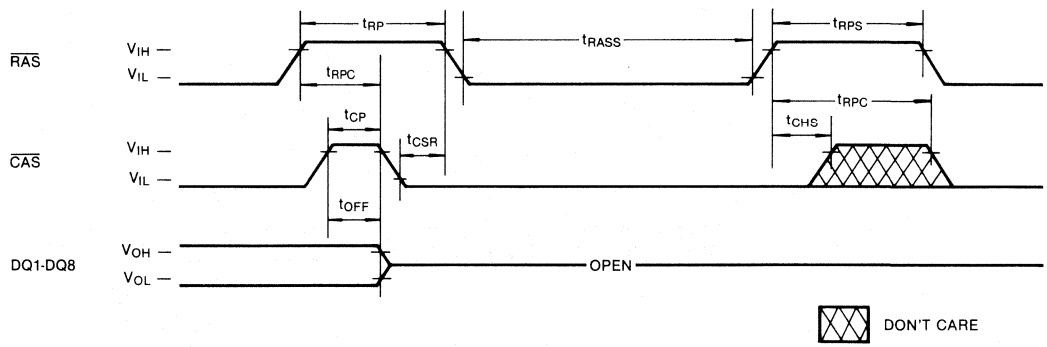
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care



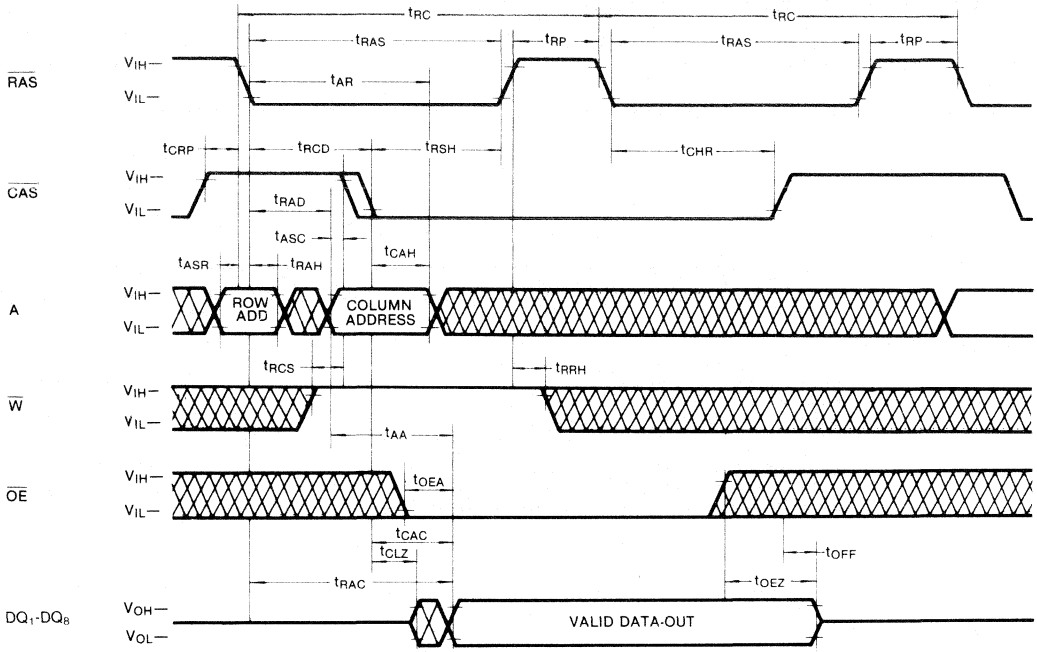
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care

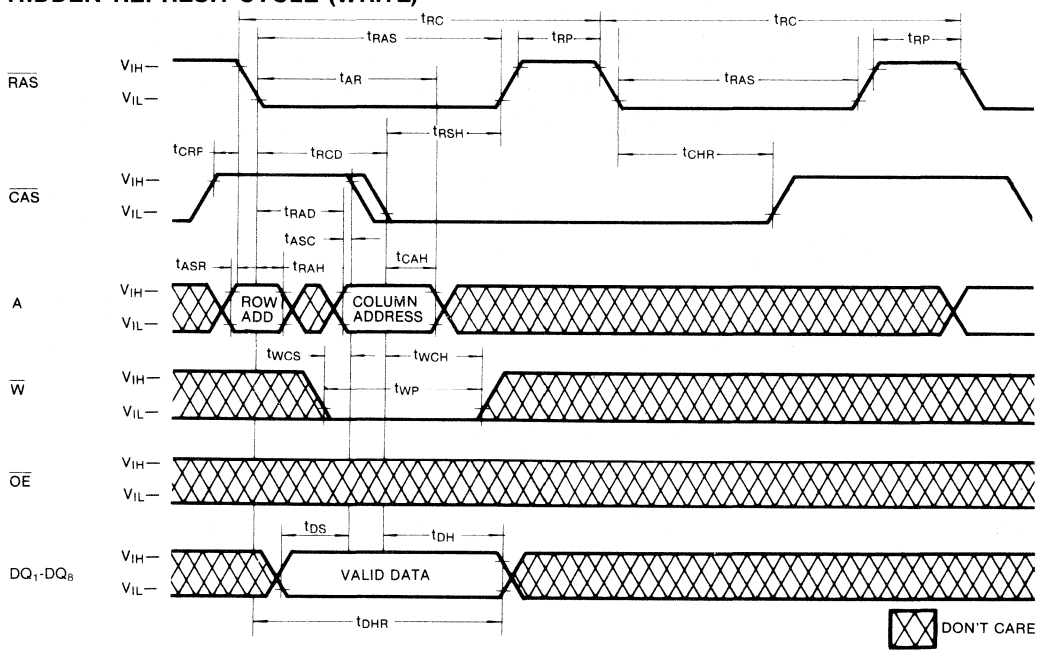


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

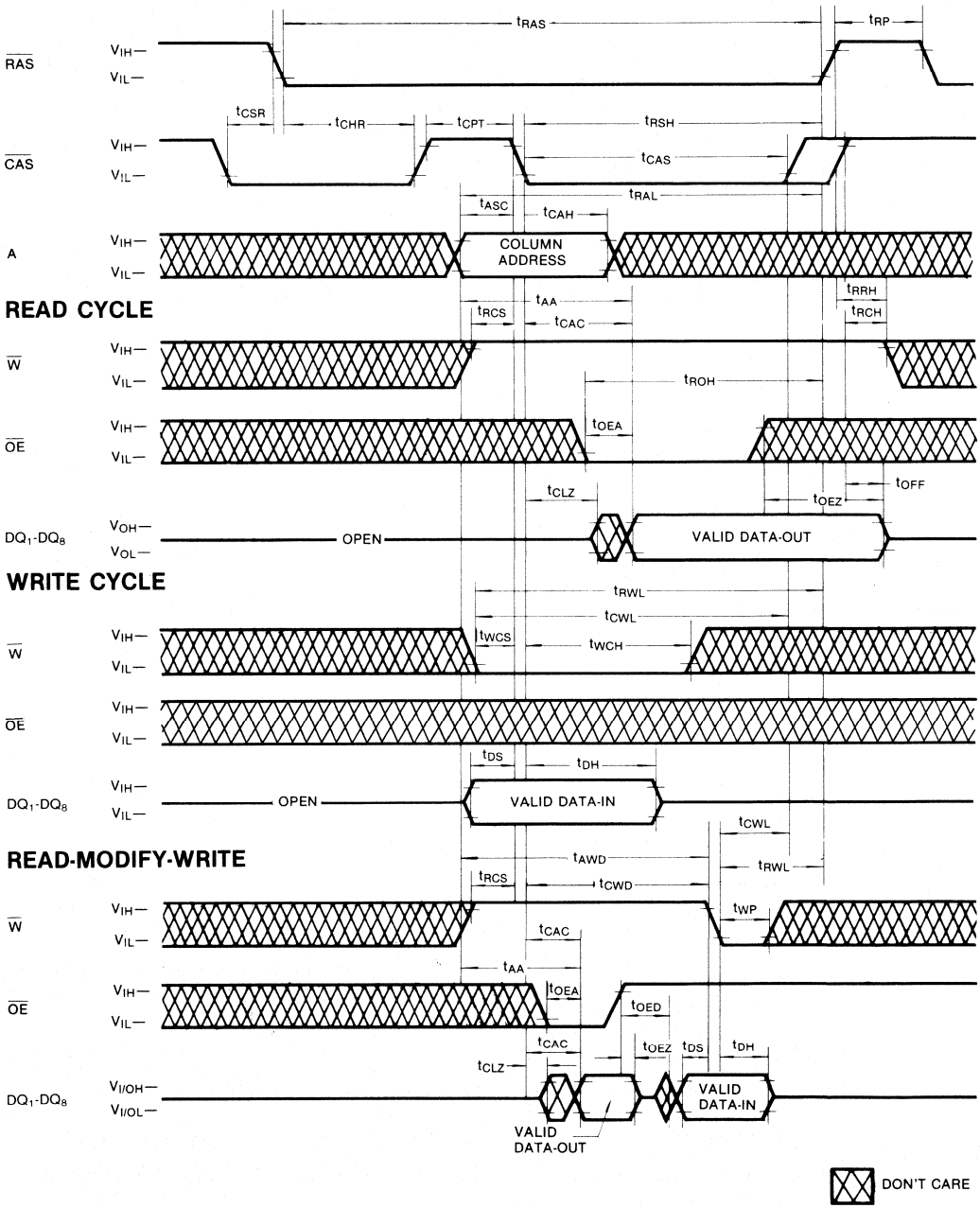


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM48C512LL contains 4,194,304 memory locations arranged in 8 groups of 524,288 × 1 bit each. Ninteen address bits are required to address a particular memory location. Since the KM48C512LL has only 10 address input pins, time multiplexed addressing is used to input 10 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM48C512LL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM48C512LL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM48C512LL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM48C512LL can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$, $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 8-bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cells. This cycle is achieved by bringing W low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The $\overline{OE}$ input must be low during the time defined by t_{OEA} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM48C512LL DQ pins.

Data Output

The KM48C512LL has a three-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}), the outputs are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs enter into the low impedance state in the time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM48C512LL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} times are not met)

DEVICE OPERATION (Continued)

Refresh

The data in the KM48C512LL is stored as a charge on microscopic capacitor within each memory cell. The stored charge tends to dissipate over time and will affect data integrity if the charge is not periodically refreshed. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 1024 row address (A0-A9).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM48C512LL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ transitions low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending either input active time and cycling $\overline{RAS}$. The hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Self Refresh: The self refresh is $\overline{CAS}$-before-$\overline{RAS}$ refresh to be used for long periods of standby, such as a battery back-up. In normal $\overline{CAS}$-before-$\overline{RAS}$ condition, when $\overline{RAS}$ is held low above 100μs an internal timer activates an refresh operation of consecutive row addresses in DRAM. The self refresh mode is exited when either $\overline{RAS}$ or $\overline{CAS}$ goes high(V_{IH}).

Other Refresh Methods: It is also possible to refresh the KM48C512LL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM48C512LL has Fast page mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is asserted high and then low again while $\overline{RAS}$ is asserted low, the read and write operations are enabled. In this method, the row address bits A0 through A9 are supplied by on chip refresh counter.

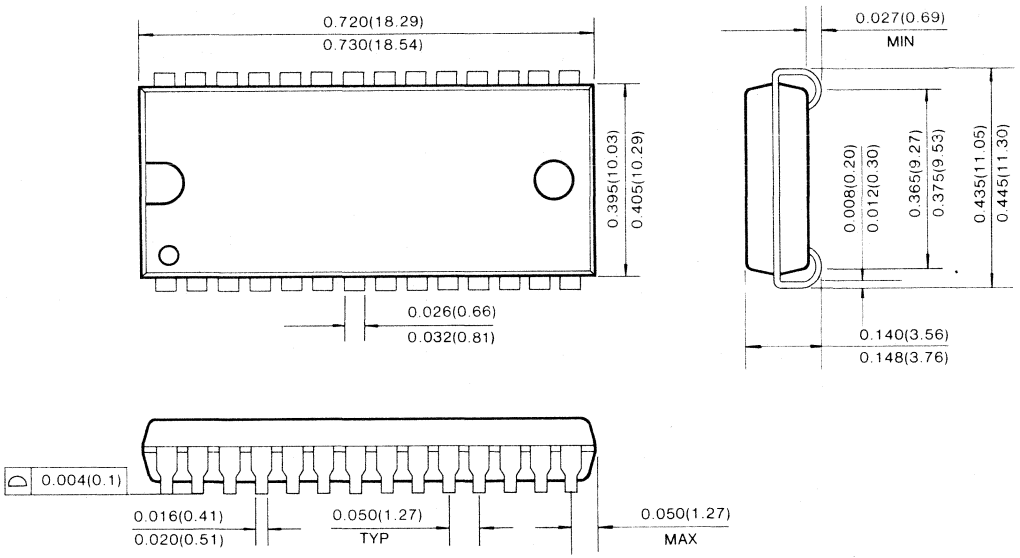
Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM48C512LL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held a valid V_{IH} in order to minimize the power-up current.

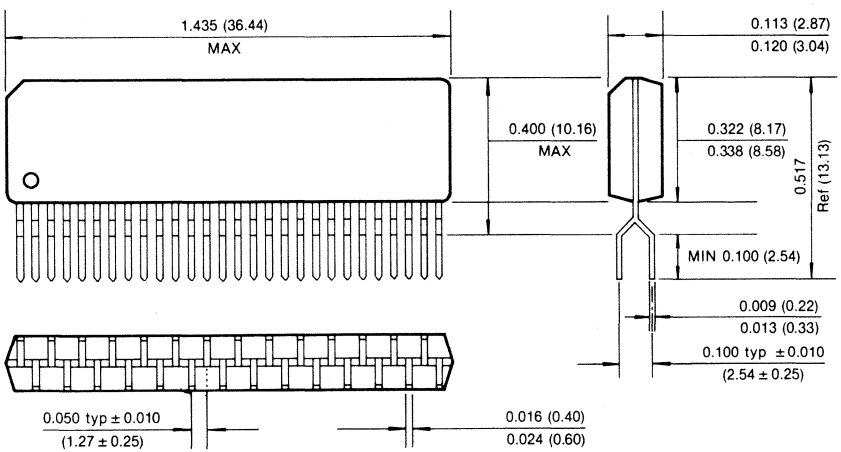
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)

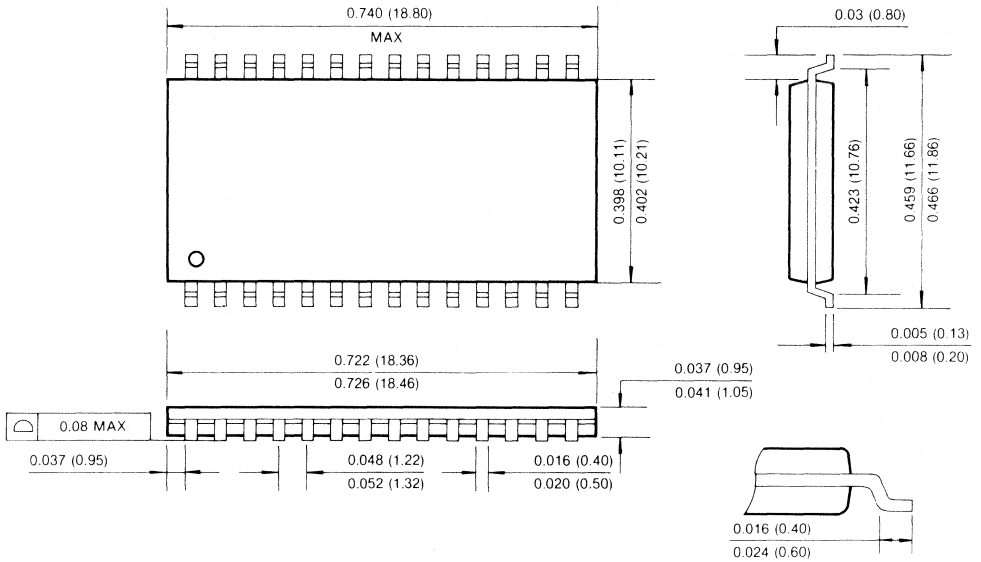


28-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

Units: Inches (millimeters)



512K x 9 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM49C512/L/SL-7	70ns	20ns	130ns
KM49C512/L/SL-8	80ns	20ns	150ns
KM49C512/L/SL-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Dual +5V±10% power supply**
- **Refresh Cycle**
  - **— 1024 cycle/16ms (Normal)**
  - **— 1024 cycle/128ms (L-version)**
  - **— 1024 cycle/256ms (SL-version)**
- **Power Dissipation**
  - **— Standby: 11mW (Normal)**
    1.1mW (L-version)
    0.55mW (SL-version)
  - **— Active (70/80/100): 605/523/440mW**
- **JEDEC Standard pinout**
- **Available in Plastic SOJ, ZIP and TSOP II**

GENERAL DESCRIPTION

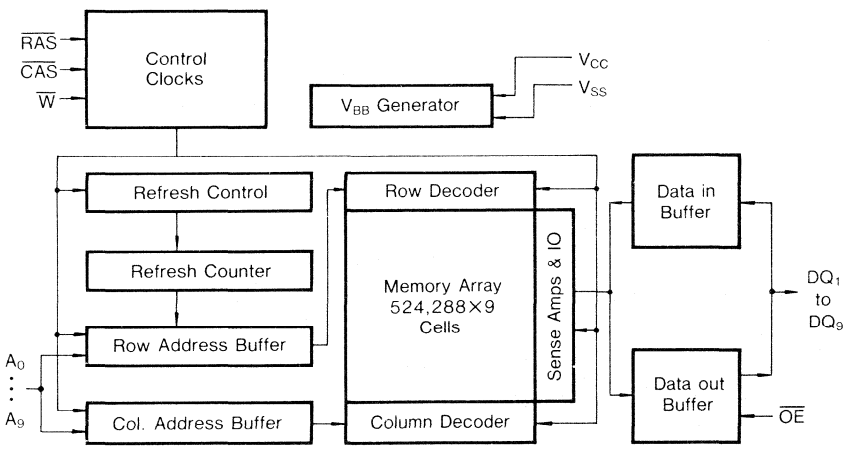
The Samsung KM49C512/L/SL is a CMOS high speed 524,288 bit x 9 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM49C512/L/SL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM49C512/L/SL is fabricated using Samsung's advanced CMOS process.

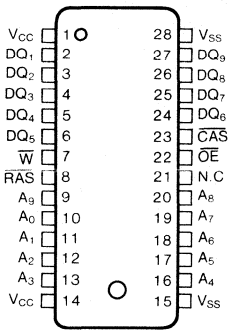
2

FUNCTIONAL BLOCK DIAGRAM



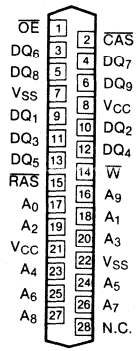
PIN CONFIGURATION (Top Views)

• KM49C512J/LJ/SLJ



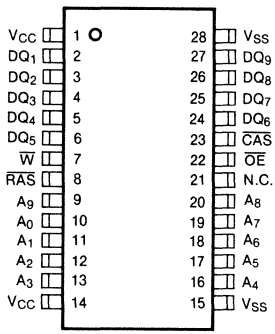
(SOJ)

• KM49C512Z/LZ/SLZ



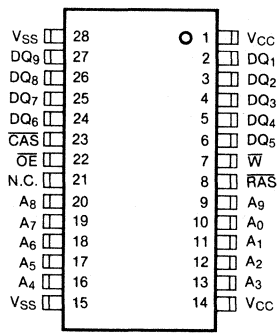
(ZIP)

• KM49C512T/LT/SLT



(TSOP(II)-Forward Type)

• KM49C512TR/LTR/SLTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A_0-A_9	Address Input
DQ_{1-9}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe

Pin Name	Pin Function
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power(+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC} = min.)	KM49C512/L/SL-7 KM49C512/L/SL-8 KM49C512/L/SL-10	I_{CC1}	— — —	110 95 80	mA mA mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM49C512/L/SL-7 KM49C512/L/SL-8 KM49C512/L/SL-10	I_{CC3}	— — —	110 95 80	mA mA mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC} = min.)	KM49C512/L/SL-7 KM49C512/L/SL-8 KM49C512/L/SL-10	I_{CC4}	— — —	85 75 65	mA mA mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)	KM49C512 KM49C512L KM49C512SL	I_{CC5}	— — —	1 200 100	mA μA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min.)	KM49C512/L/SL-7 KM49C512/L/SL-8 KM49C512/L/SL-10	I_{CC6}	— — —	110 95 80	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode Input High Voltage (V_{IH}) = V_{CC}-0.2V Input Low Voltage (V_{IL}) = 0.2V $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V D_{IN} = Don't Care T_{RC}=125μS(L-ver), T_{RC}=250μS(SL-ver), T_{RAS}=T_{RAS}min.~1μS,	KM49C512L KM49C512SL	I_{CC7}	— —	300 150	μA μA

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any Input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test=0V)	I_{LL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	I_{OL}	−10	10	μA
Output High Voltage Level(I_{OH}=−5mA)	V_{OH}	2.4	—	V
Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS} = V_{IL}$. In I_{CC4}, Address can be changed maximum once while $\overline{CAS} = V_{IH}$.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_9)	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1, 2)

Parameter	Symbol	KM49C512/L/SL-7		KM49C512/L/SL-8		KM49C512/L/SL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	180		200		240		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	55	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	

AC CHARACTERISTICS (Continued)

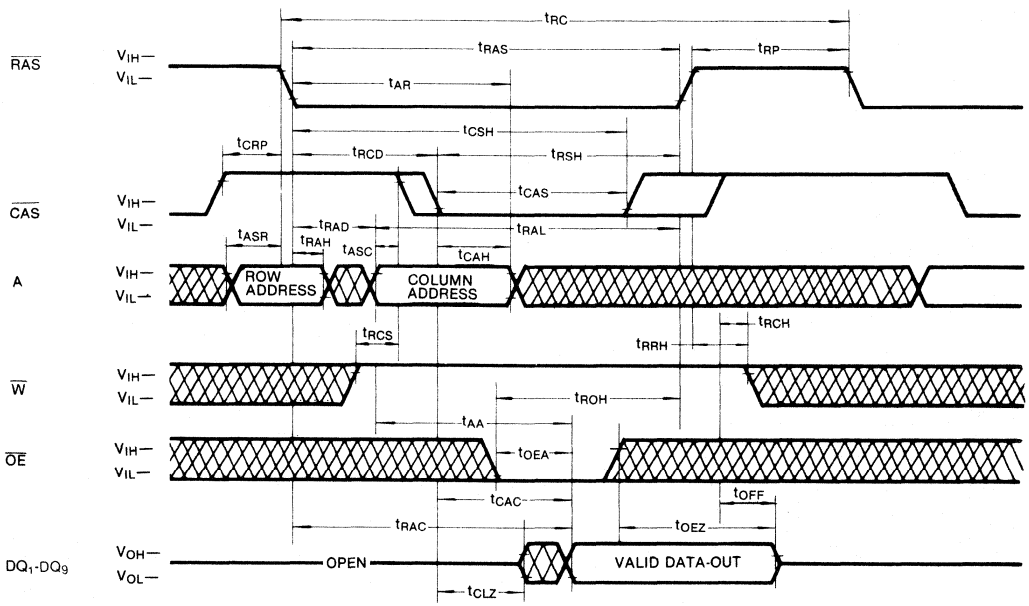
Parameter	Symbol	KM49C512/L/SL-7		KM49C512/L/SL-8		KM49C512/L/SL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command set-up time	t_{WCS}	0		0		0		ns	8
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Refresh period (L-version)	t_{REF}		128		128		128	ms	
Refresh period (SL-version)	t_{REF}		256		256		256	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	45		45		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	95		105		130		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	60		65		75		ns	8
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3
Fast page mode cycle time	t_{PC}	45		50		55		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	95		100		115		ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
Access time from $\overline{OE}$	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data-in delay time	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} to V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min),the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

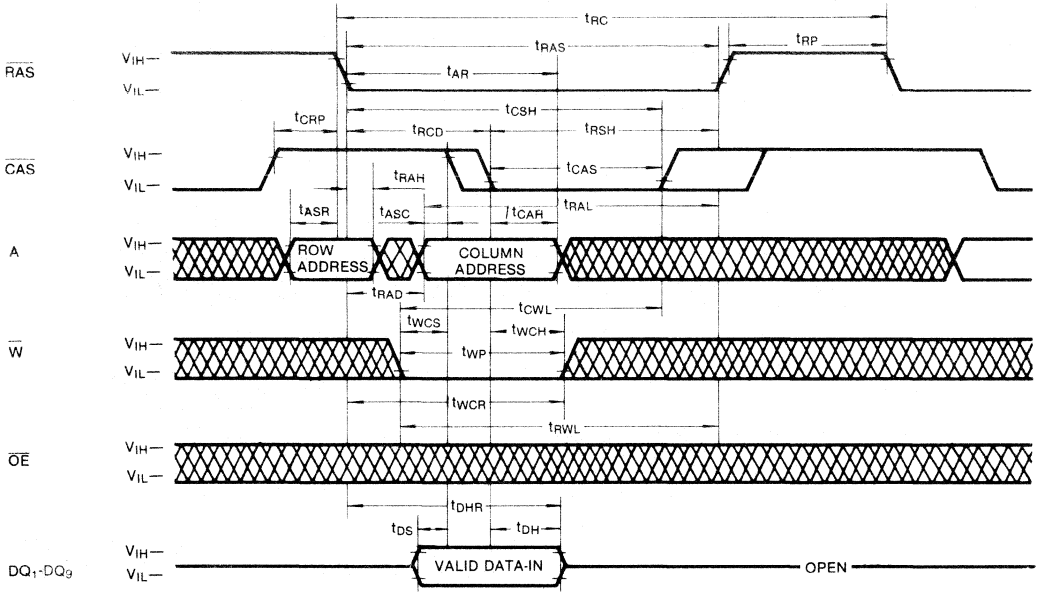
TIMING DIAGRAMS

READ CYCLE

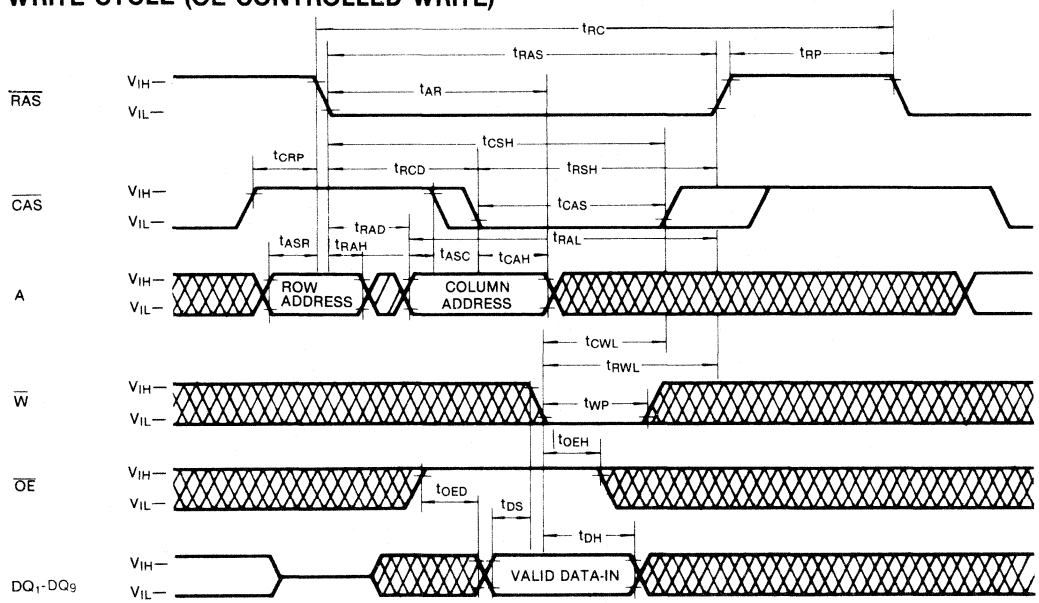


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

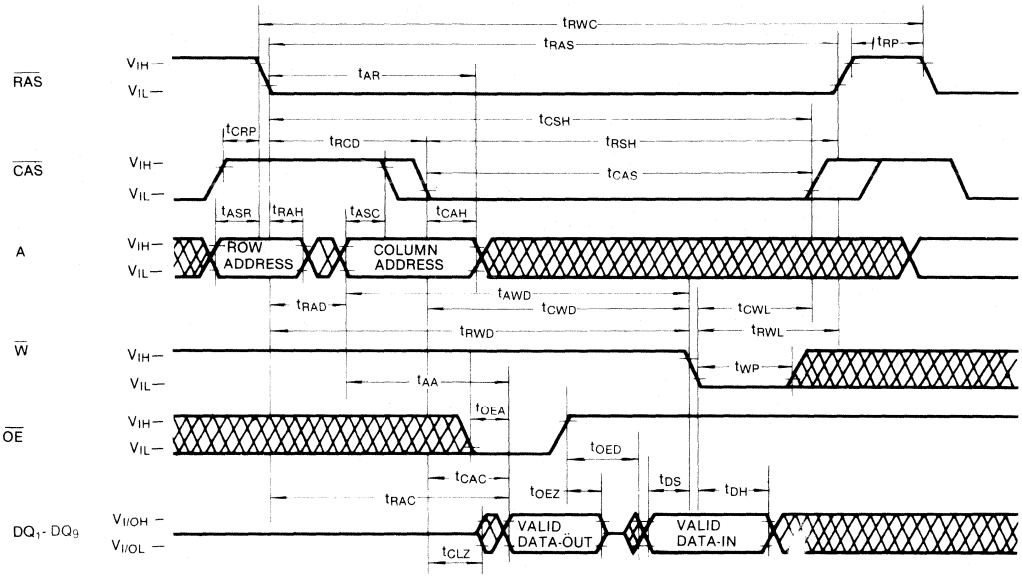


WRITE CYCLE (OE CONTROLLED WRITE)

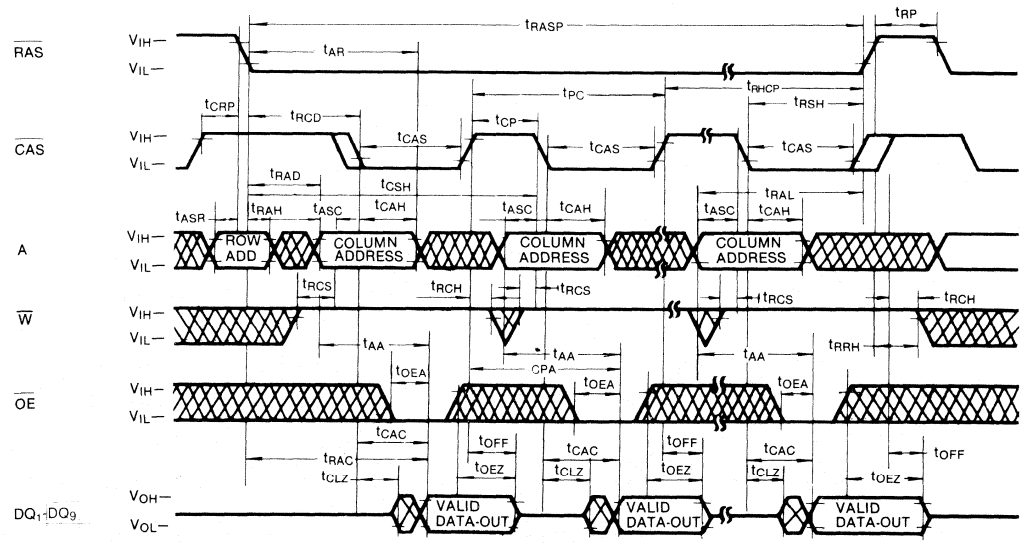


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



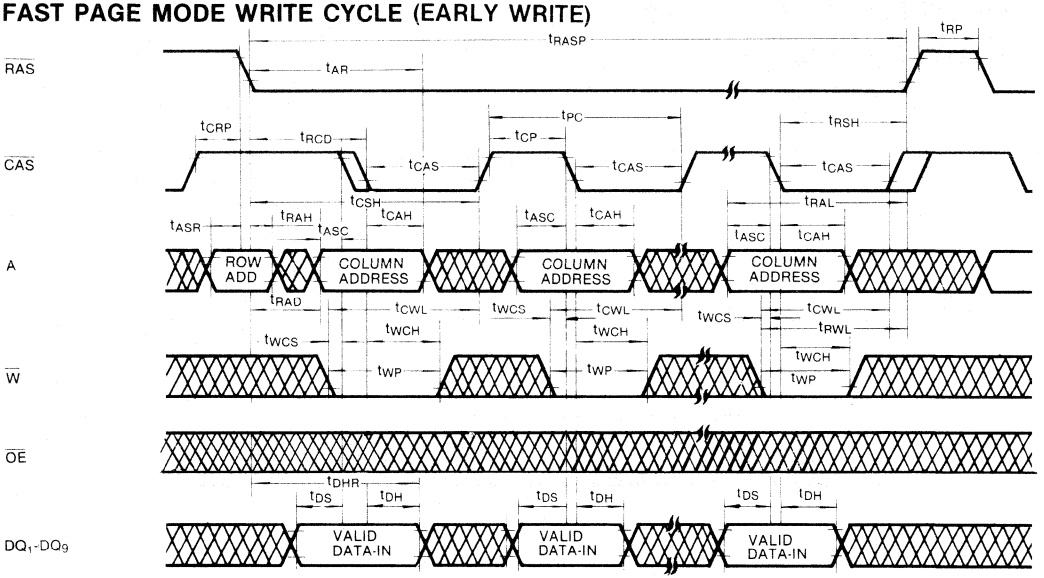
FAST PAGE MODE READ CYCLE



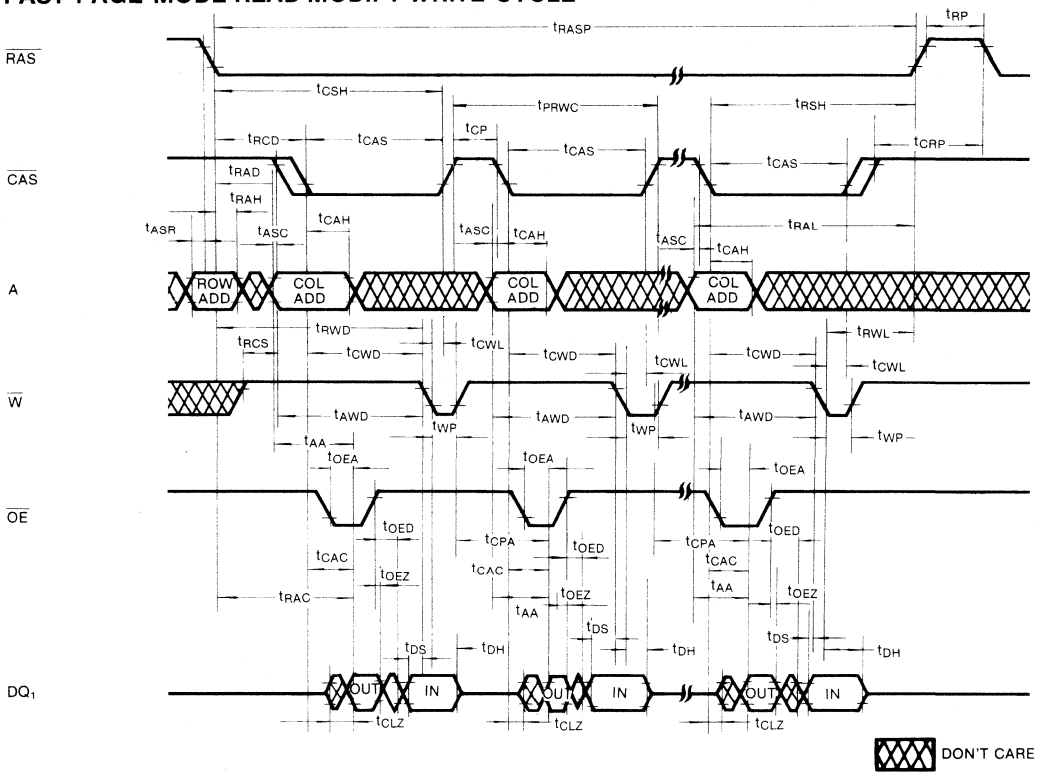
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



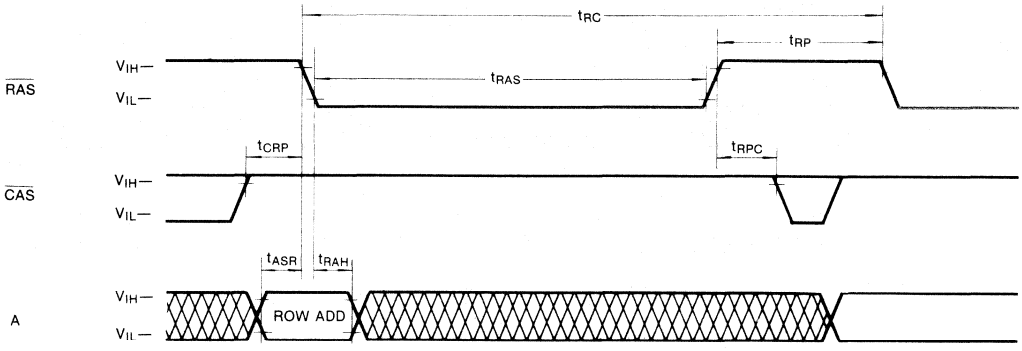
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

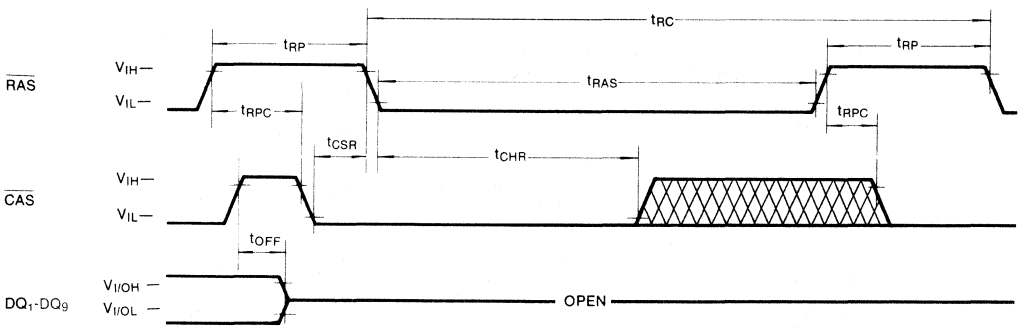
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

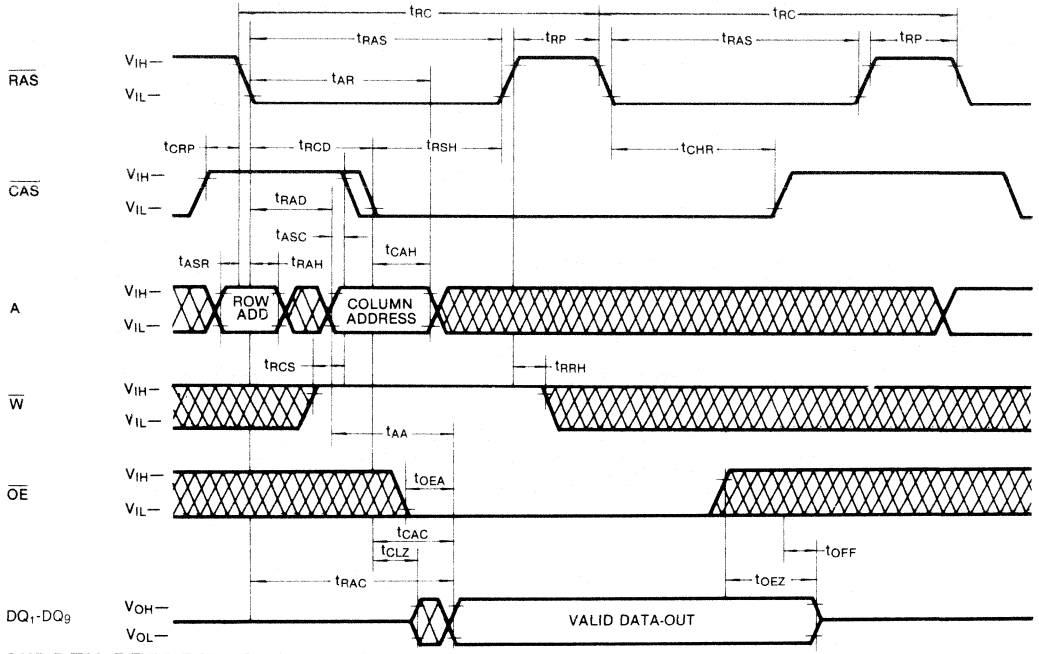
NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care



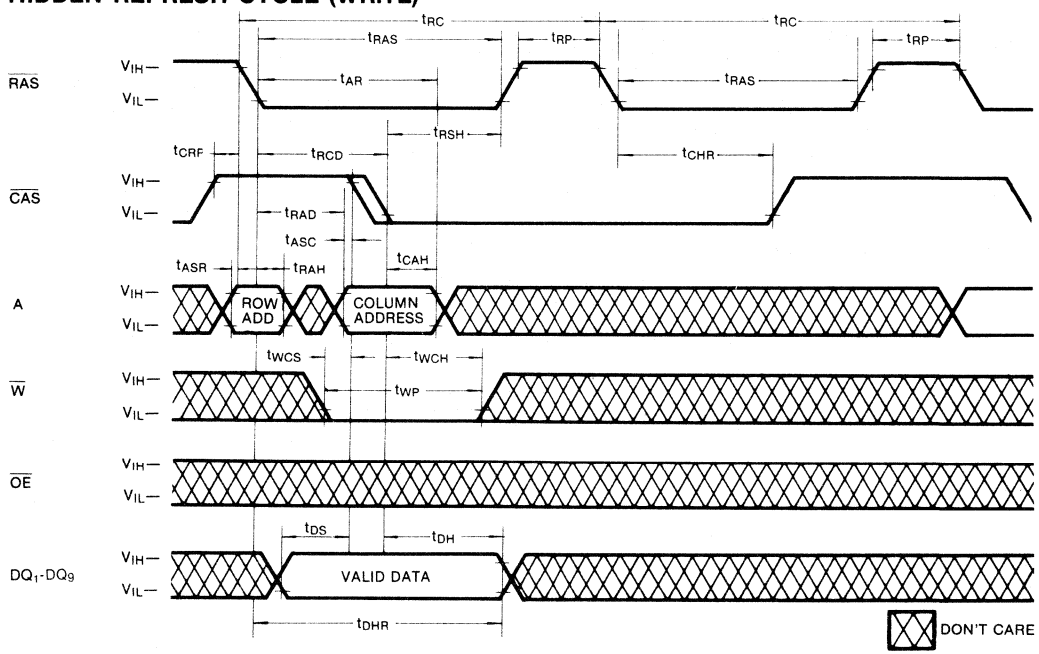
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

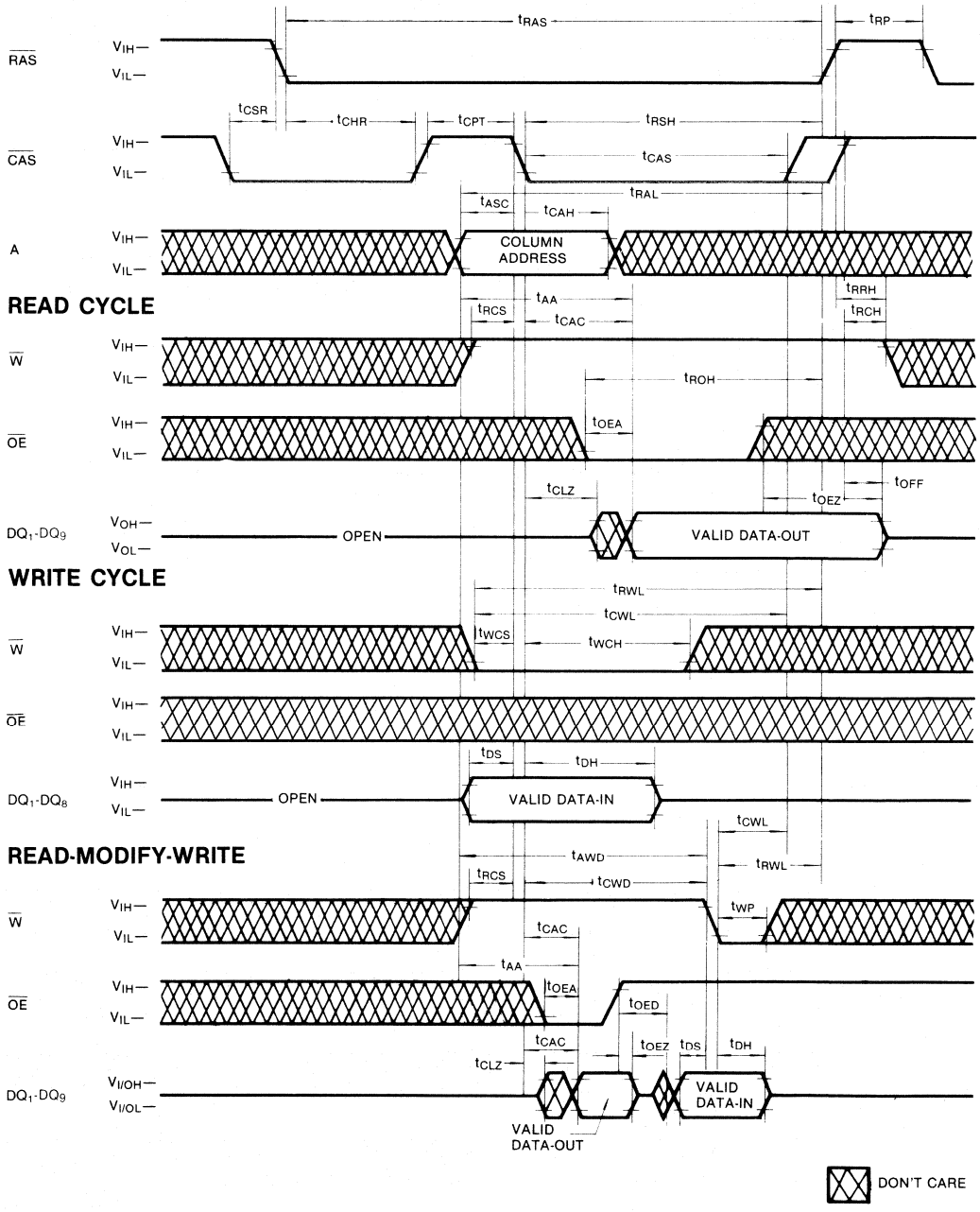


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM49C512/L/SL contains 4,718,592 memory locations arranged in 9 groups of 524,288 × 1 bit each. Nineteen address bits are required to address a particular memory location. Since the KM49C512/L/SL has only 10 address input pins, time multiplexed addressing is used to input 10 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM49C512/L/SL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM49C512/L/SL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM49C512/L/SL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM49C512/L/SL can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$, $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 9-bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cells. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The $\overline{OE}$ input must be low during the time defined by t_{OEA} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM49C512/L/SL DQ pins.

Data Output

The KM49C512/L/SL has a three-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}), the outputs are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs enter into the low impedance state in the time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM49C512/L/SL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} times are not met)

DEVICE OPERATION (Continued)

Refresh

The data in the KM49C512/L/SL is stored as a charge on microscopic capacitor within each memory cell. The stored charge tends to dissipate over time and will affect data integrity if the charge is not periodically refreshed. Refresh of the individual storage cells is accomplished by accessing all rows within the refresh period (t_{REF}) off within 16ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 1024 row address (A0-A9).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM49C512/L/SL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ transitions low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending either input active time and cycling $\overline{RAS}$. The hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM49C512/L/SL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM49C512/L/SL has Fast page mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is asserted high and then low again while $\overline{RAS}$ is asserted low, the read and write operations are enabled. In this method, the row address bits A0 through A9 are supplied by on chip refresh counter.

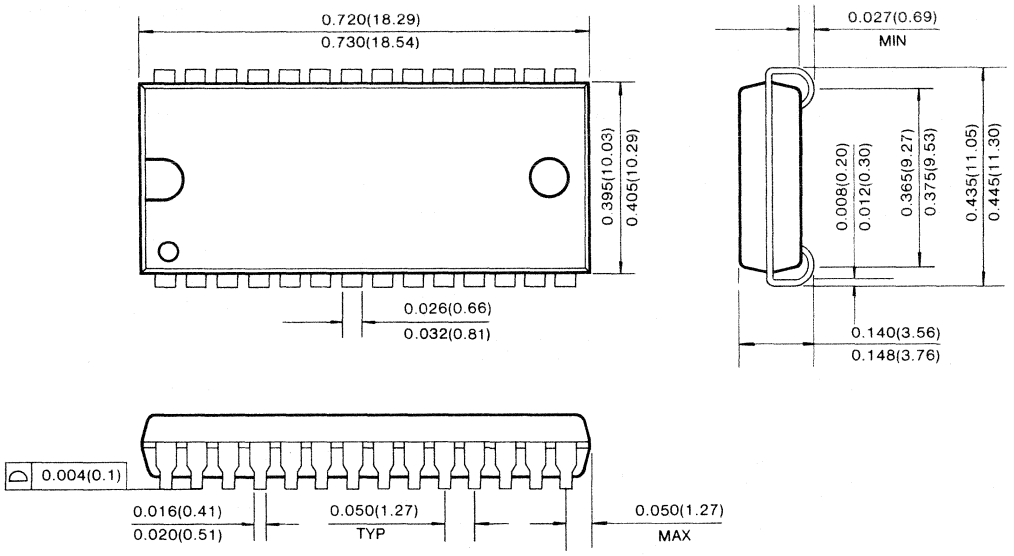
Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM49C512/L/SL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held a valid V_{IH} in order to minimize the power-up current.

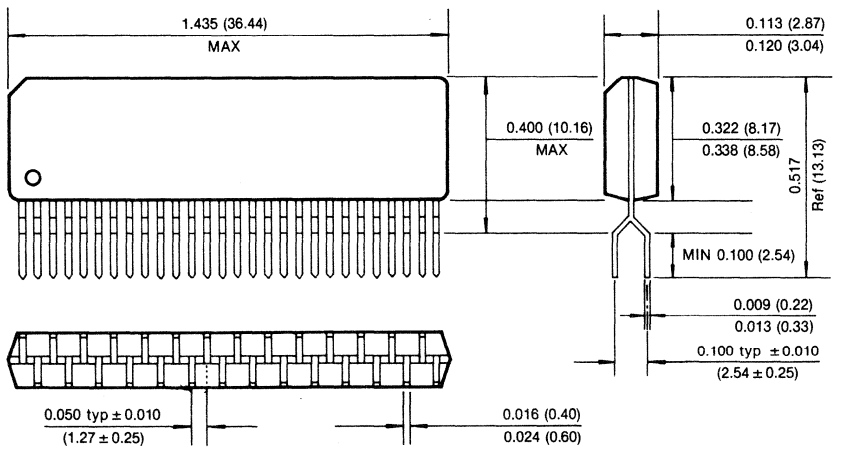
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)

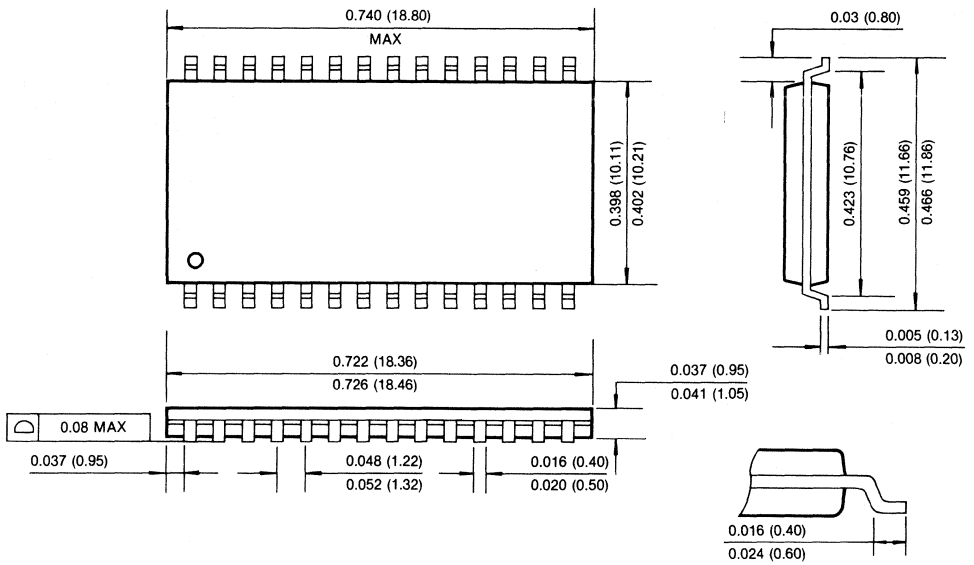


28-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

Units: Inches (millimeters)



512K x 9 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM49C512LL-7	70ns	20ns	130ns
KM49C512LL-8	80ns	20ns	150ns
KM49C512LL-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Dual +5V±10% power supply**
- **Refresh Cycle**
  - **— 1024 cycle/128ms (self-refresh)**
- **Power Dissipation**
  - **— Standby: 11mW (Normal)**
    0.55mW (self-refresh)
  - **— Active (70/80/100): 605/523/440mW**
- **JEDEC Standard pinout**
- **Available in Plastic SOJ, ZIP and TSOP II**

GENERAL DESCRIPTION

The Samsung KM49C512LL is a CMOS high speed 524,288 bit x 9 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM49C512LL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM49C512LL is fabricated using Samsung's advanced CMOS process.

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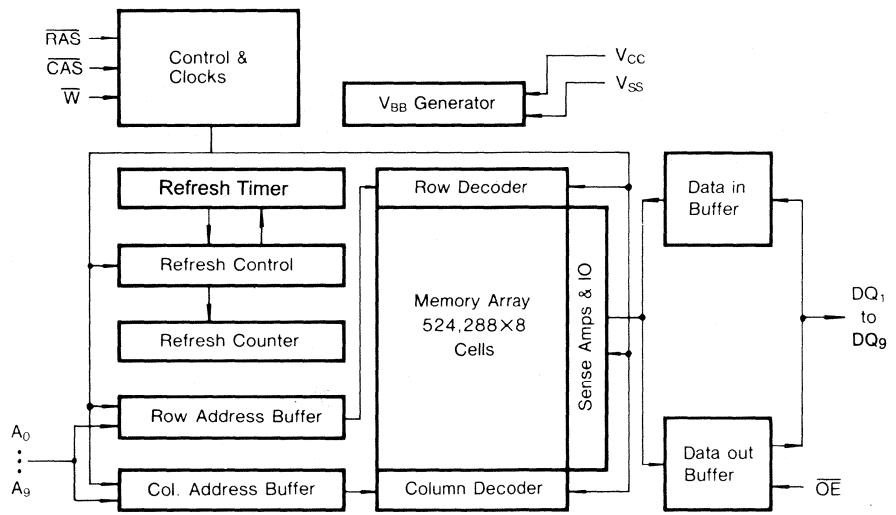
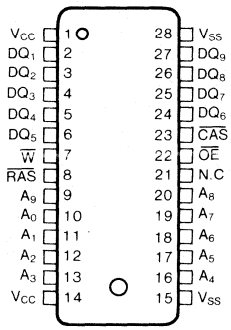
FUNCTIONAL BLOCK DIAGRAM



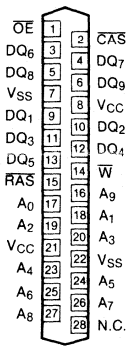
PIN CONFIGURATION (Top Views)

• **KM49C512LLJ**



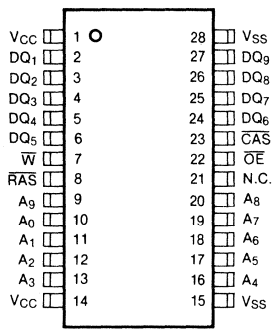
(SOJ)

• **KM49C512LLZ**



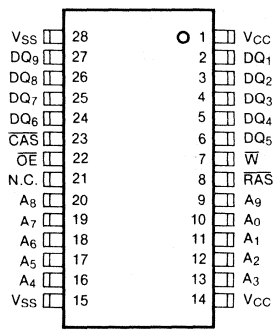
(ZIP)

• **KM49C512LLT**



(TSOP(II)-Forward Type)

• **KM49C512LLTR**



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A_0-A_9	Address Input
DQ_{1-9}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe

Pin Name	Pin Function
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power(+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC} = min.)	KM49C512LL-7	I_{CC1}	—	110	mA
	KM49C512LL-8		—	95	mA
	KM49C512LL-10		—	80	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM49C512LL-7	I_{CC3}	—	110	mA
	KM49C512LL-8		—	95	mA
	KM49C512LL-10		—	80	mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC} = min.)	KM49C512LL-7	I_{CC4}	—	85	mA
	KM49C512LL-8		—	75	mA
	KM49C512LL-10		—	65	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		I_{CC5}	—	100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min.)	KM49C512LL-7	I_{CC6}	—	110	mA
	KM49C512LL-8		—	95	mA
	KM49C512LL-10		—	80	mA
Self Refresh Current $\overline{RAS}$ = $\overline{CAS}$ = V_{IL} $\overline{WE}$ = $\overline{OE}$ = A0 ~ A9: V_{CC}-0.2V or 0.2V DQ1 ~ 9 = V_{CC}-0.2V, 0.2V or OPEN		I_{CC5}	—	200	μA

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any Input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test=0V)	I_{LL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	I_{OL}	−10	10	μA
Output High Voltage Level(I_{OH}=−5mA)	V_{OH}	2.4	—	V
Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS} = V_{IL}$. In I_{CC4}, Address can be changed maximum once while $\overline{CAS} = V_{IH}$.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_9)	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1, 2)

Parameter	Symbol	KM49C512LL-7		KM49C512LL-8		KM49C512LL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	180		200		240		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	55	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	

AC CHARACTERISTICS (Continued)

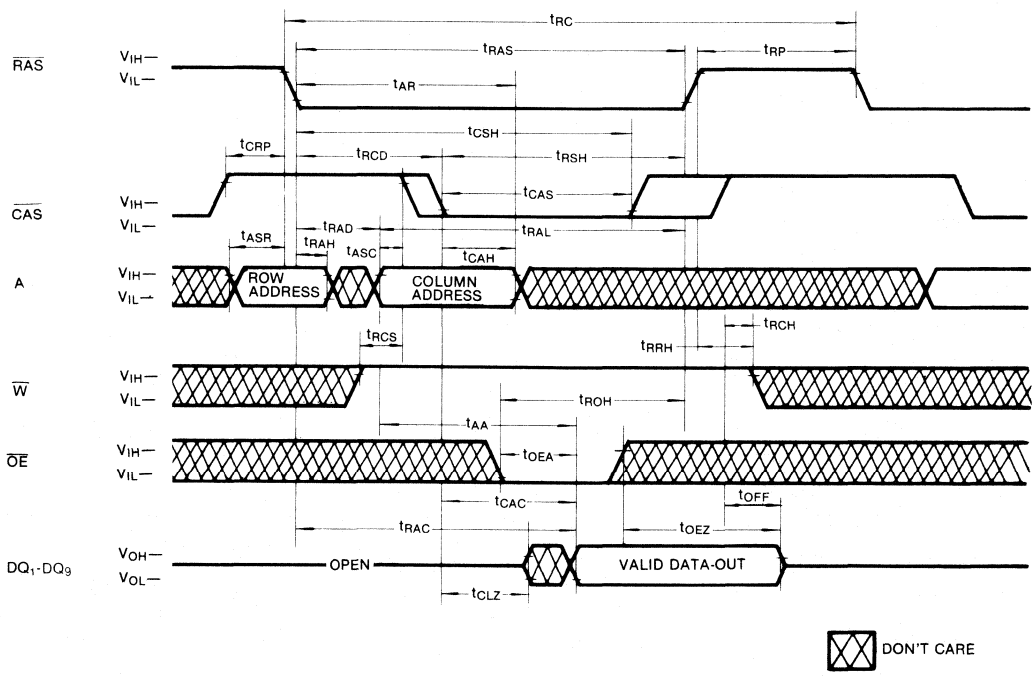
Parameter	Symbol	KM49C512LL-7		KM49C512LL-8		KM49C512LL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command set-up time	t_{WCS}	0		0		0		ns	8
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RASS}	100		100		100		μs	
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RPS}	130		150		180		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{CHS}	0		0		0		ns	
Refresh period (self-refresh)	t_{REF}		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	45		45		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	95		105		130		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	60		65		75		ns	8
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3
Fast page mode cycle time	t_{PC}	45		50		55		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	95		100		115		ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
Access time from $\overline{OE}$	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data-in delay time	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} to V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min),the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

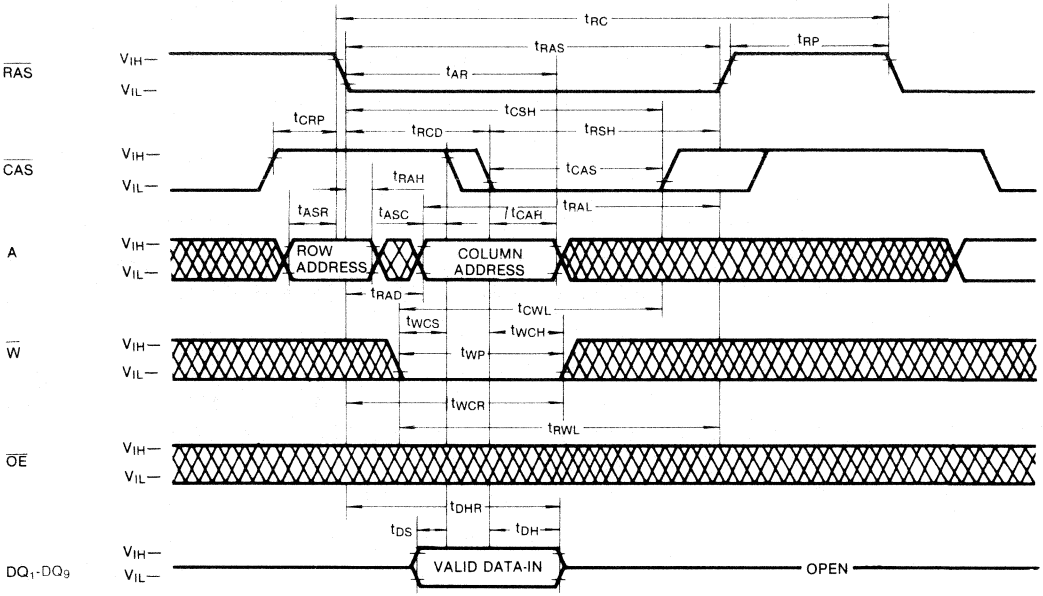
TIMING DIAGRAMS

READ CYCLE

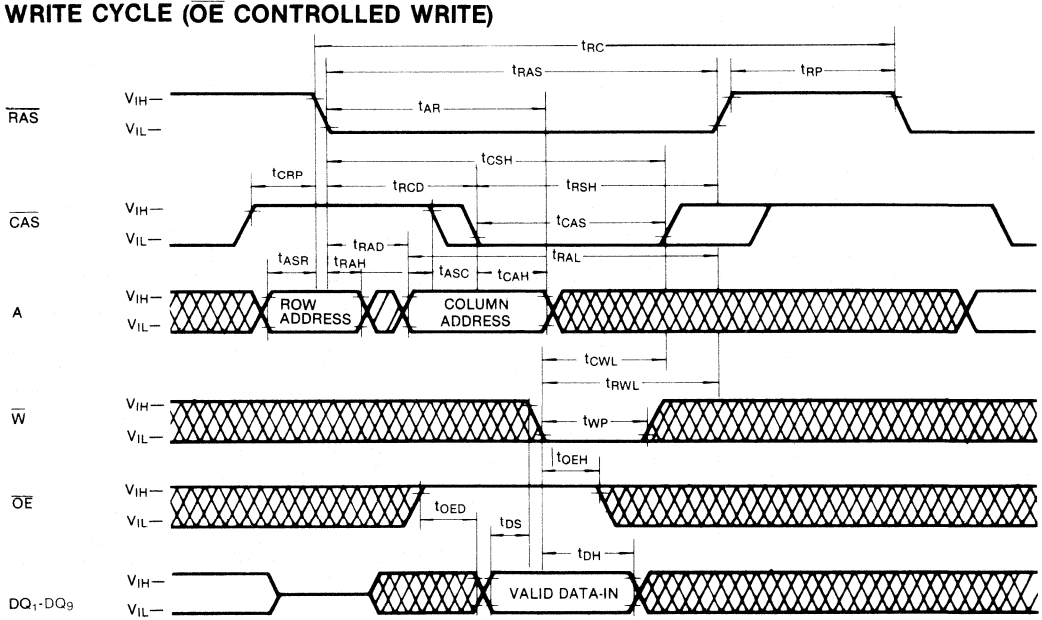


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



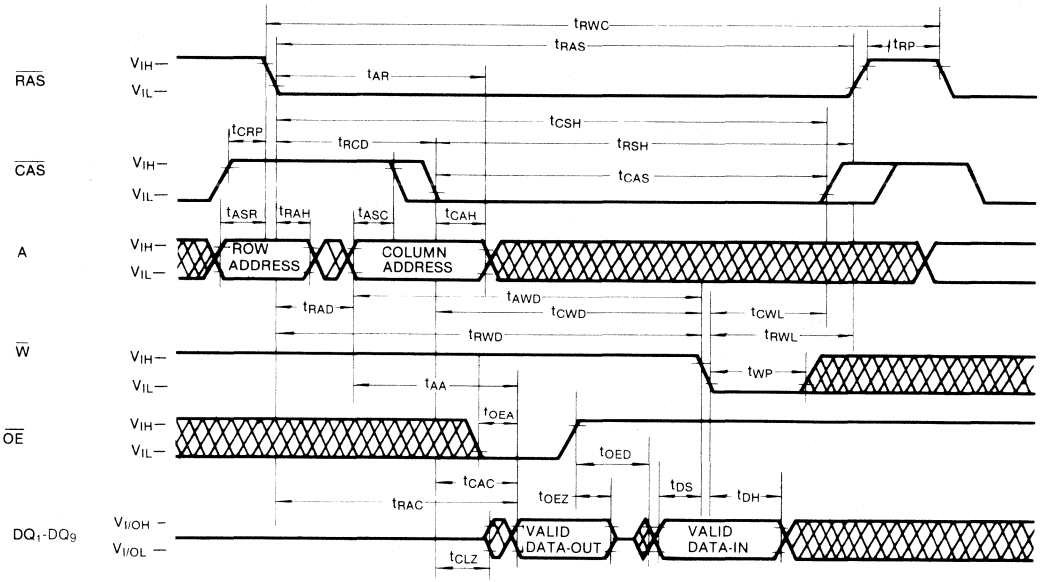
WRITE CYCLE (OE CONTROLLED WRITE)



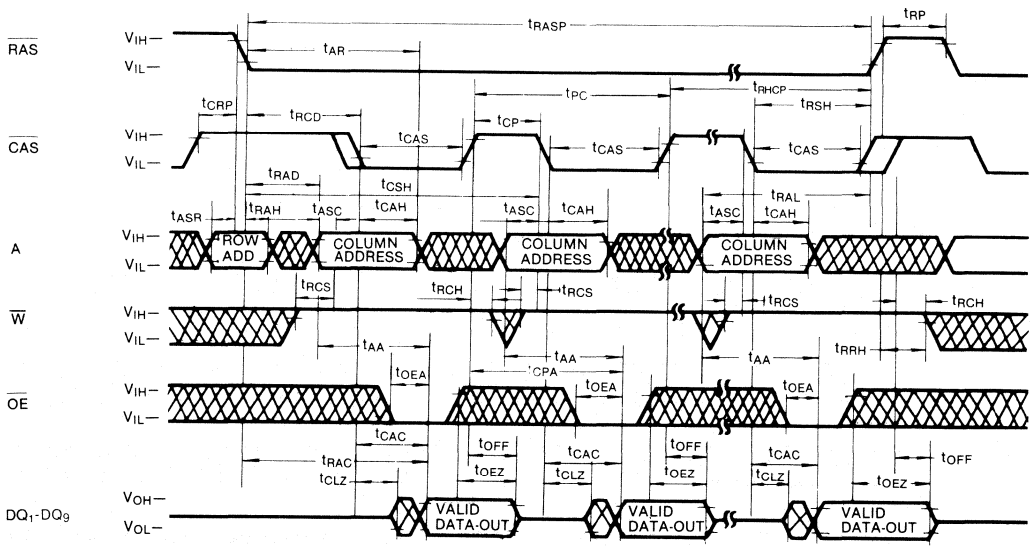
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



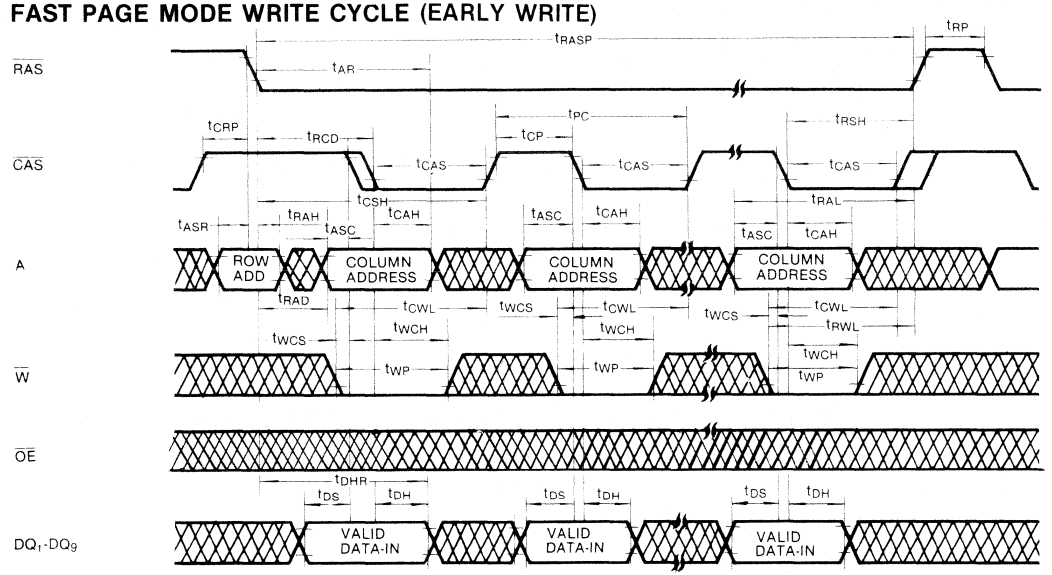
FAST PAGE MODE READ CYCLE



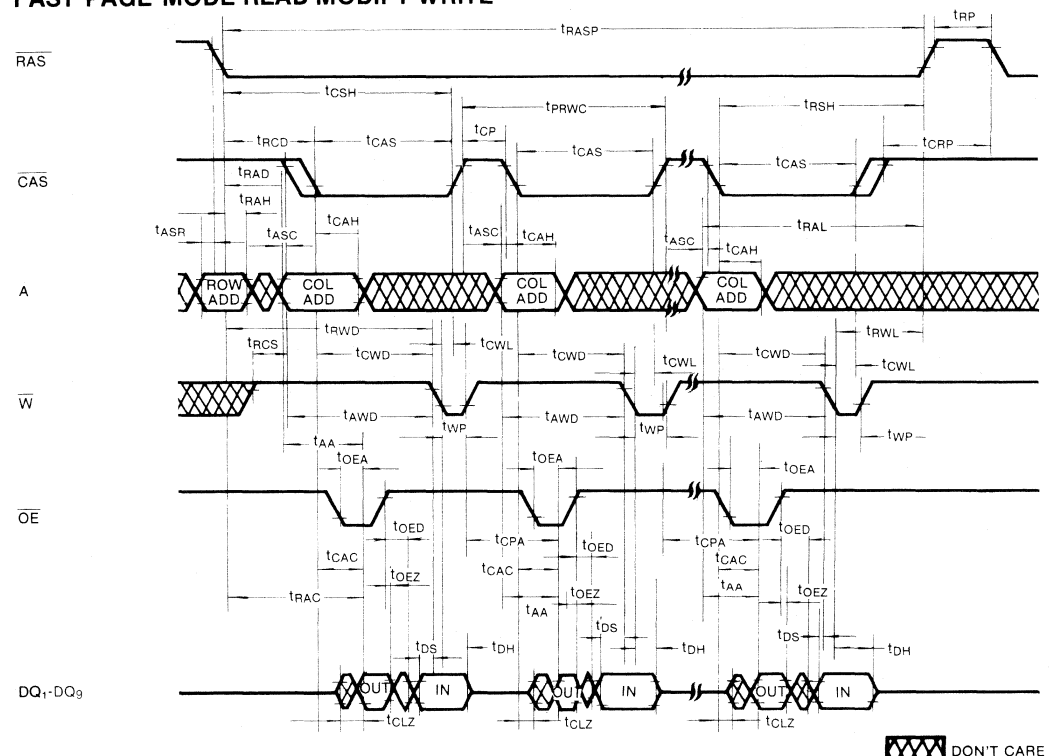
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



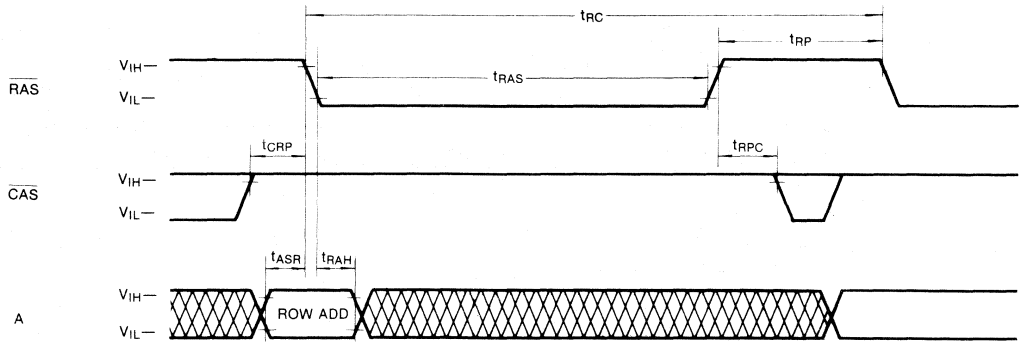
FAST PAGE MODE READ-MODIFY-WRITE



TIMING DIAGRAMS (Continued)

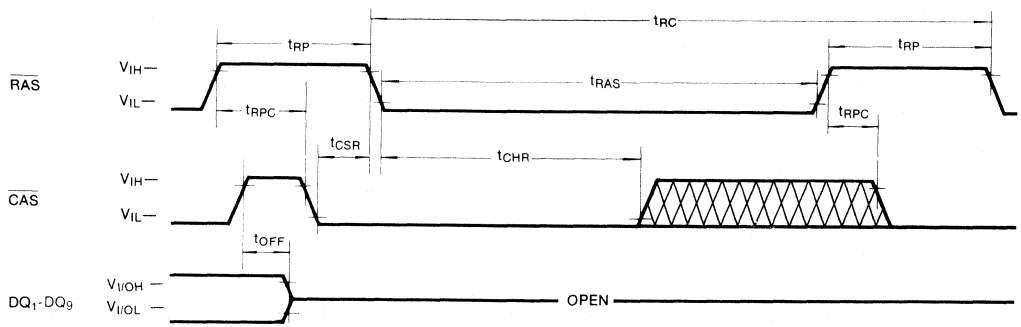
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



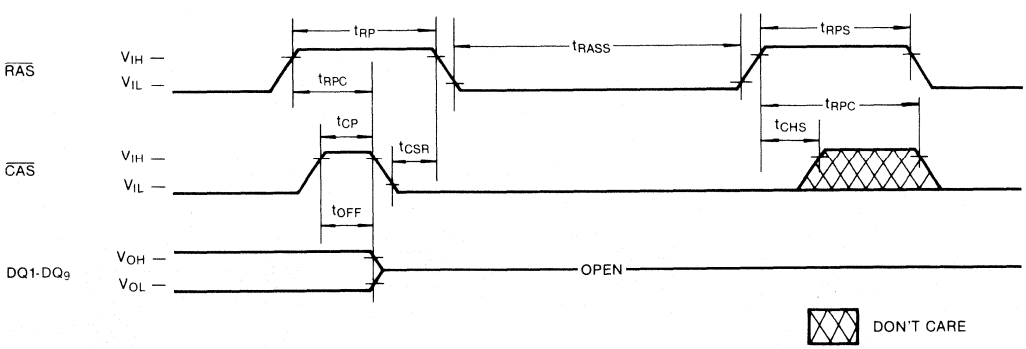
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care



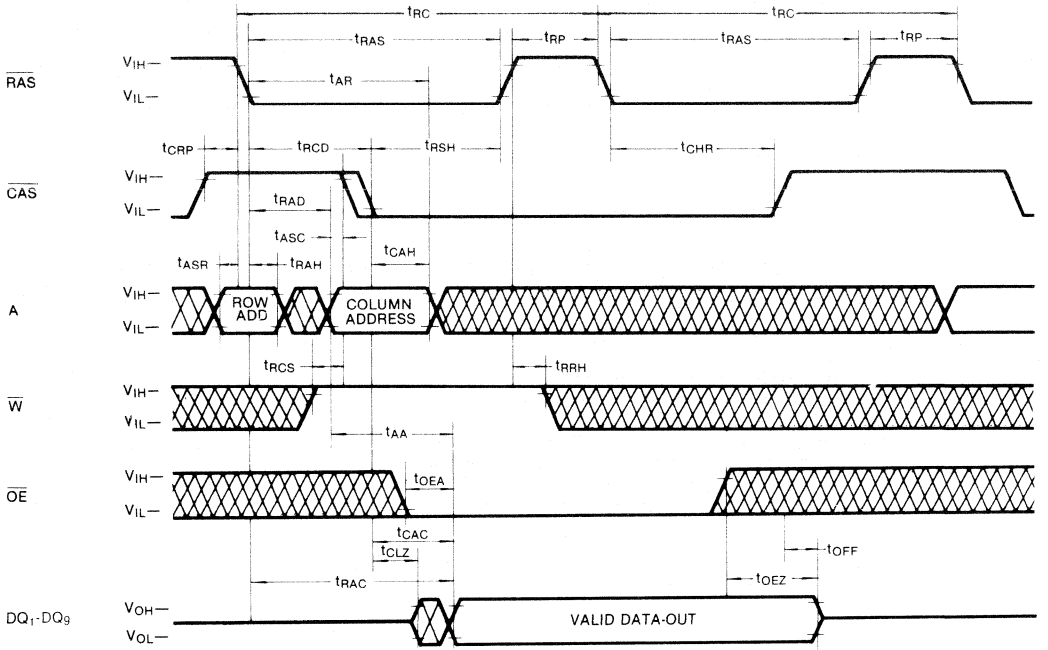
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care

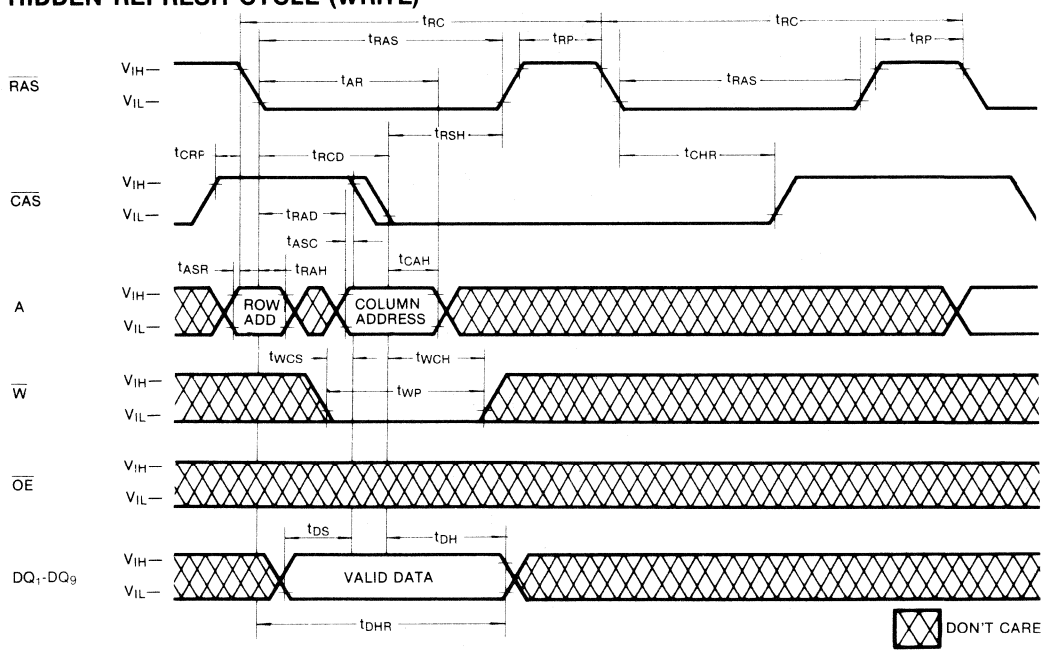


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

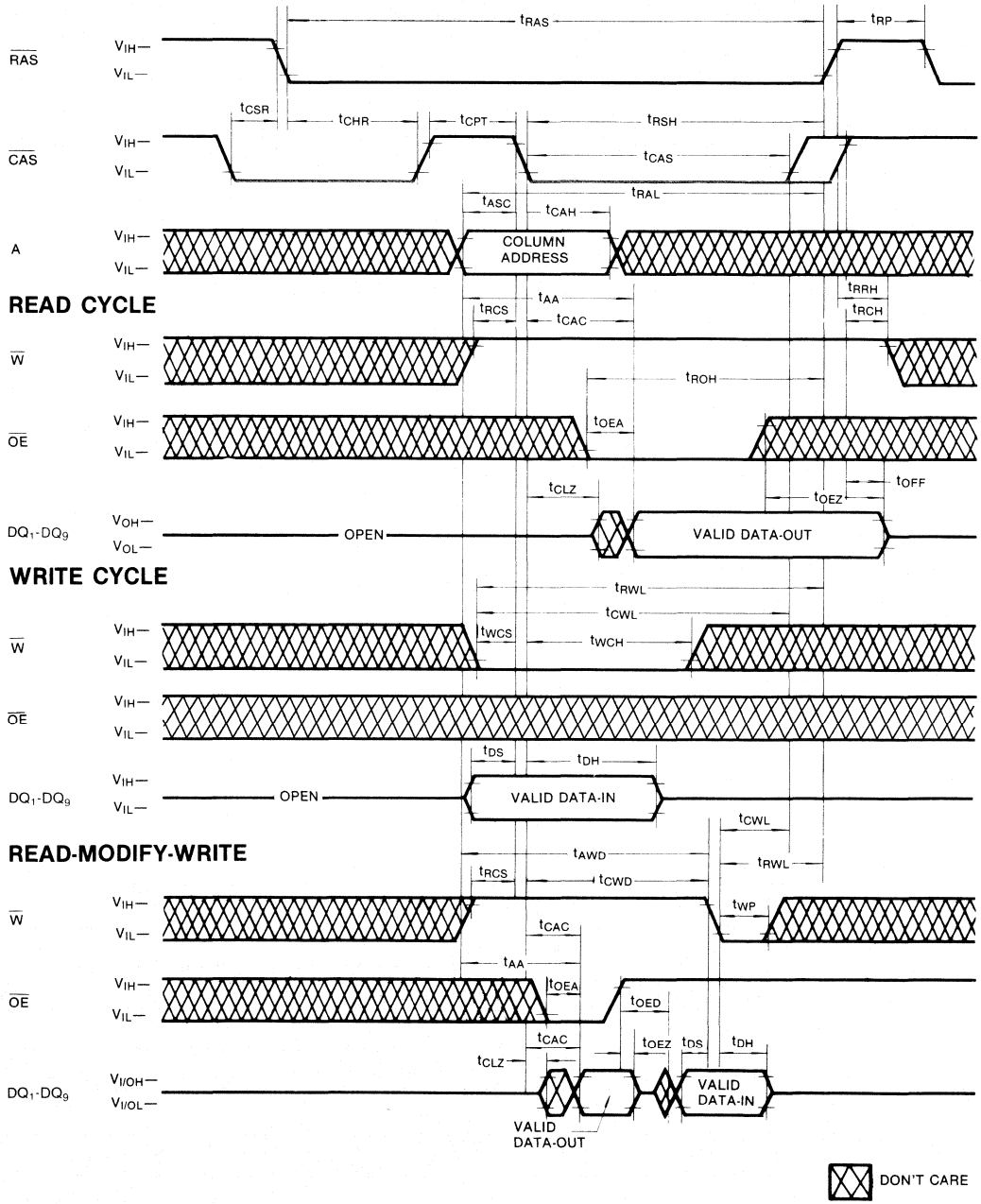


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM49C512LL contains 4,718,592 memory locations arranged in 9 groups of 524,288 × 1 bit each. Nineteen address bits are required to address a particular memory location. Since the KM49C512LL has only 10 address input pins, time multiplexed addressing is used to input 10 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM49C512LL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM49C512LL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM49C512LL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM49C512LL can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$, $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing W low before $\overline{CAS}$. The 9-bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cells. This cycle is achieved by bringing W low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The $\overline{OE}$ input must be low during the time defined by t_{OEA} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM49C512LL DQ pins.

Data Output

The KM49C512LL has a three-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}), the outputs are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs enter into the low impedance state in the time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM49C512LL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} times are not met)

DEVICE OPERATION (Continued)

Refresh

The data in the KM49C512LL is stored as a charge on microscopic capacitor within each memory cell. The stored charge tends to dissipate over time and will affect data integrity if the charge is not periodically refreshed. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 1024 row address (A0-A9).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM49C512LL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ transitions low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending either input active time and cycling $\overline{RAS}$. The hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Self Refresh: The self refresh is $\overline{CAS}$-before-$\overline{RAS}$ refresh to be used for long periods of standby, such as a battery back-up. In normal $\overline{CAS}$-before-$\overline{RAS}$ condition, when $\overline{RAS}$ is held low above 100μs an internal timer activates an refresh operation of consecutive row addresses in DRAM. The self refresh mode is exited when either $\overline{RAS}$ or $\overline{CAS}$ goes high(V_{IH}).

Other Refresh Methods: It is also possible to refresh the KM49C512LL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM49C512LL has Fast page mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is asserted high and then low again while $\overline{RAS}$ is asserted low, the read and write operations are enabled. In this method, the row address bits A0 through A9 are supplied by on chip refresh counter.

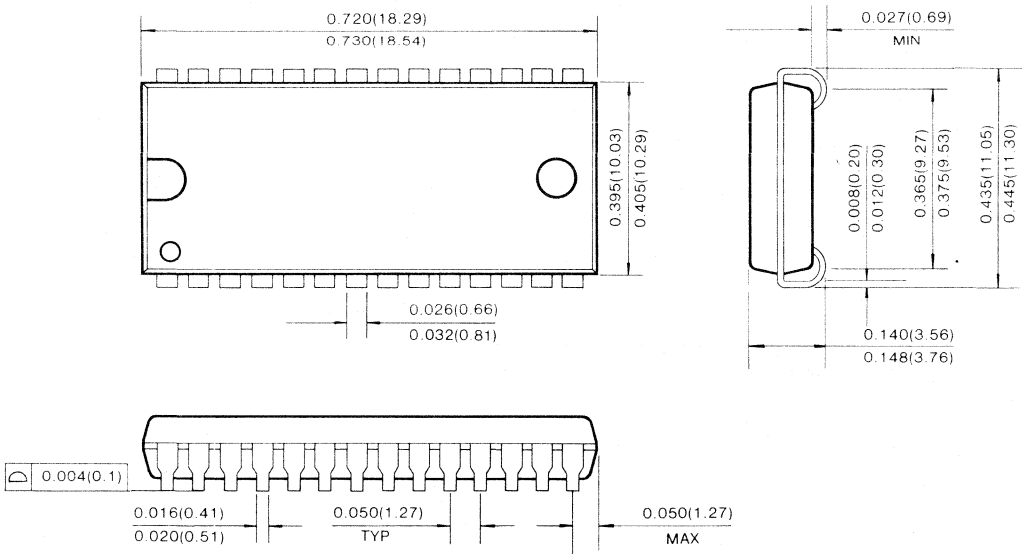
Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM49C512LL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held a valid V_{IH} in order to minimize the power-up current.

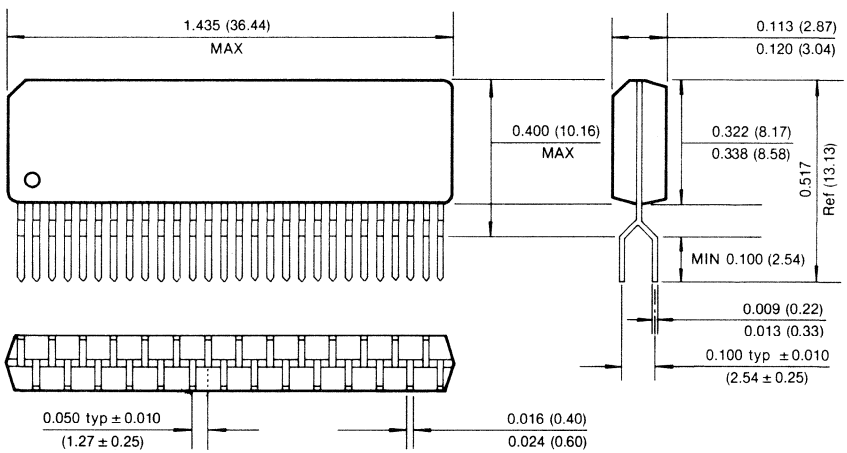
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)

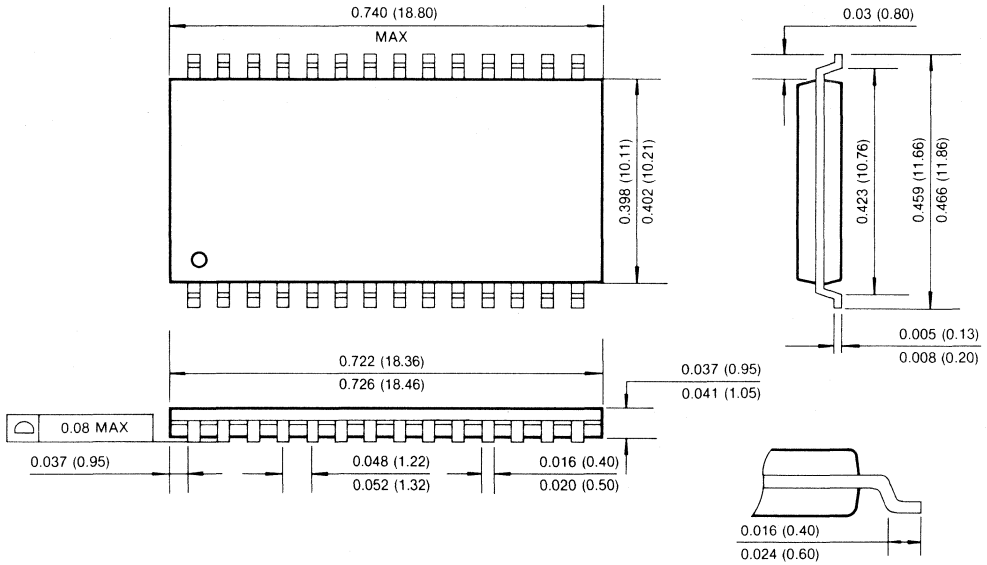


28-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

Units: Inches (millimeters)



256K x 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM416C256/L/SL-7	70ns	20ns	130ns
KM416C256/L/SL-8	80ns	20ns	150ns
KM416C256/L/SL-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Triple +5V±10% power supply**
- **Refresh Cycle**
  - **— 512 cycle/8ms (Normal)**
  - **— 512 cycle/64ms (L-version)**
  - **— 512 cycle/128ms (SL-version)**
- **Power Dissipation**
  - **— Standby: 11mW (Normal)**
    1.1mW (L-version)
    0.55mW (SL-version)
  - **— Active (70/80/100): 798/688/578mW**
- **JEDEC Standard pinout**
- **Available in Plastic SOJ and ZIP**

GENERAL DESCRIPTION

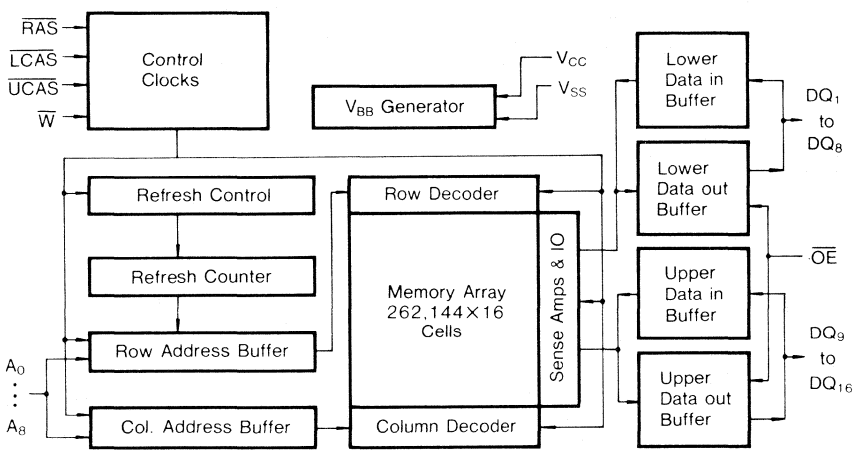
The Samsung KM416C256/L/SL is a CMOS high speed 262,144 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM416C256/L/SL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM416C256/L/SL is fabricated using Samsung's advanced CMOS process.

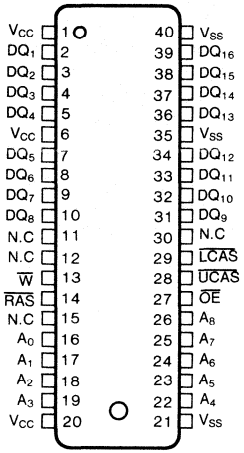
2

FUNCTIONAL BLOCK DIAGRAM



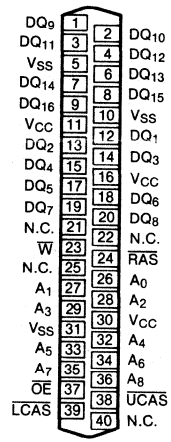
PIN CONFIGURATION (Top Views)

• KM416C256J/LJ/SLJ



(SOJ)

• KM416C256Z/LZ/SLZ



(ZIP)

Pin Name	Pin Function
A_0-A_8	Address Inputs
$DQ_{1\text{-}16}$	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe

Pin Name	Pin Function
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power (+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$, or $\overline{LCAS}$, Address Cycling @t_{RC} = min.)	KM416C256/L/SL-7	I_{CC1}	—	145	mA
	KM416C256/L/SL-8		—	125	mA
	KM416C256/L/SL-10		—	105	mA
Standby Current ($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$)		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$ = $\overline{LCAS}$, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM416C256/L/SL-7	I_{CC3}	—	145	mA
	KM416C256/L/SL-8		—	125	mA
	KM416C256/L/SL-10		—	105	mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{PC} = min.)	KM416C256/L/SL-7	I_{CC4}	—	90	mA
	KM416C256/L/SL-8		—	80	mA
	KM416C256/L/SL-10		—	70	mA
Standby Current ($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ ≥ V_{CC} − 0.2V)	KM416C256	I_{CC5}	—	1	mA
	KM416C256L		—	200	μA
	KM416C256SL		—	100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @t_{RC} = min.)	KM416C256/L/SL-7	I_{CC6}	—	145	mA
	KM416C256/L/SL-8		—	125	mA
	KM416C256/L/SL-10		—	105	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode Input High Voltage (V_{IH}) = V_{CC}-0.2V Input Low Voltage (V_{IL}) = 0.2V $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V D_{IN} = Don't Care T_{RC}=125μS(L-ver), T_{RC}=250μS(SL-ver), T_{RAS}= T_{RAS}min. ~ 1μS.	KM416C256L	I_{CC7}	—	300	μA
	KM416C256SL		—	150	μA
Input Leakage Current (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$ = V_{IL}. In I_{CC4}, Address can be changed maximum once while $\overline{UCAS}$ and $\overline{UCAS}$ = V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_8)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN3}	—	7	pF
Output Capacitance (DQ_1-DQ_{16})	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1, 2)

Parameter	Symbol	KM416C256/L/SL-7		KM416C256/L/SL-8		KM416C256/L/SL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	180		200		240		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	55	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command set-up time	t_{WCS}	0		0		0		ns	8
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	

AC CHARACTERISTICS (Continued)

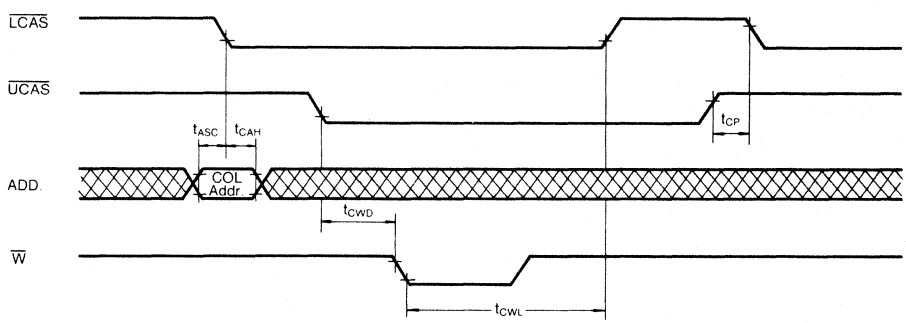
Parameter	Symbol	KM416C256/L/SL-7		KM416C256/L/SL-8		KM416C256/L/SL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold time referenced to RAS	t_{DHR}	55		60		75		ns	6
Refresh period (512 cycles)	t_{REF}		8		8		8	ms	
Refresh period (L-version)	t_{REF}		64		64		64	ms	
Refresh period (SL-version)	t_{REF}		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	45		45		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	95		105		130		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	60		65		75		ns	8
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3
Fast page mode cycle time	t_{PC}	45		50		55		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	95		100		115		ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
Access time from $\overline{OE}$	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data-in delay time	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

KM416C256 Truth Table

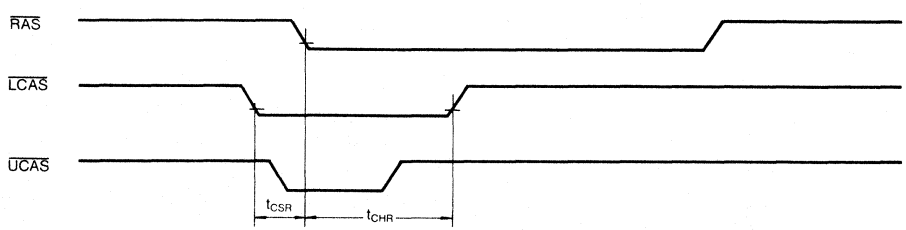
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	$DQ_{1\sim8}$	$DQ_{9\sim16}$	State
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Lower Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-In	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	—

NOTES

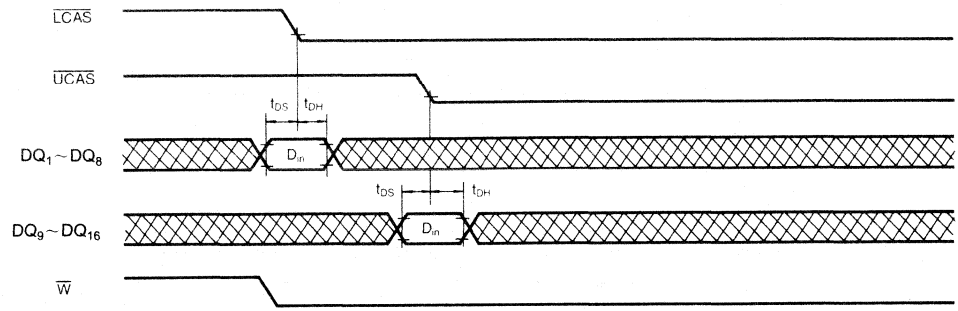
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating aprameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
17. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.

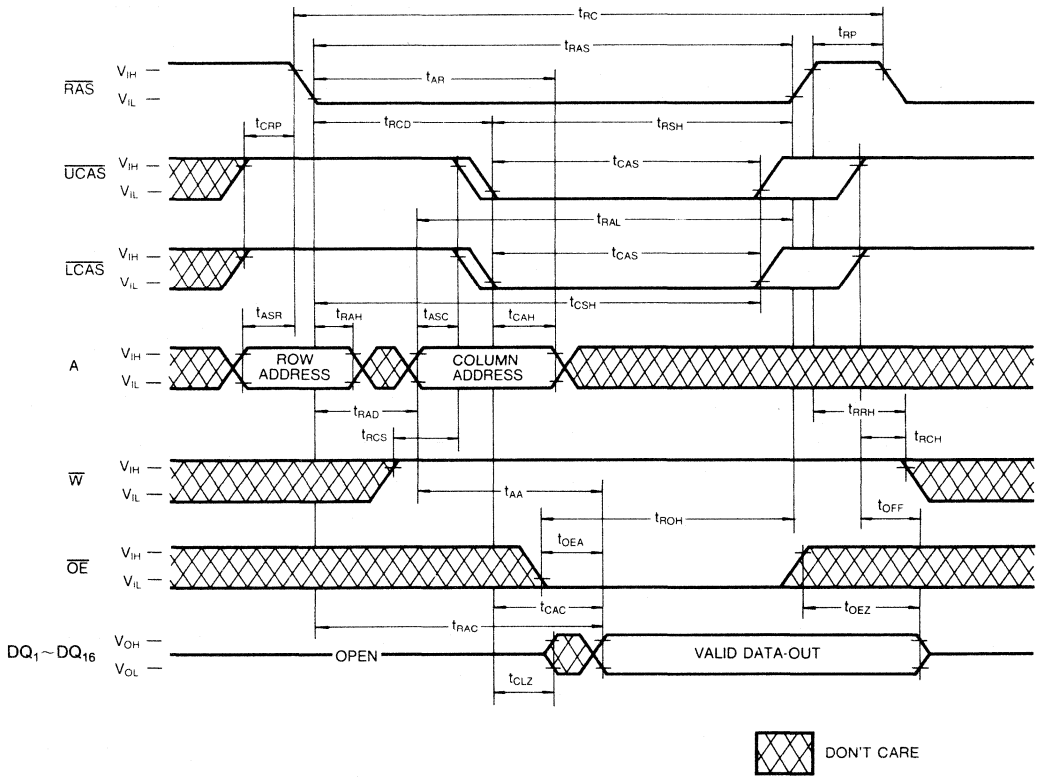


18. t_{DS}, t_{DH} is independetly specified for lower byte $D_{in(1\sim9)}$, upper byte $D_{in(10\sim18)}$.



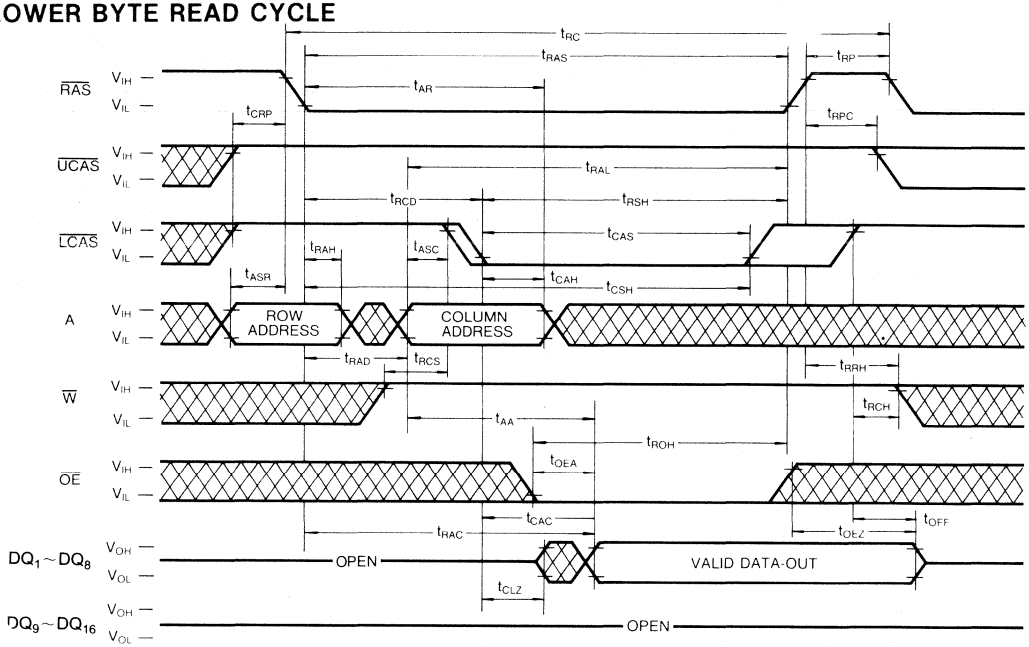
TIMING DIAGRAMS

WORD READ CYCLE

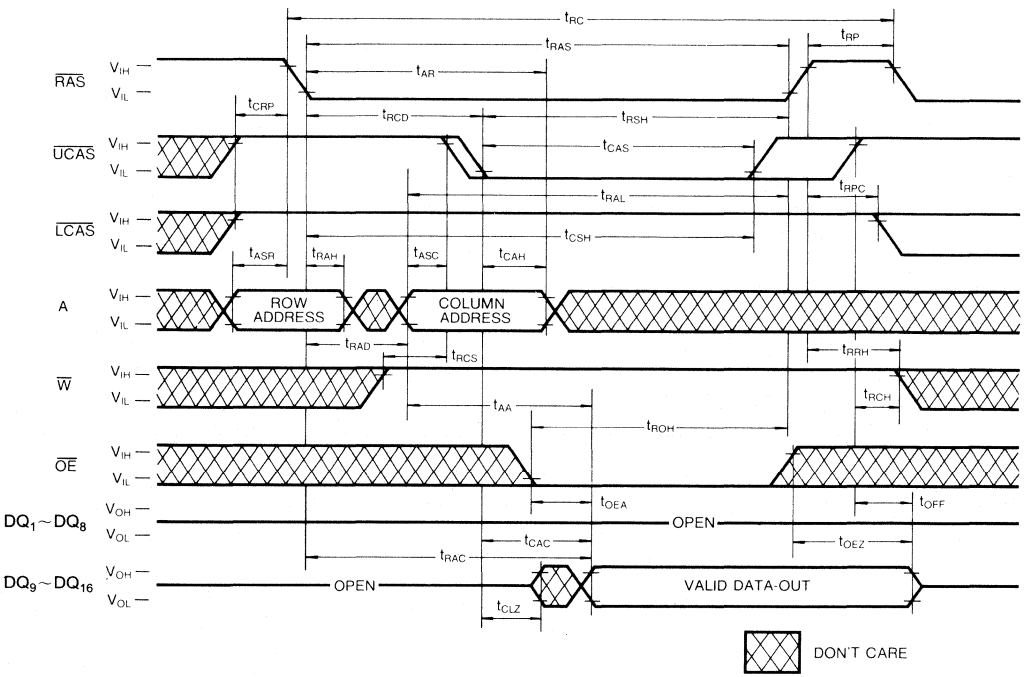


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE

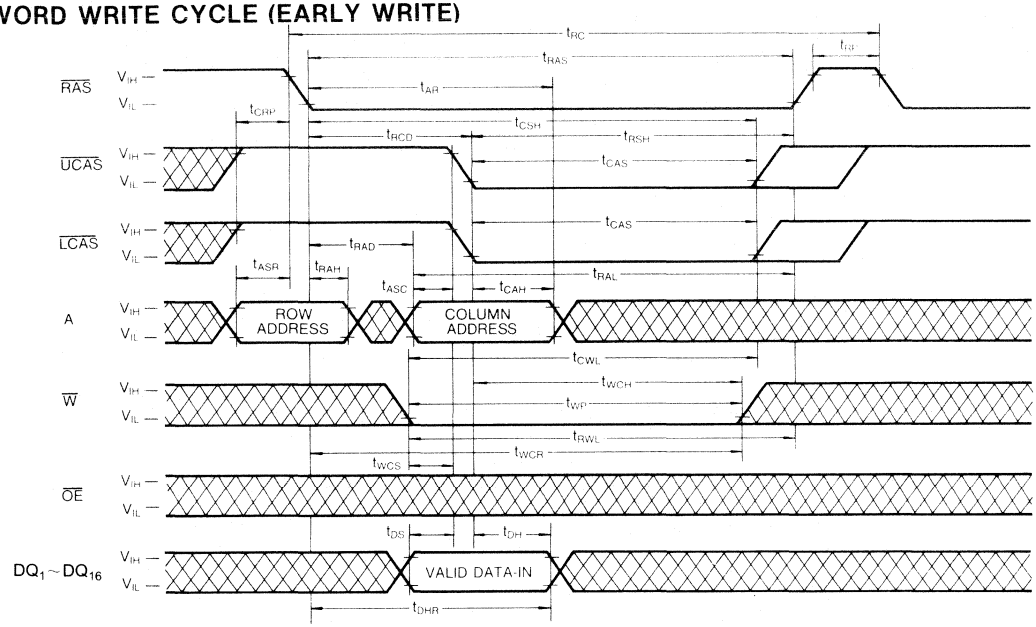


UPPER BYTE READ CYCLE

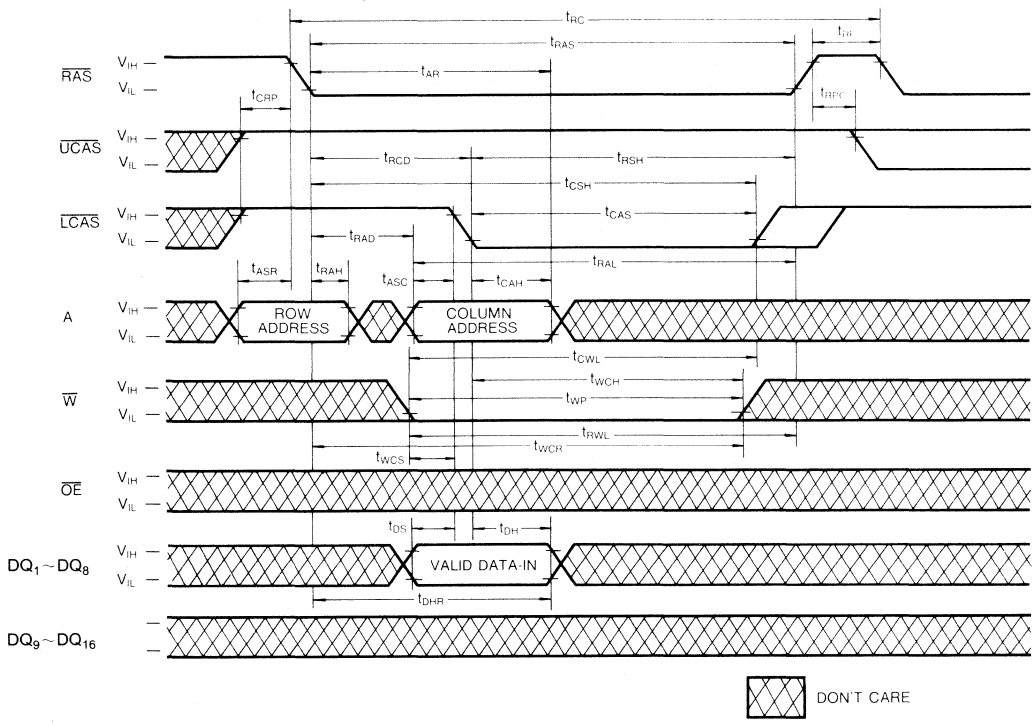


TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)

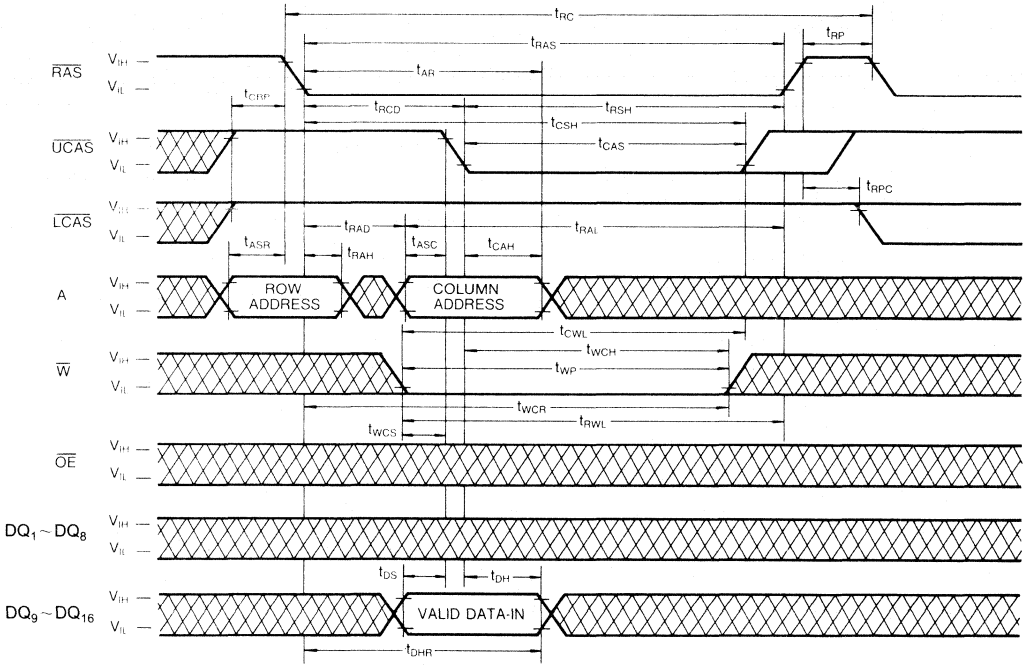


LOWER BYTE WRITE CYCLE (EARLY WRITE)

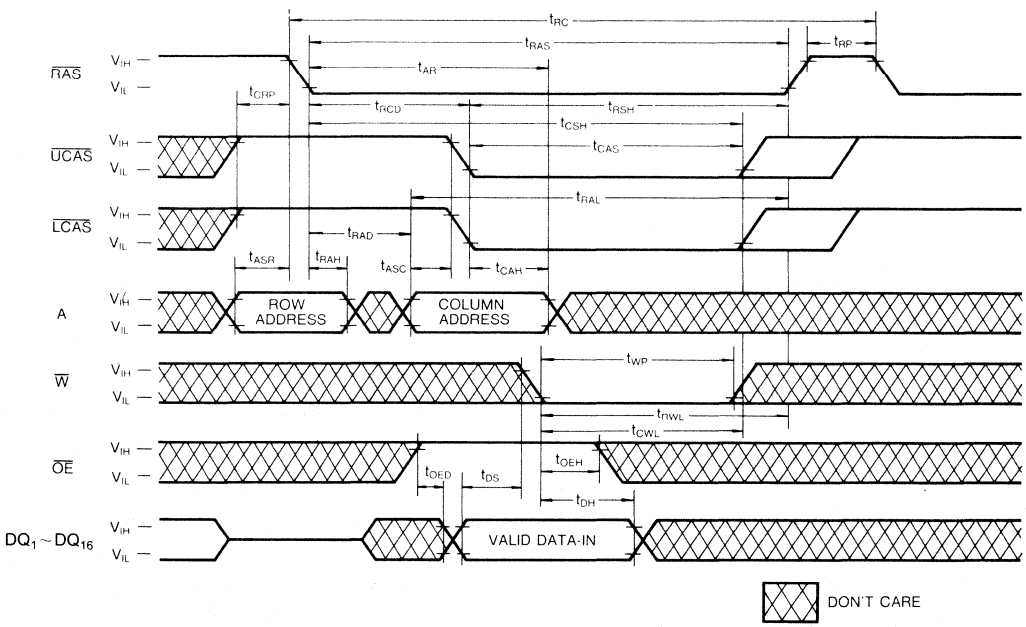


TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)

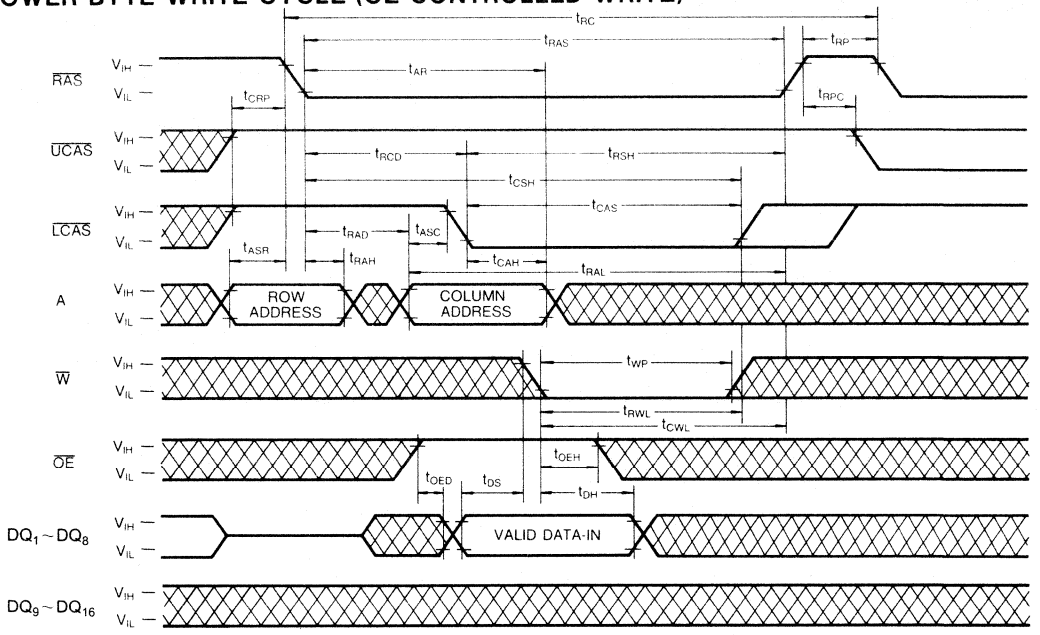


WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

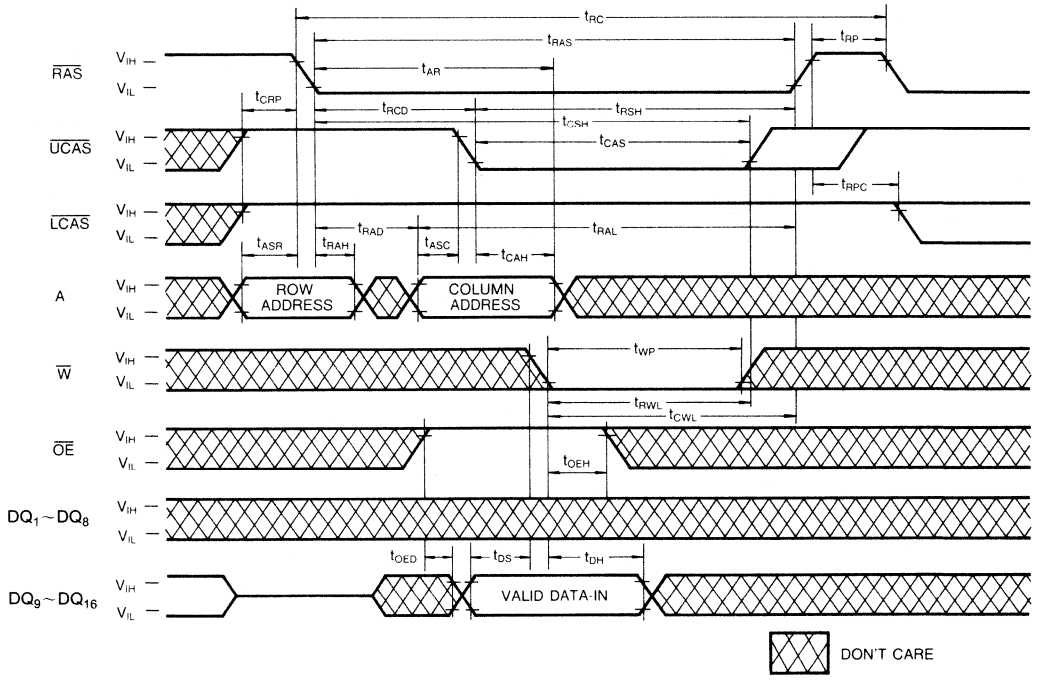


TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

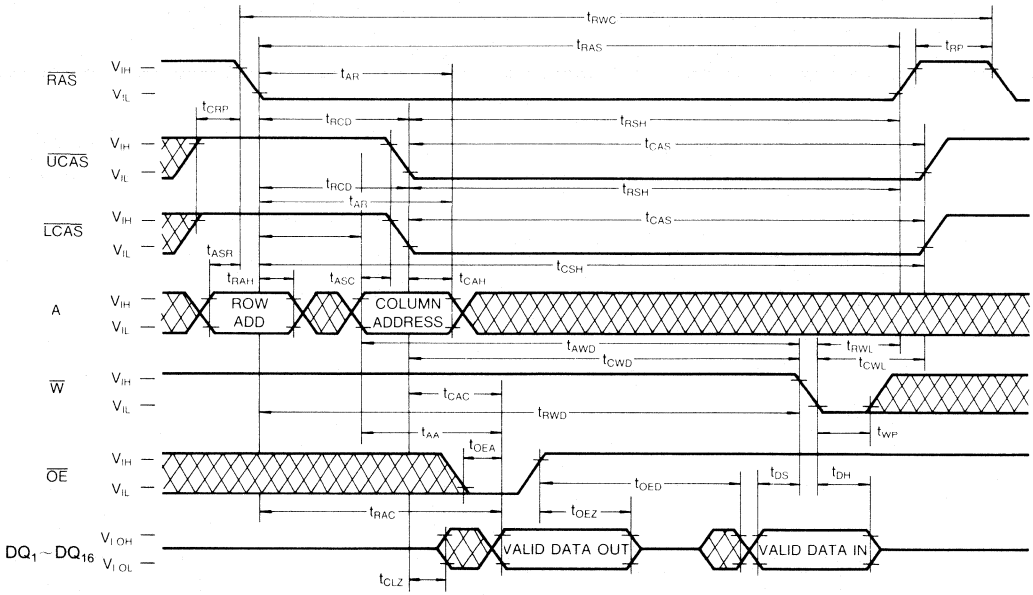


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

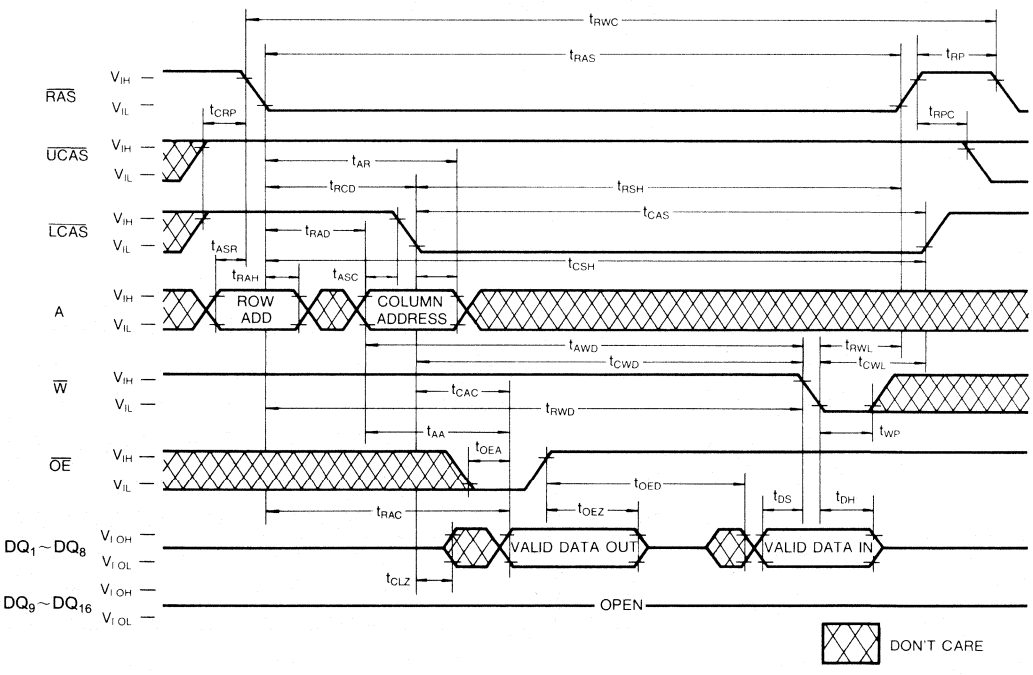


TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE

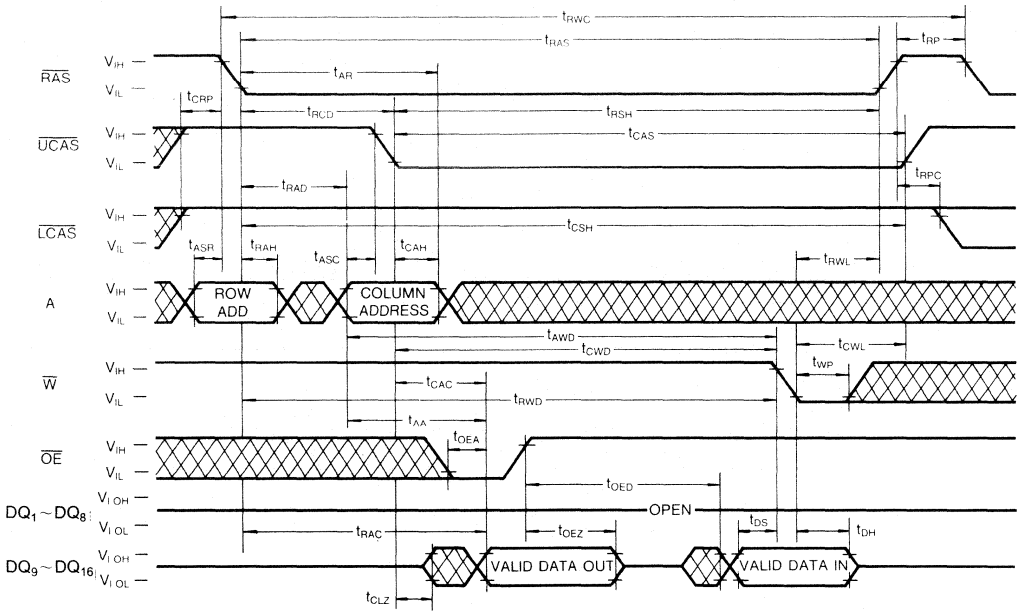


LOWER-BYTE READ-MODIFY-WRITE CYCLE

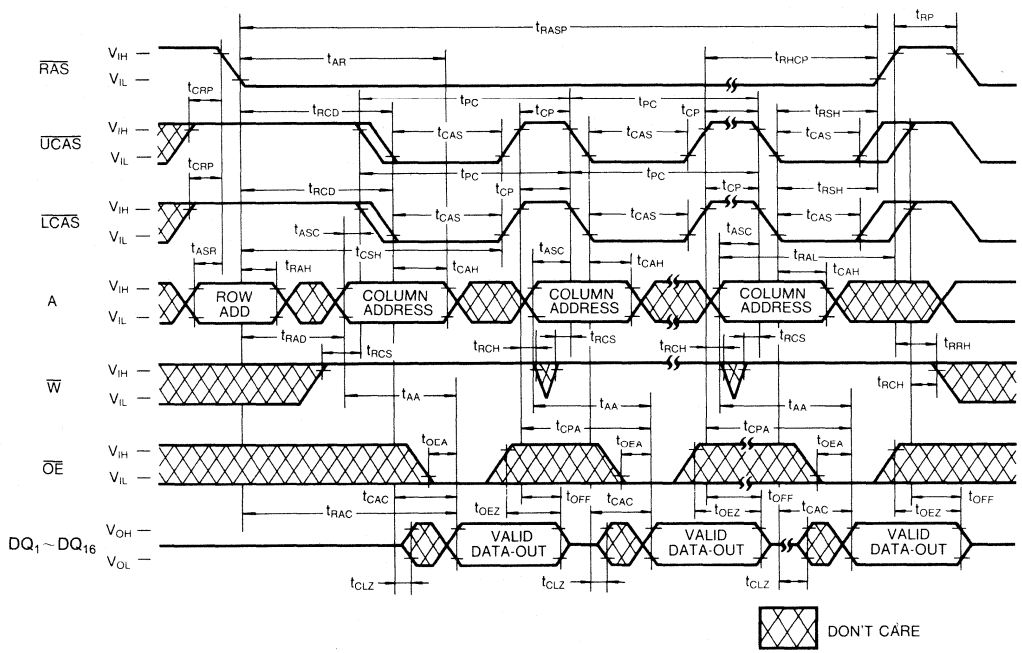


TIMING DIAGRAMS (Continued)

UPPER-BYTE READ-MODIFY-WRITE CYCLE

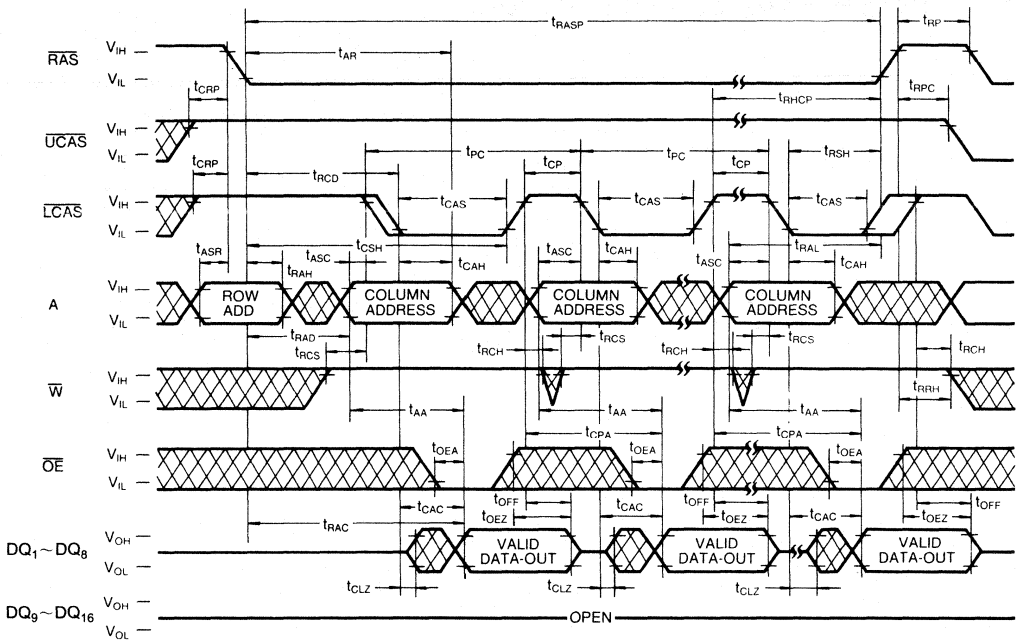


FAST PAGE MODE WORD READ CYCLE

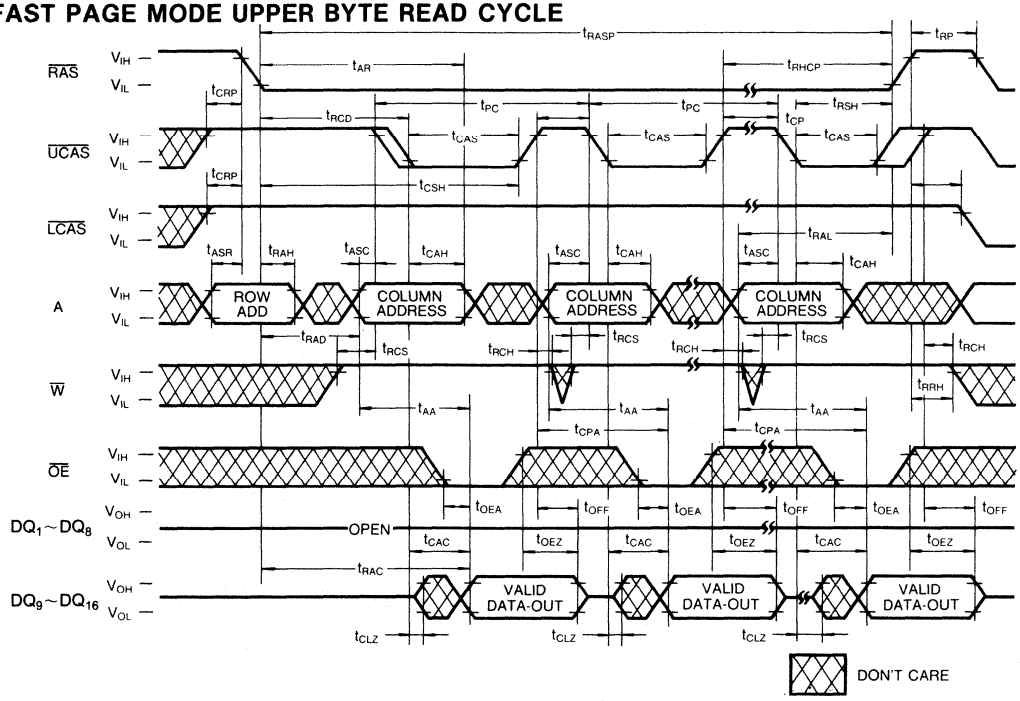


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE

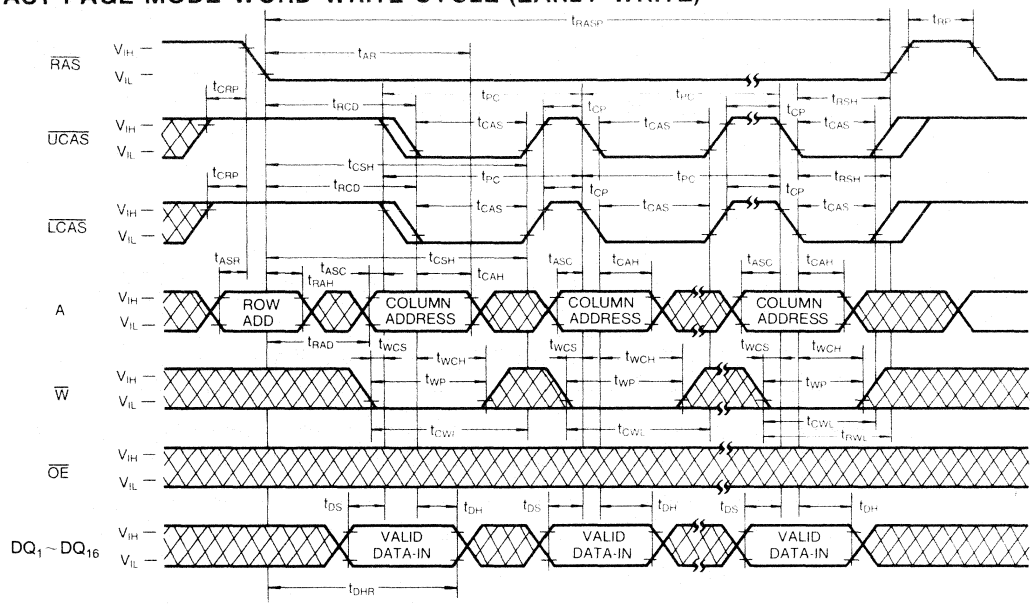


FAST PAGE MODE UPPER BYTE READ CYCLE

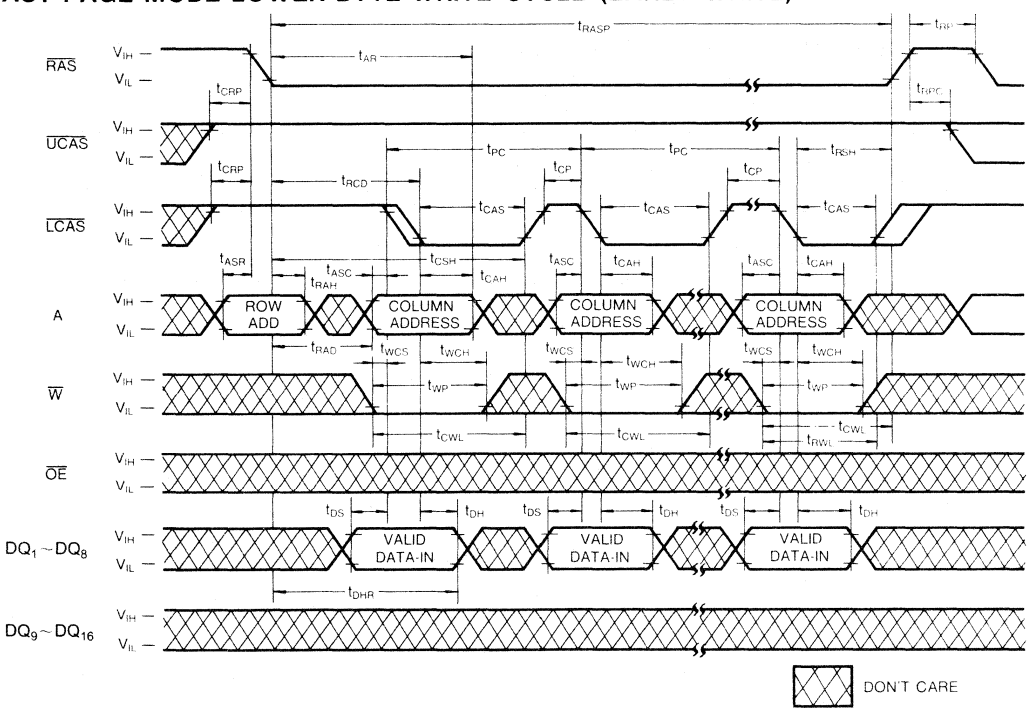


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

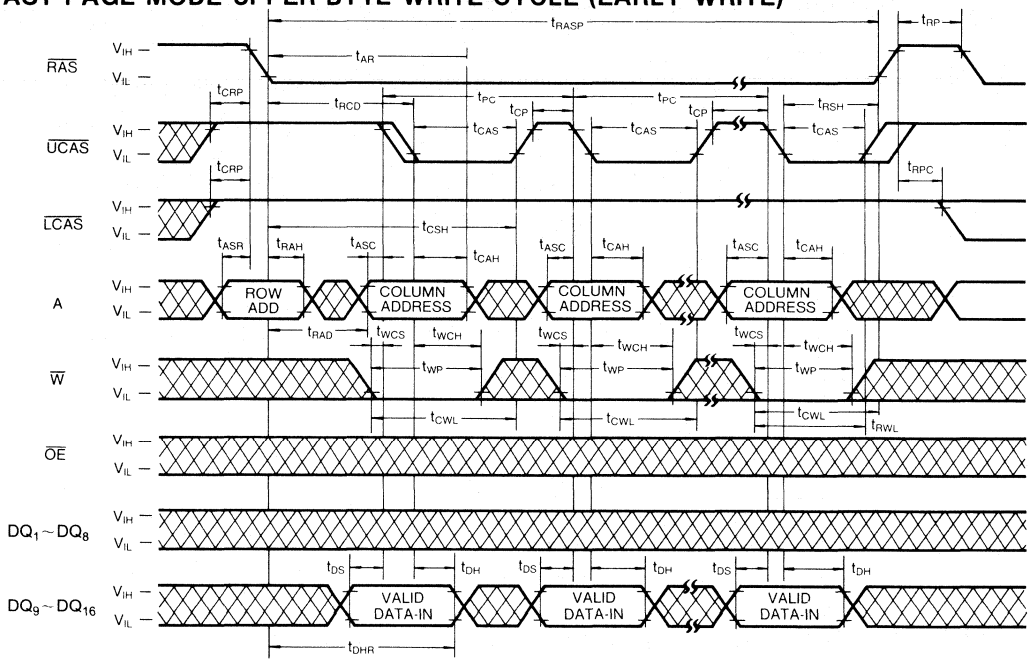


FAST PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

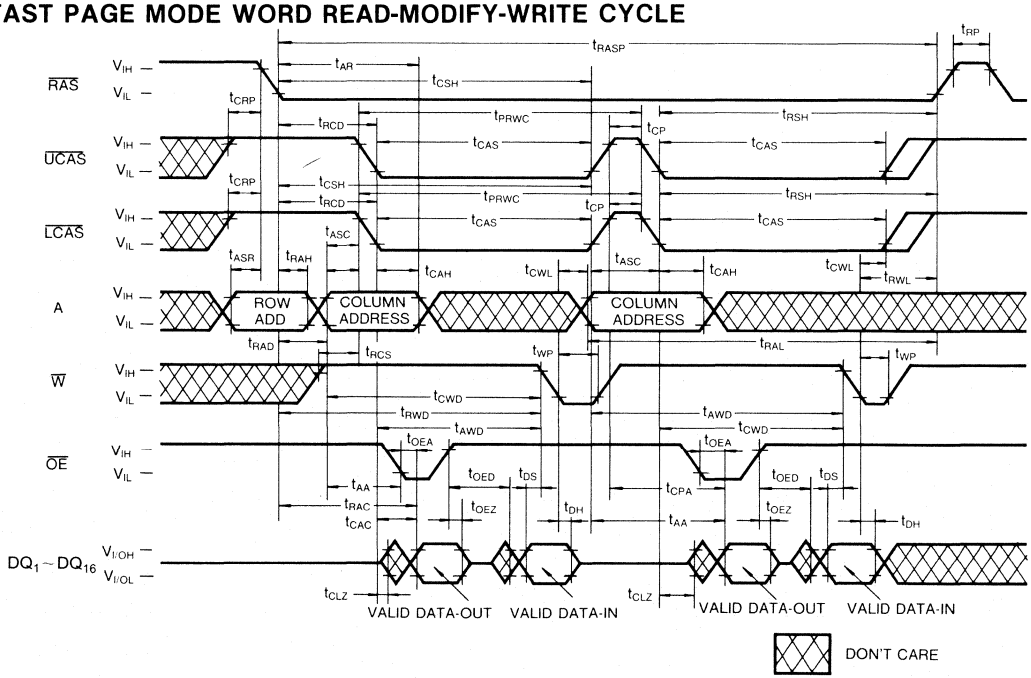


TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

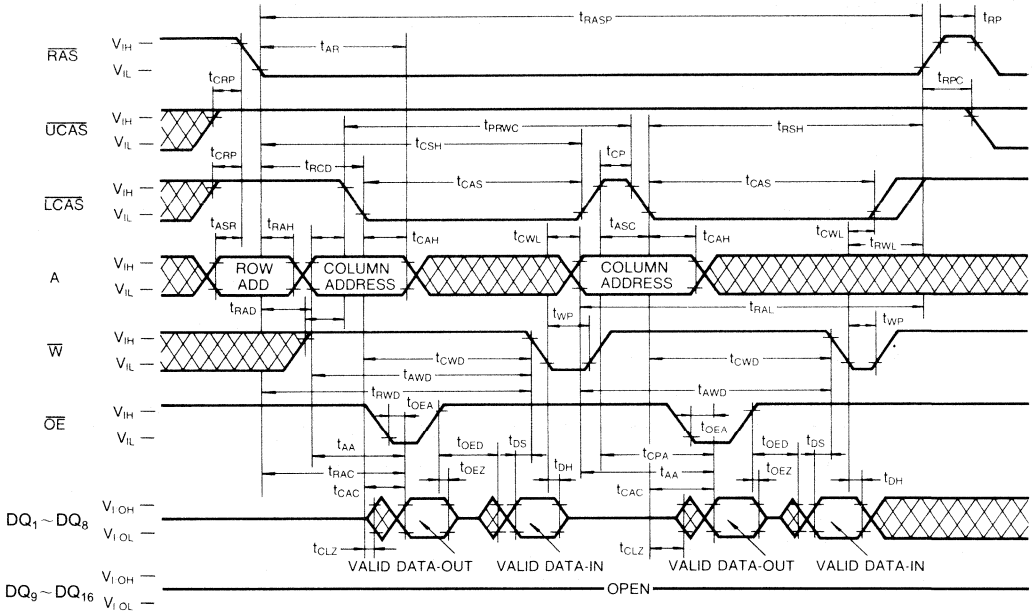


FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE

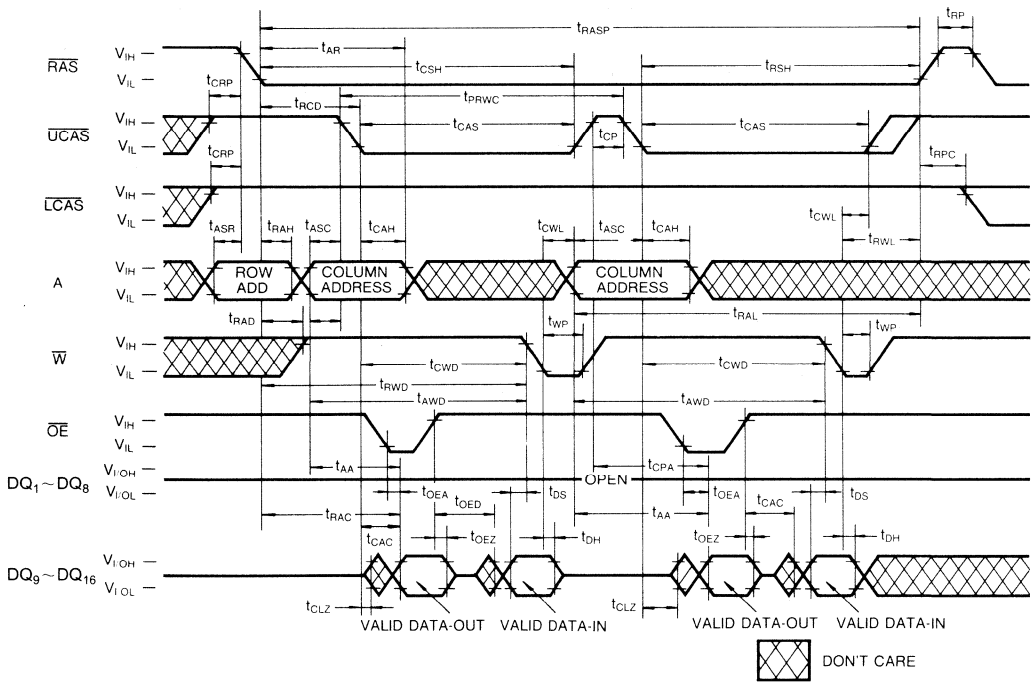


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE



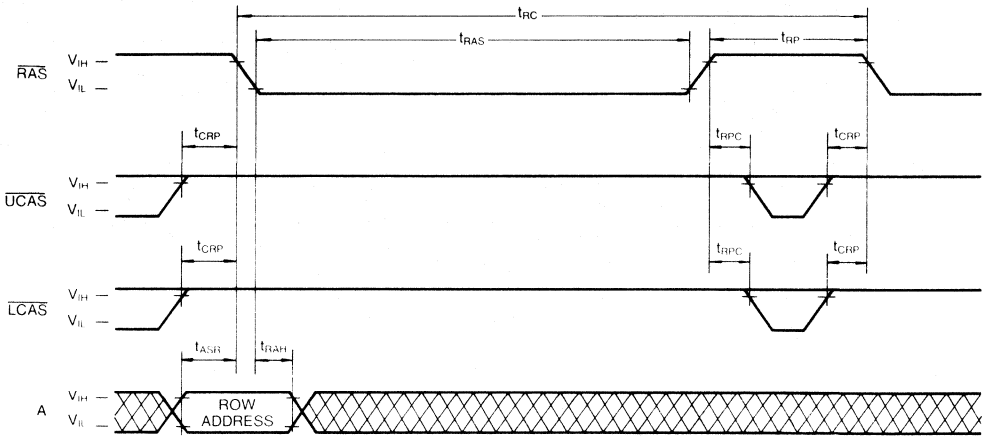
FAST PAGE MODE UPPER-BYTE- READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

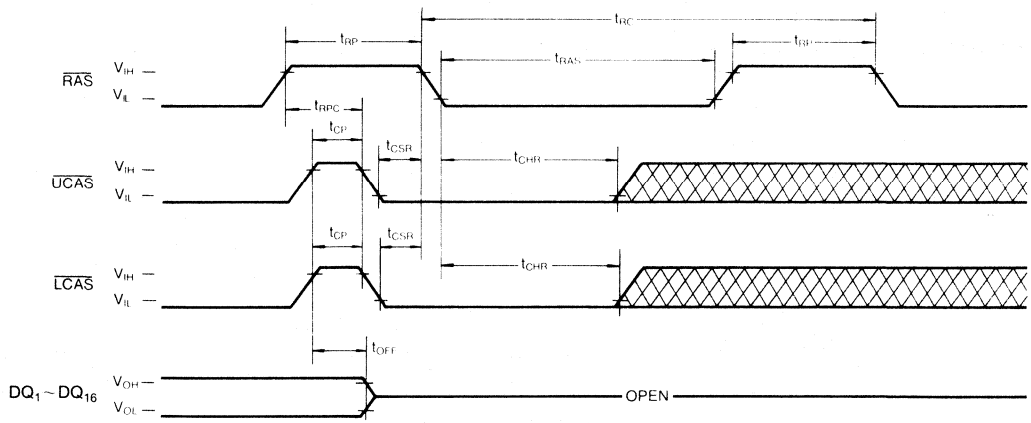
$\overline{RAS}$ ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$=Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

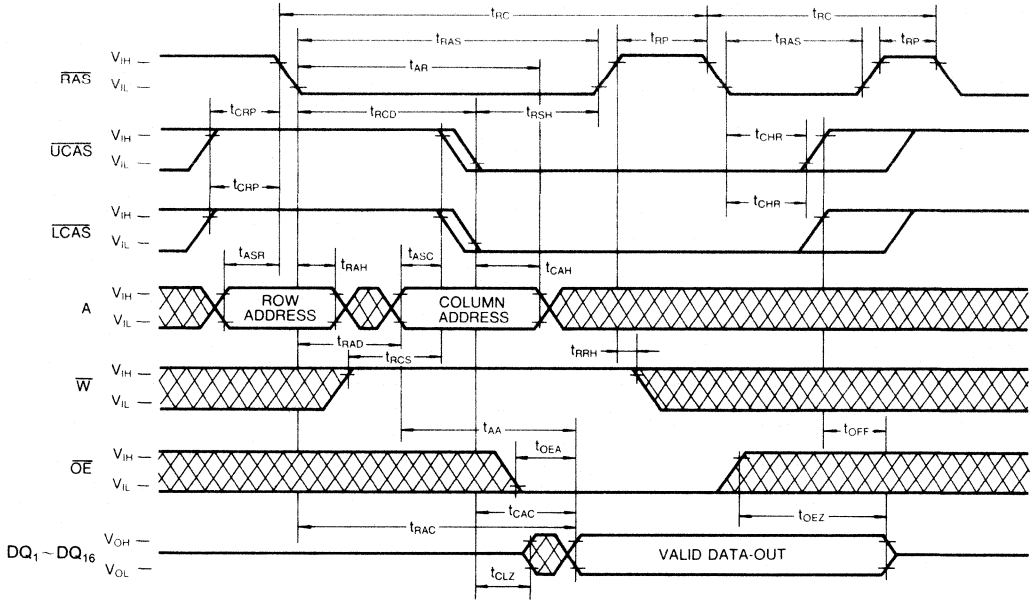
NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care



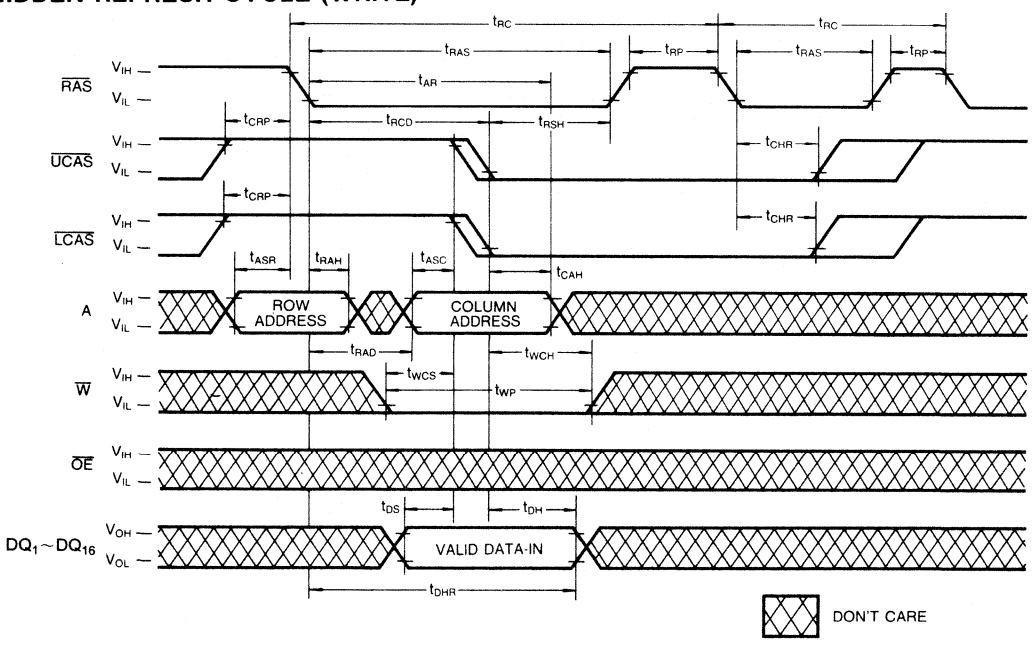
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

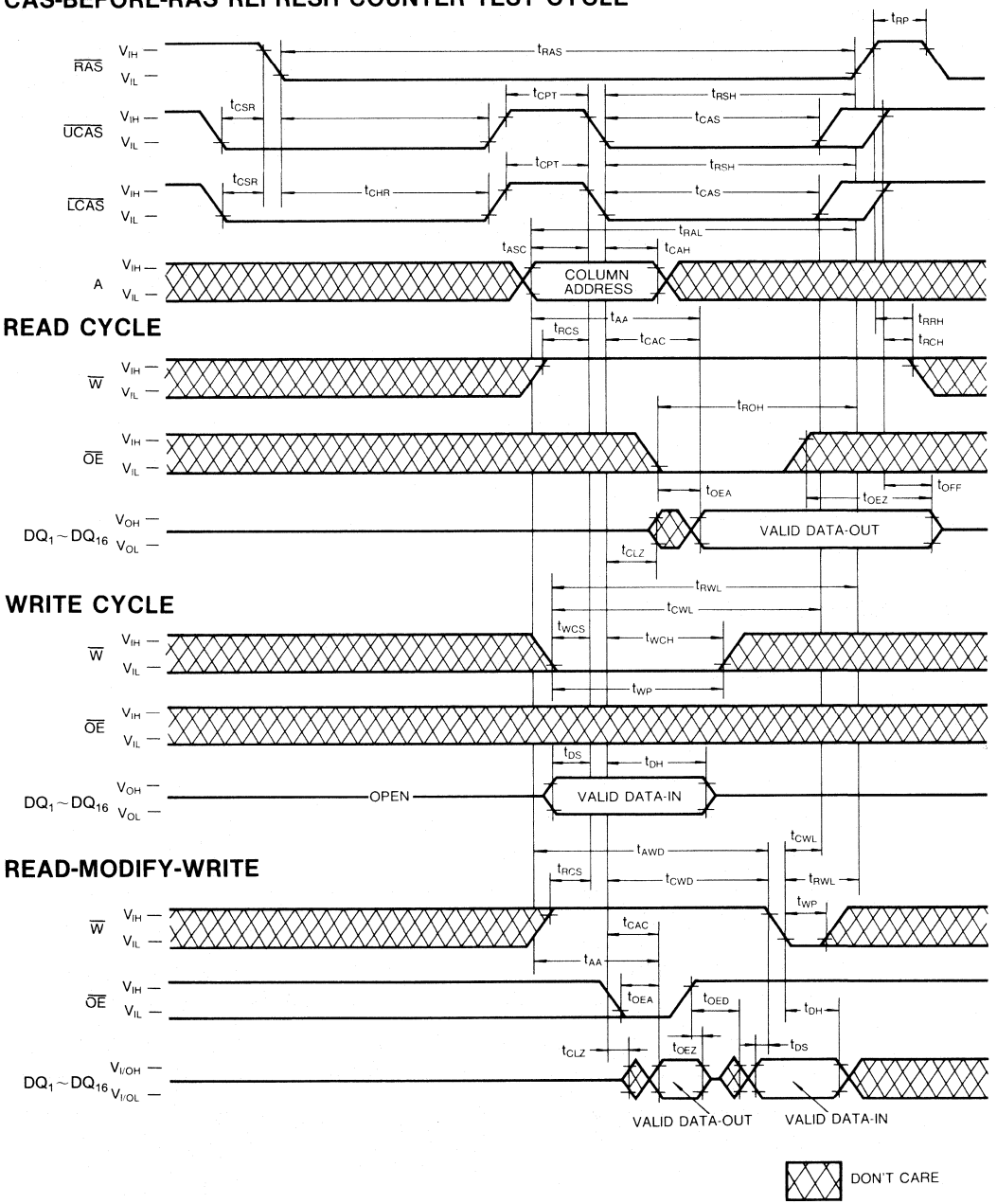


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM416C256/L/SL contains 4,194,304 memory locations arranged in 16 groups of 262,144 x 1 bit each. Eighteen address bits are required to address a particular memory location. Since the KM416C256/L/SL has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{LCAS}$, $\overline{UCAS}$) and the valid row and column address inputs.

Operation of the KM416C256/L/SL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{LCAS}$ ($\overline{UCAS}$) remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{LCAS}$ ($\overline{UCAS}$). This is the beginning of any KM416C256/L/SL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{LCAS}$ ($\overline{UCAS}$) have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM416C256/L/SL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/x$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If x$\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if x$\overline{CAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM416C256/L/SL can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$, $\overline{LCAS}$ and $\overline{UCAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or x$\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before x$\overline{CAS}$. The 8-bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the OE input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cells. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The $\overline{OE}$ input must be low during the time defined by t_{OEA} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM416C256/L/SL DQ pins.

Data Output

The KM416C256/L/SL has a three-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}), the outputs are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs enter into the low impedance state in the time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM416C256/L/SL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} times are not met)

DEVICE OPERATION (Continued)

Refresh

The data in the KM416C256/L/SL is stored as a charge on microscopic capacitor within each memory cell. The stored charge tends to dissipate over time and will affect data integrity if the charge is not periodically refreshed. Refresh of the individual storage cells is accomplished by accessing all rows within the refresh period (t_{REF}) off within 8ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row address (A0-A8).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM416C256/L/SL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If either $\overline{LCAS}$ or $\overline{UCAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ transitions low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending either $\overline{LCAS}$ or $\overline{UCAS}$ input active time and cycling $\overline{RAS}$. The hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM416C256/L/SL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM416C256/L/SL has Fast page mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is asserted high and then low again while $\overline{RAS}$ is asserted low, the read and write operations are enabled. In this method, the row address bits A0 through A8 are supplied by on chip refresh counter.

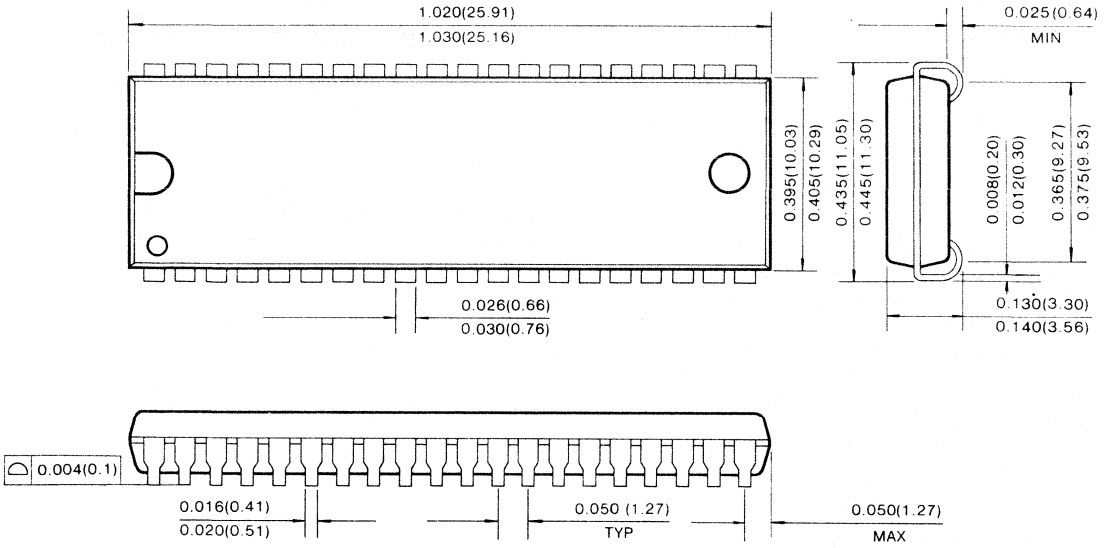
Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM416C256/L/SL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held a valid V_{IH} in order to minimize the power-up current.

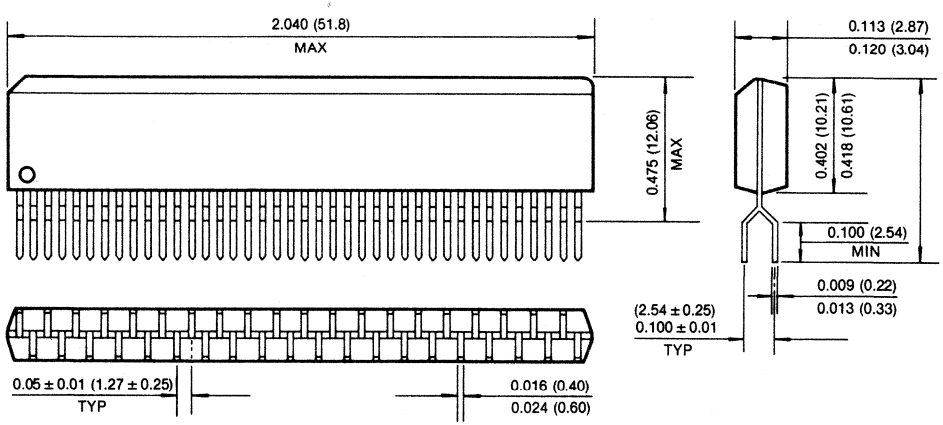
PACKAGE DIMENSION

40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



40-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



256K x 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM416C256LL-7	70ns	20ns	130ns
KM416C256LL-8	80ns	20ns	150ns
KM416C256LL-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Self refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Triple +5V±10% power supply**
- **Refresh Cycle**
  - **— 512 cycle/128ms (self-refresh)**
- **Power Dissipation**
  - **— Standby: 11mW (Normal)**
    0.55mW (self-refresh)
  - **— Active (70/80/100): 798/688/578mW**
- **JEDEC Standard pinout**
- **Available in Plastic SOJ and ZIP**

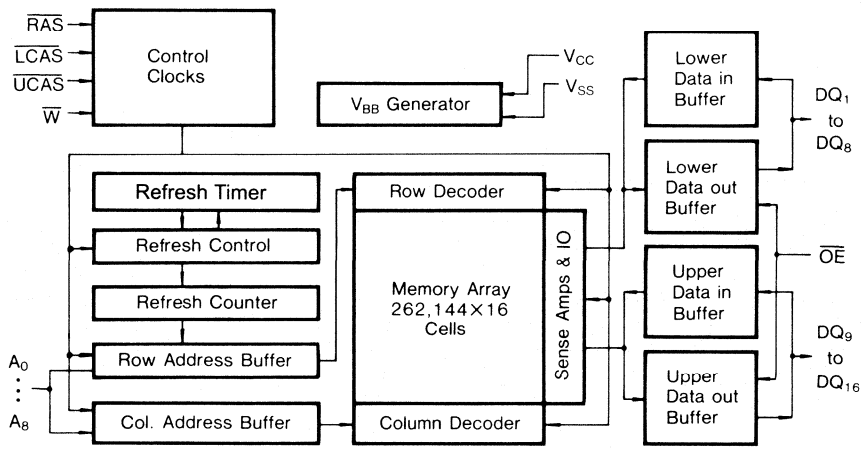
GENERAL DESCRIPTION

The Samsung KM416C256LL is a CMOS high speed 262,144 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM416C256LL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

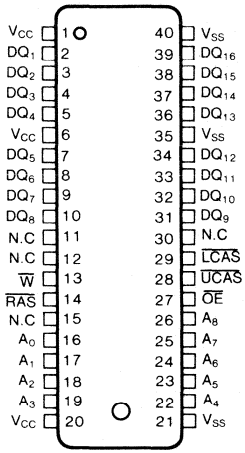
The KM416C256LL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



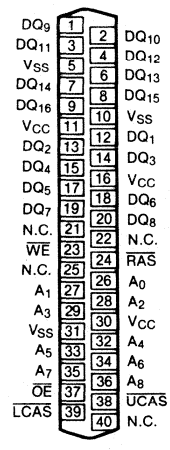
PIN CONFIGURATION (Top Views)

• **KM416C256LLJ**



(SOJ)

• **KM416C256LLZ**



(ZIP)

Pin Name	Pin Function
A_0-A_8	Address Inputs
$DQ_{1\text{-}16}$	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe

Pin Name	Pin Function
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power (+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$, or $\overline{LCAS}$, Address Cycling @t_{RC} = min.)	KM416C256LL-7	I_{CC1}	—	145	mA
	KM416C256LL-8		—	125	mA
	KM416C256LL-10		—	105	mA
Standby Current ($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$)		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$ = $\overline{LCAS}$, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM416C256LL-7	I_{CC3}	—	145	mA
	KM416C256LL-8		—	125	mA
	KM416C256LL-10		—	105	mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{PC} = min.)	KM416C256LL-7	I_{CC4}	—	90	mA
	KM416C256LL-8		—	80	mA
	KM416C256LL-10		—	70	mA
Standby Current ($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ ≥ V_{CC} − 0.2V)		I_{CC5}	—	100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @t_{RC} = min.)	KM416C256LL-7	I_{CC6}	—	145	mA
	KM416C256LL-8		—	125	mA
	KM416C256LL-10		—	105	mA
Self Refresh Current $\overline{RAS}$ = $\overline{CAS}$ = V_{IL} $\overline{WE}$ = $\overline{OE}$ = A0 ~ A8 = V_{CC}-0.2V or 0.2V DQ1 ~ 16 = V_{CC}-0.2V, 0.2V or OPEN		I_{CC5}	—	200	μA
Input Leakage Current (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$ = V_{IL}. In I_{CC4}, Address can be changed maximum once while $\overline{UCAS}$ and $\overline{UCAS}$ = V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_8)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_{16})	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1, 2)

Parameter	Symbol	KM416C256LL-7		KM416C256LL-8		KM416C256LL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	180		200		240		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	55	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command set-up time	t_{WCS}	0		0		0		ns	8
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	

AC CHARACTERISTICS (Continued)

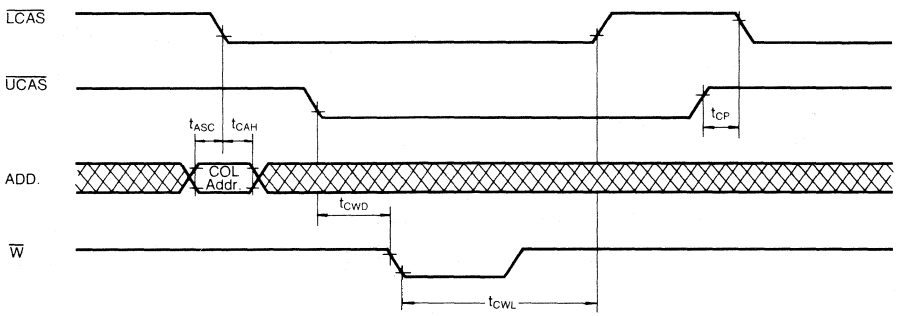
Parameter	Symbol	KM416C256LL-7		KM416C256LL-8		KM416C256LL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (self-version)	t_{REF}		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	45		45		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	95		105		130		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	60		65		75		ns	8
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3
Fast page mode cycle time	t_{PC}	45		50		55		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	95		100		115		ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
Access time from $\overline{OE}$	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data-in delay time	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RASS}	100		100		100		μs	
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RPS}	130		150		180		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{CHS}	0		0		0		ns	

KM418C256 Truth Table

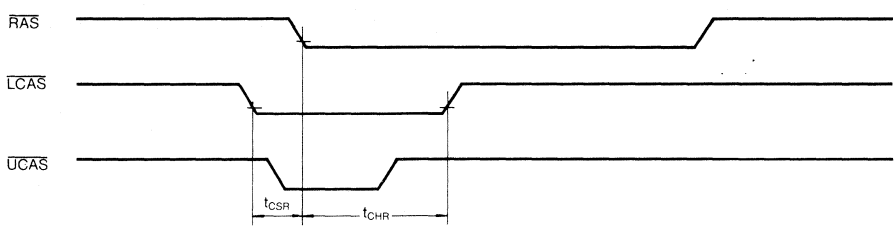
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	$DQ_{1\sim9}$	$DQ_{10\sim18}$	State
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Lower Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-In	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	—

NOTES

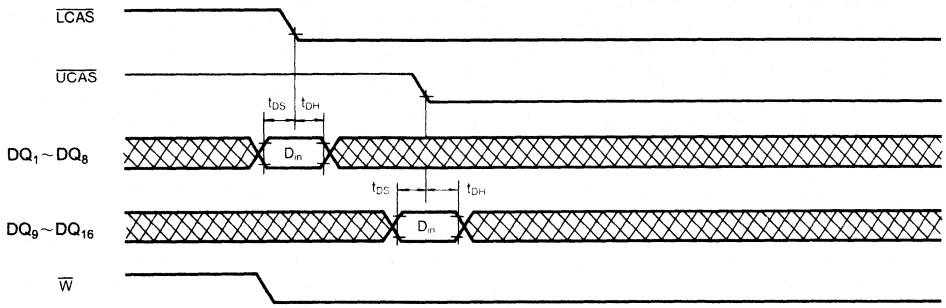
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating aprameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
17. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.

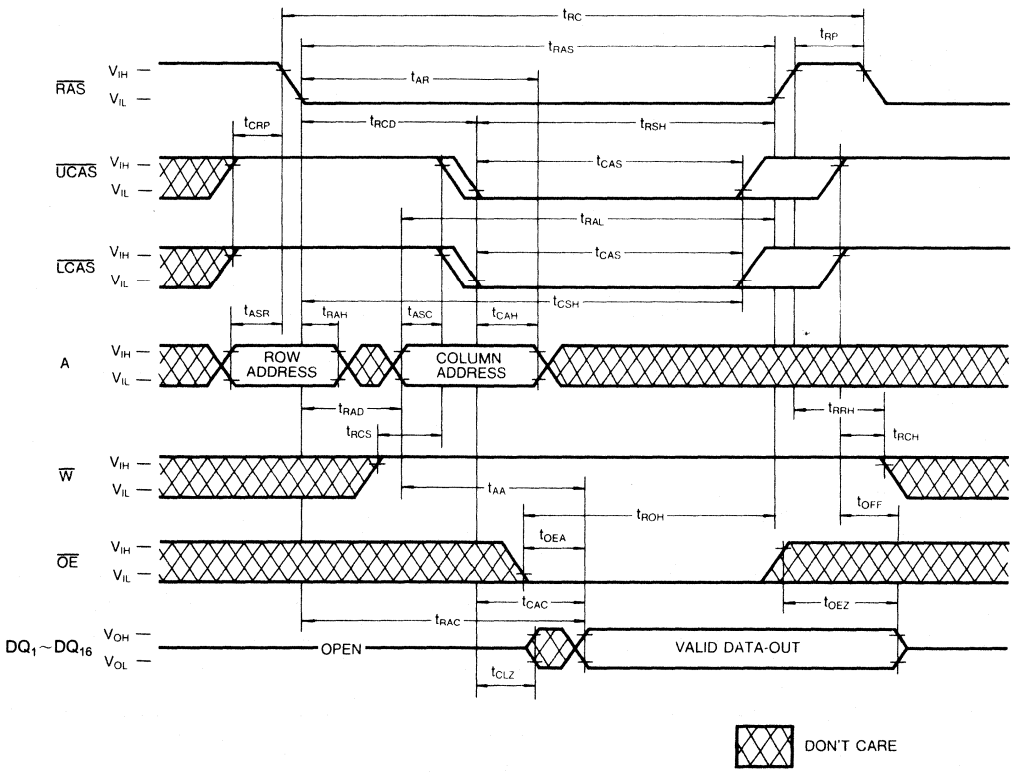


18. t_{DS}, t_{DH} is independetly specified for lower byte $D_{in(1\sim9)}$, upper byte $D_{in(10\sim18)}$.



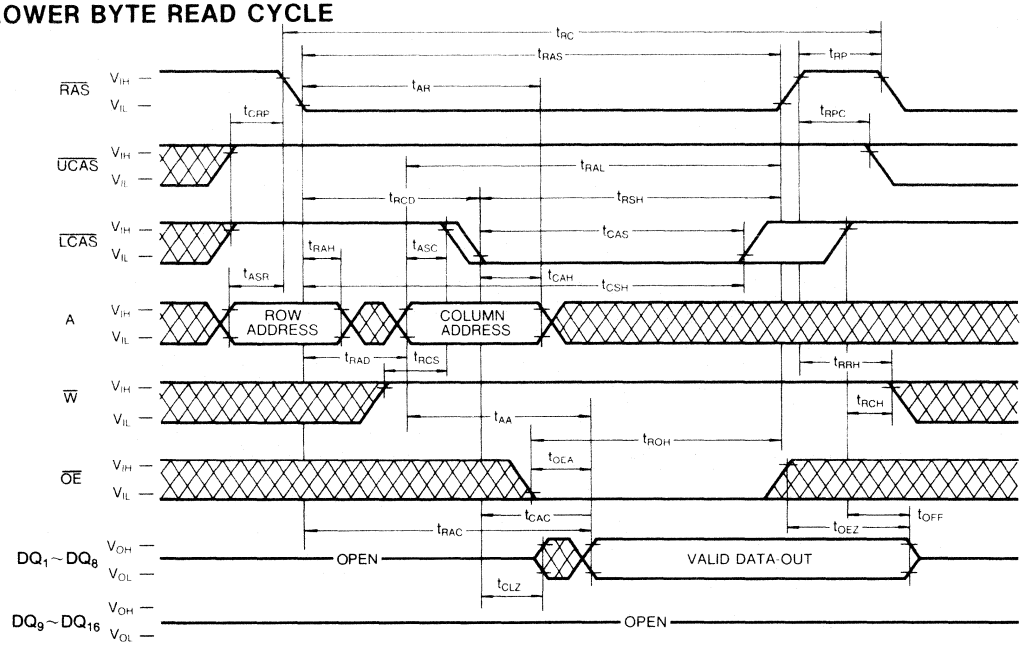
TIMING DIAGRAMS

WORD READ CYCLE

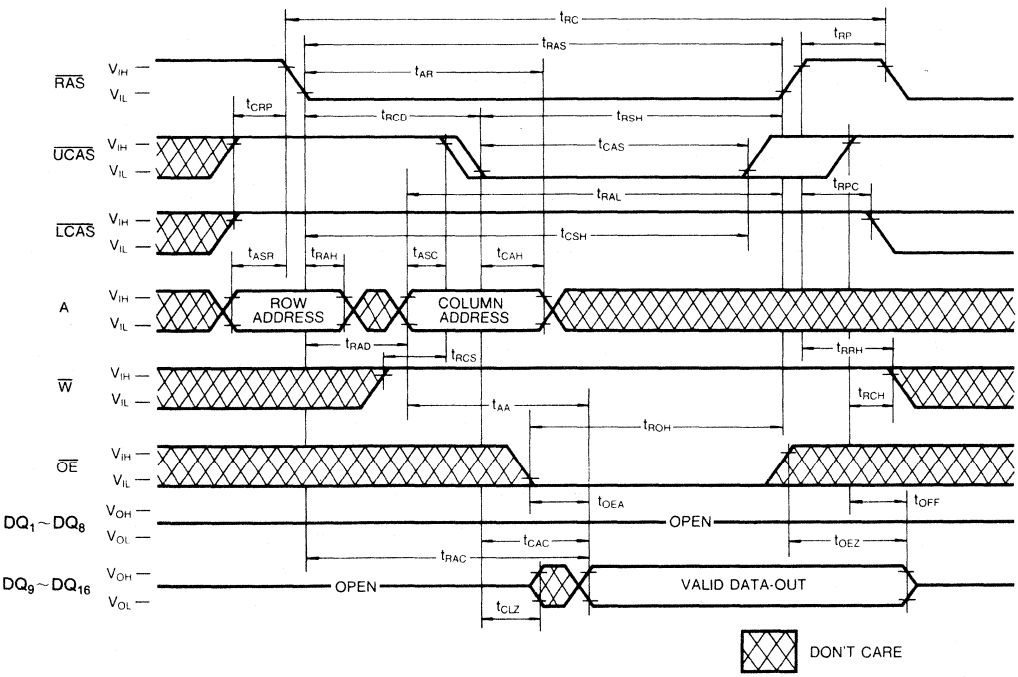


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE

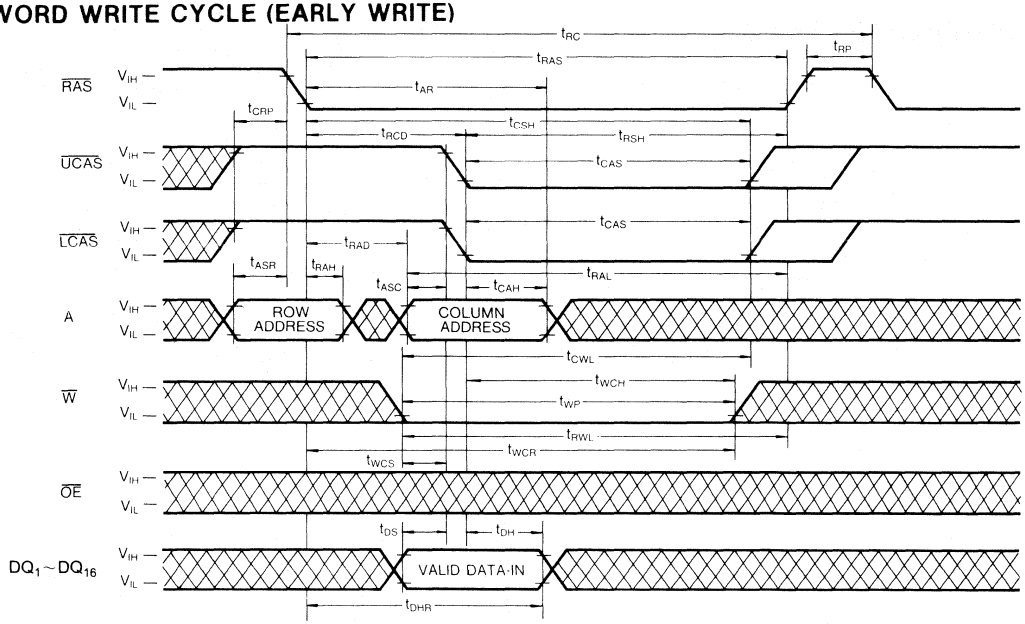


UPPER BYTE READ CYCLE

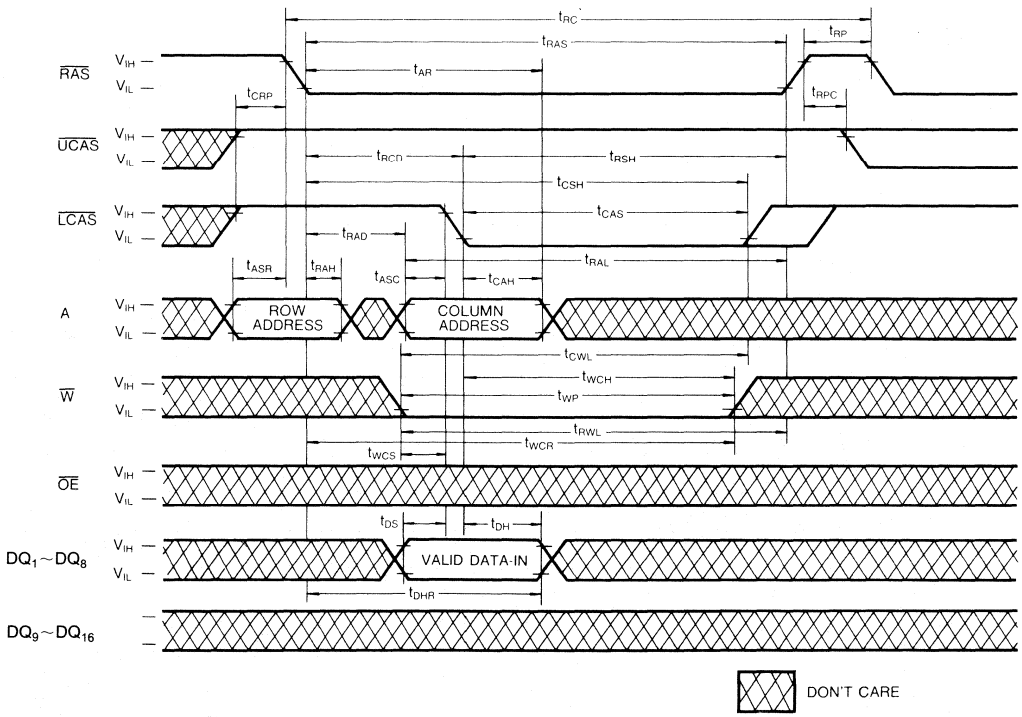


TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)

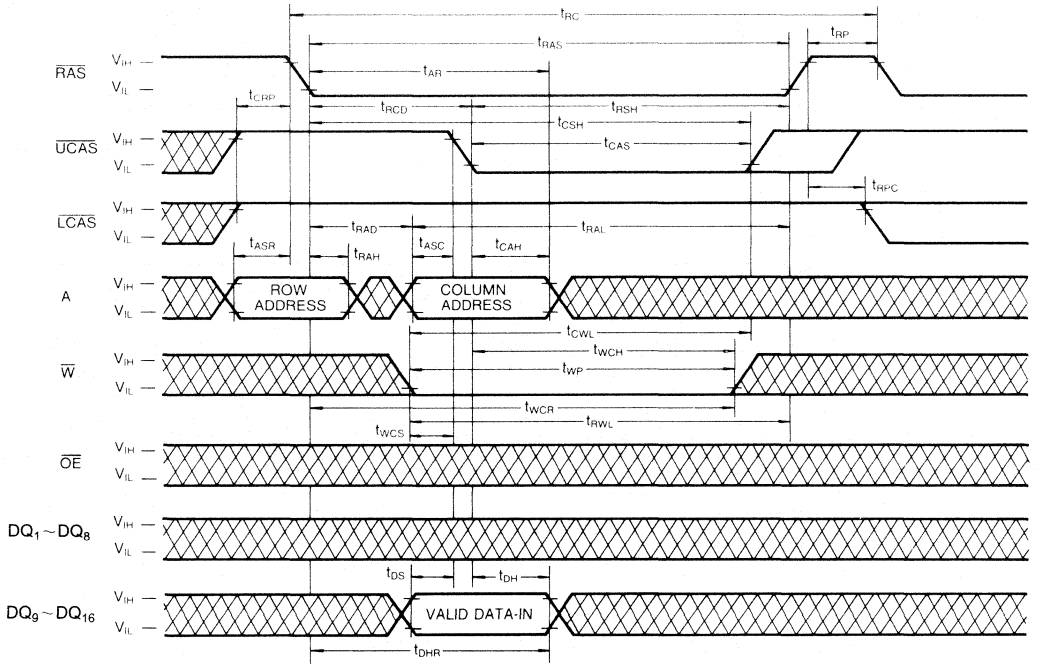


LOWER BYTE WRITE CYCLE (EARLY WRITE)

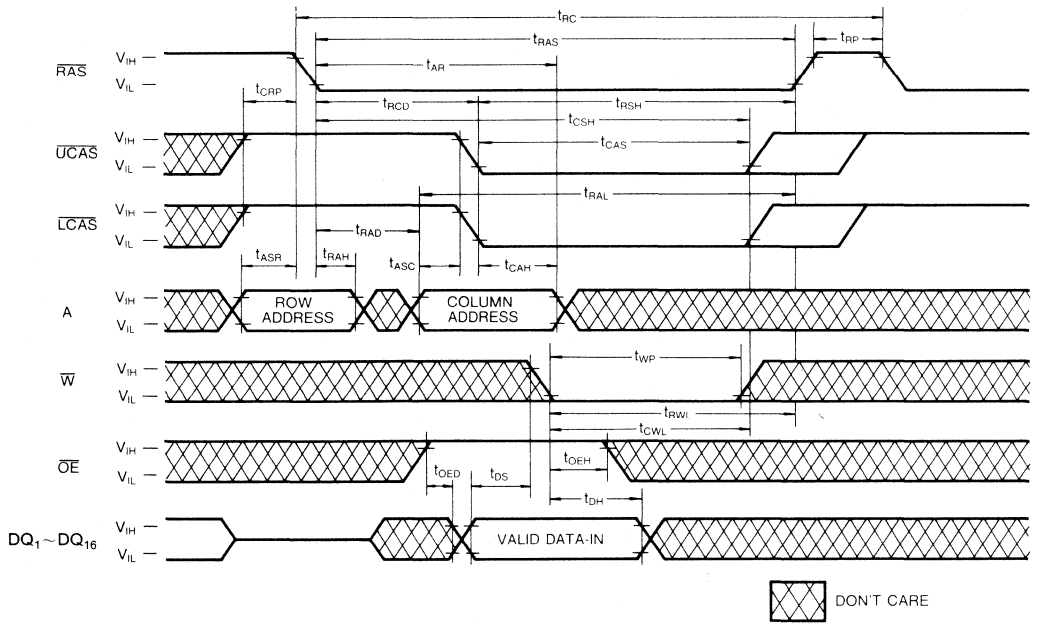


TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)

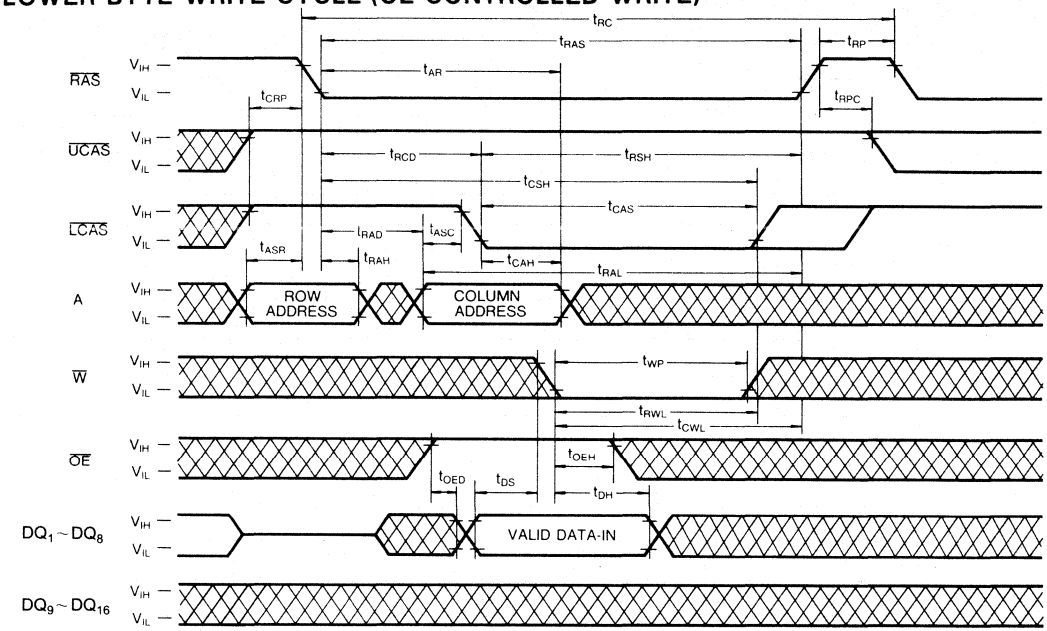


WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

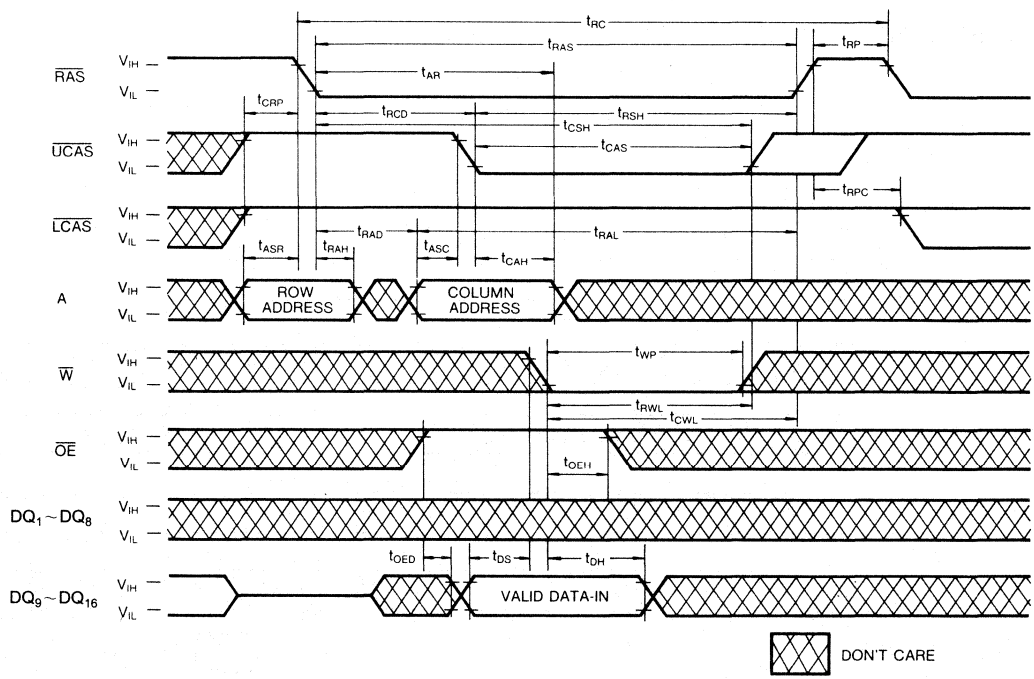


TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

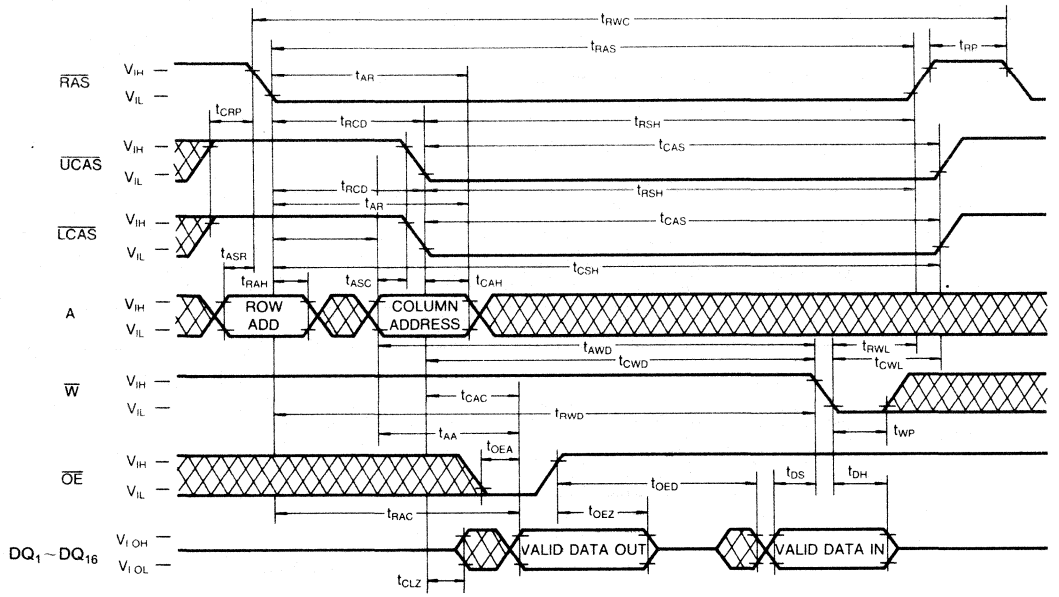


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

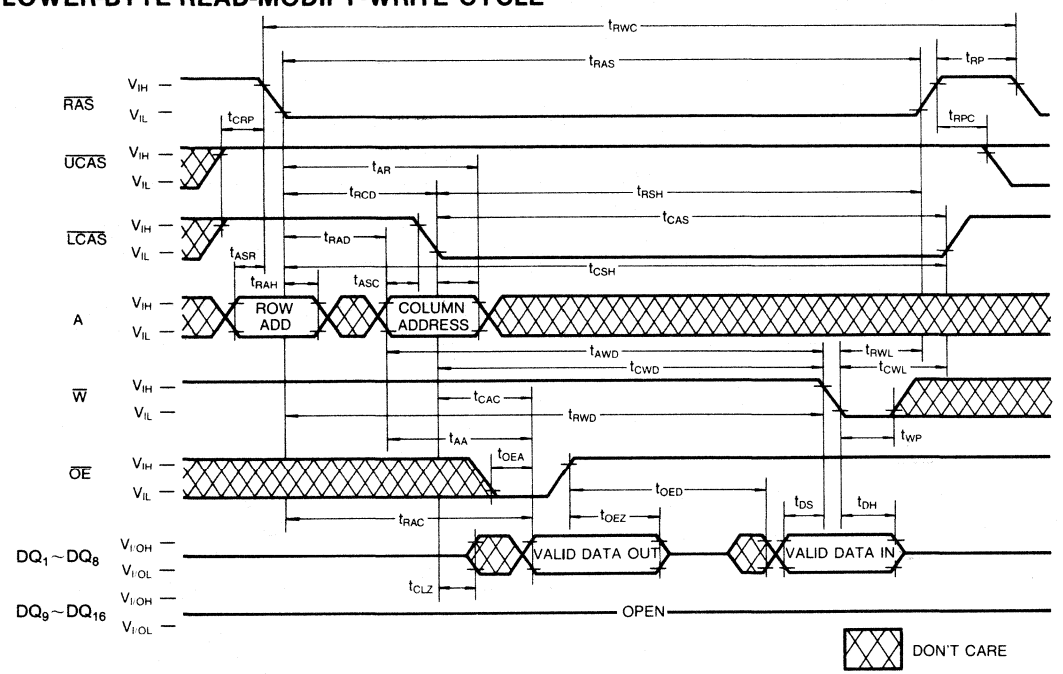


TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE

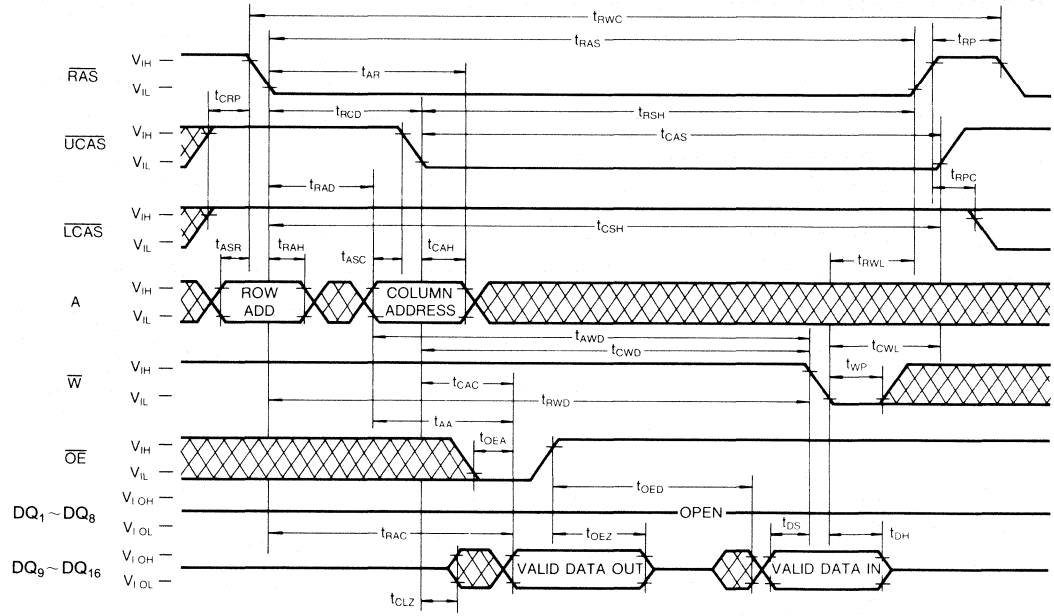


LOWER-BYTE READ-MODIFY-WRITE CYCLE

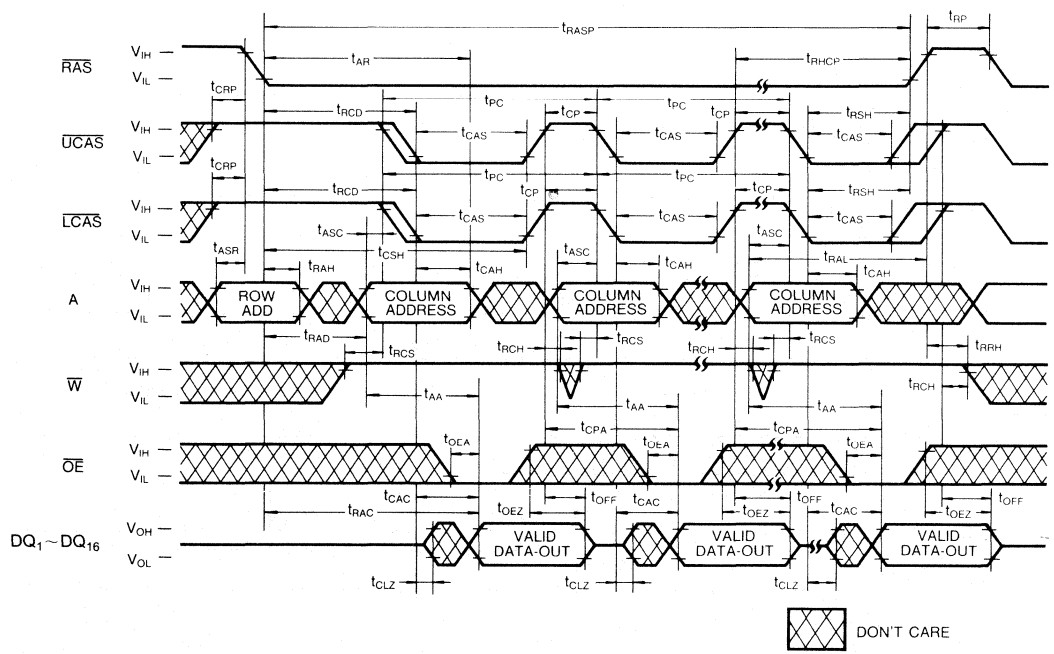


TIMING DIAGRAMS (Continued)

UPPER-BYTE READ-MODIFY-WRITE CYCLE

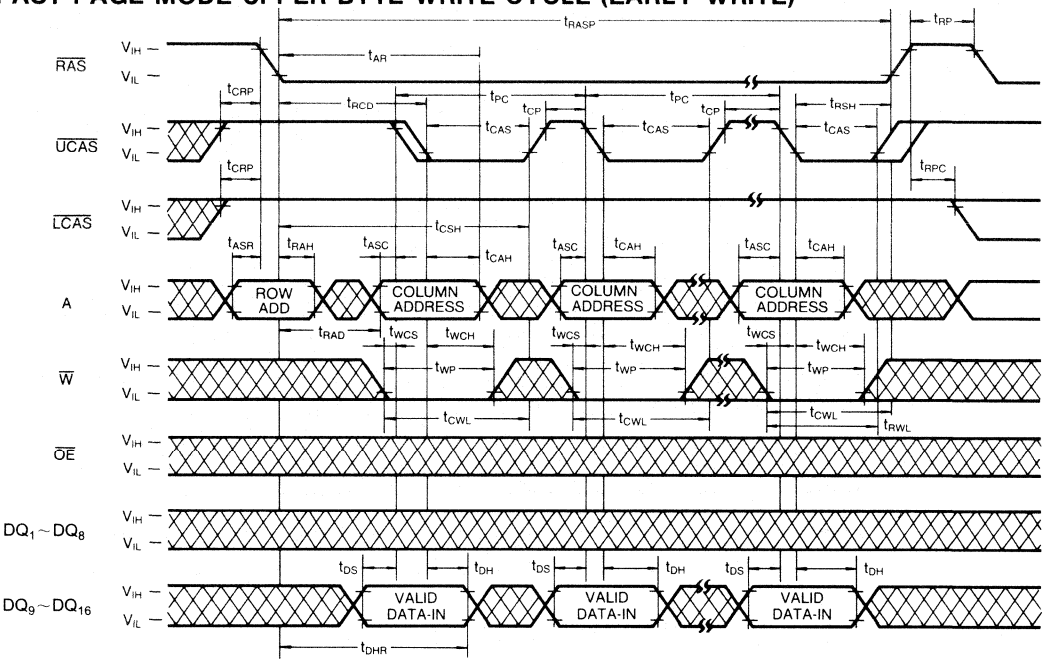


FAST PAGE MODE WORD READ CYCLE

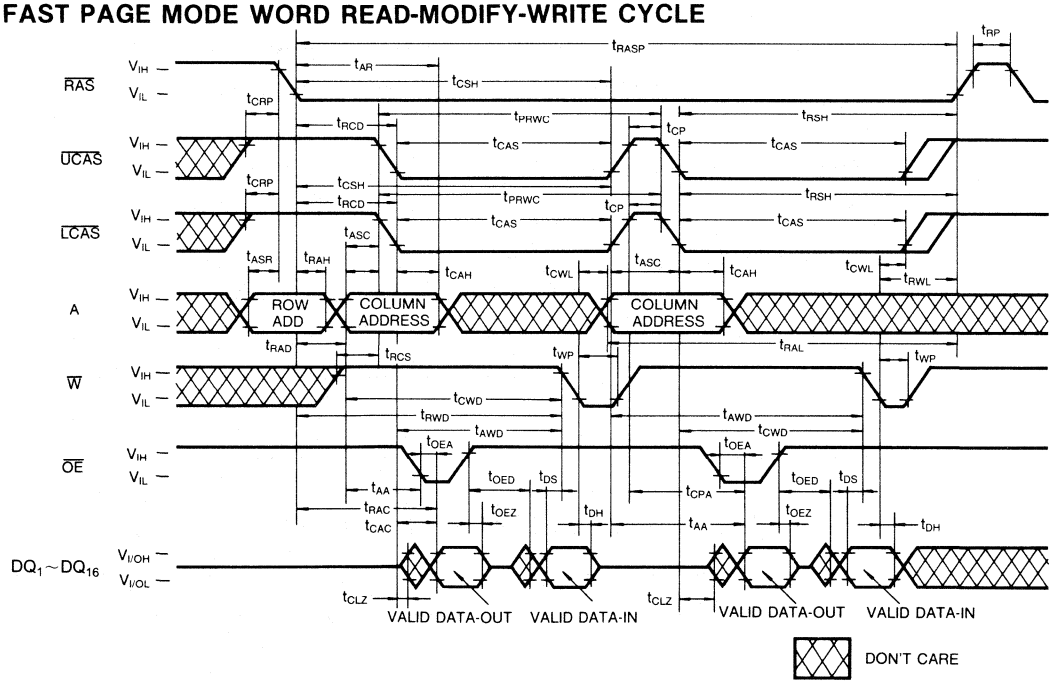


TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

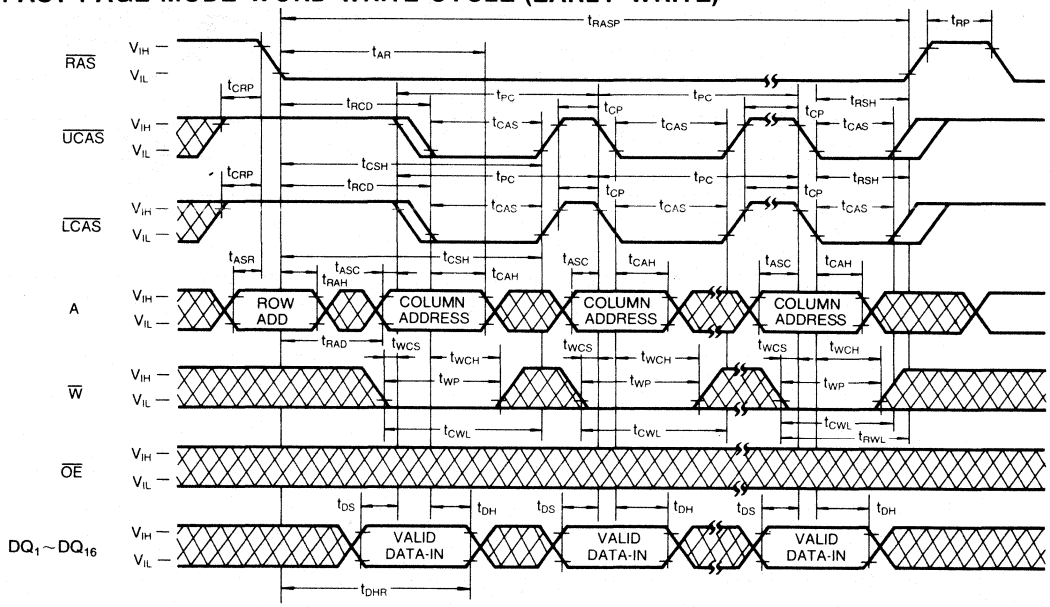


FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE

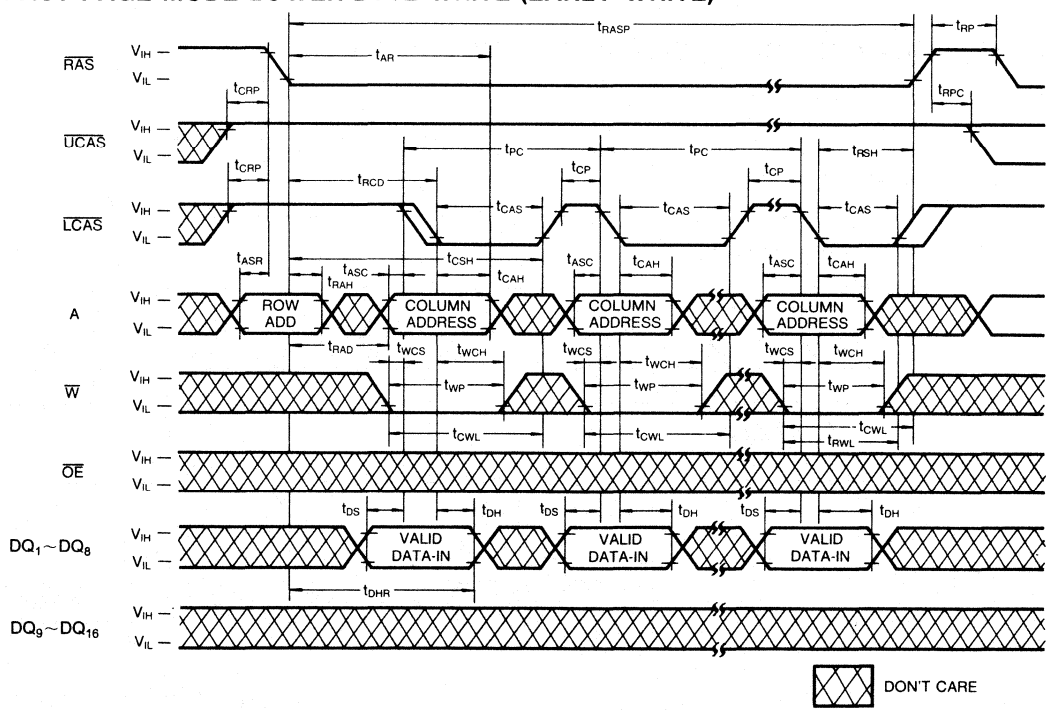


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

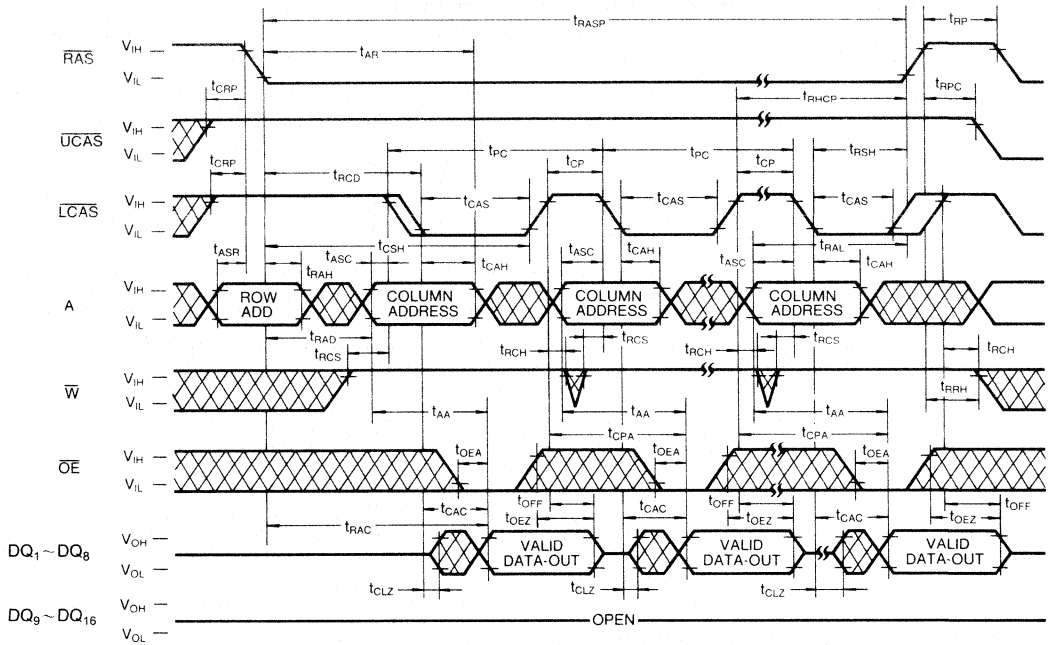


FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)

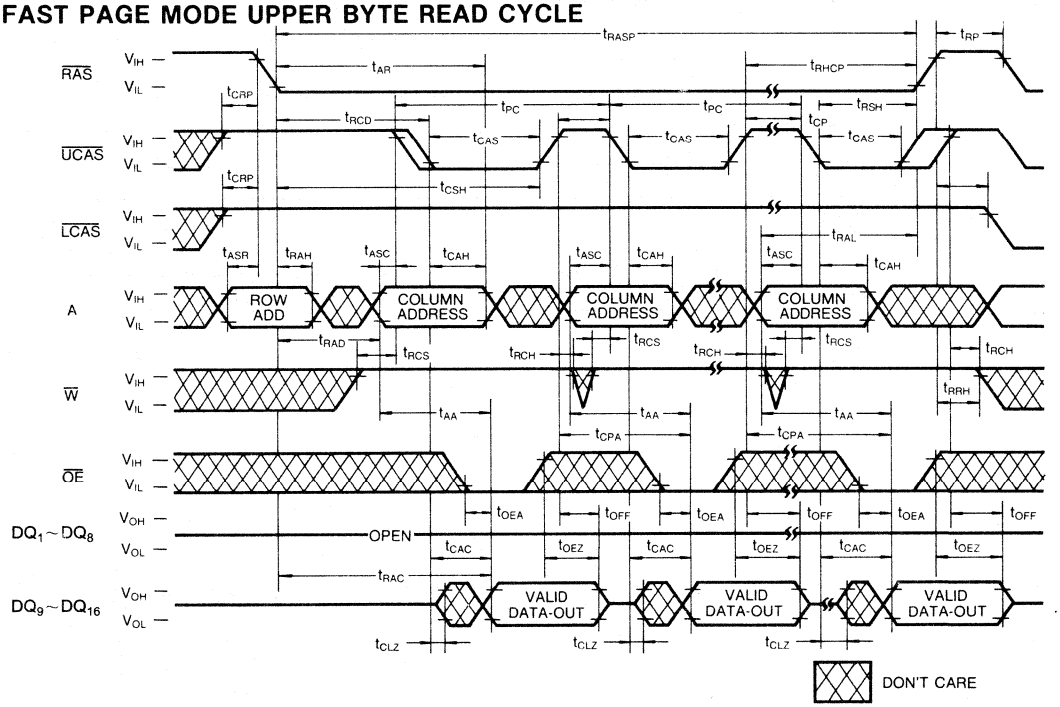


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE

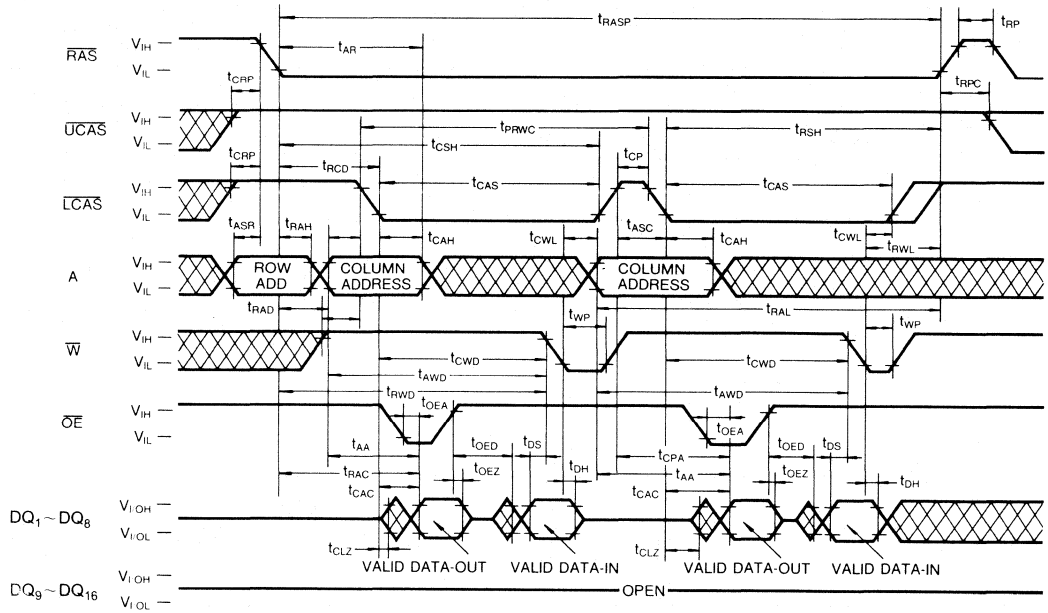


FAST PAGE MODE UPPER BYTE READ CYCLE

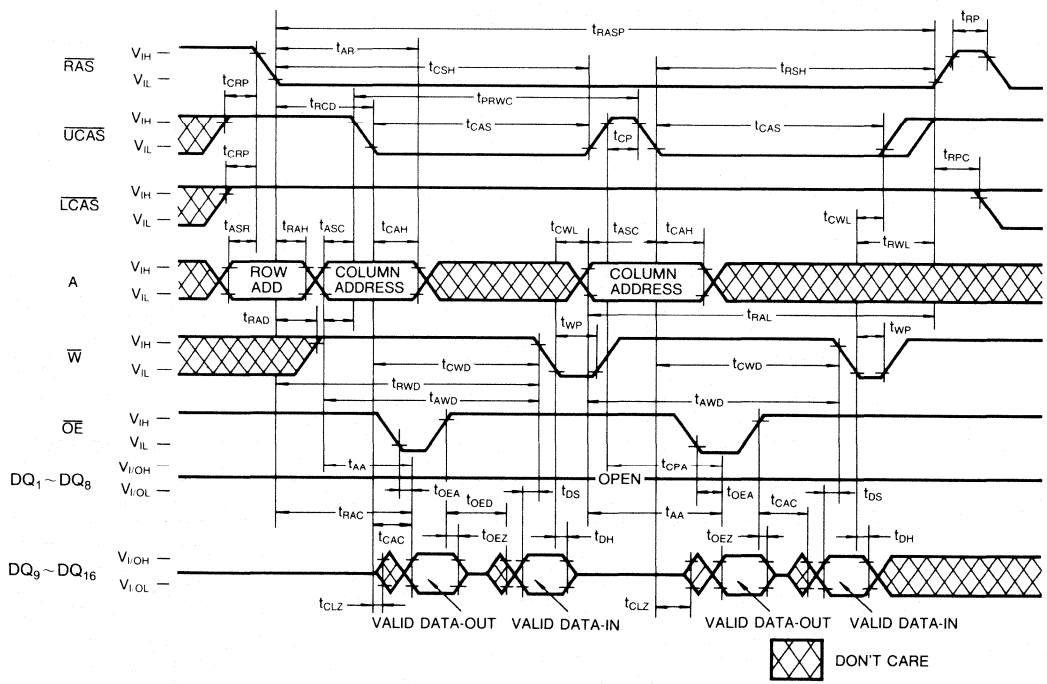


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ-MODIFY-WRITE CYCLE



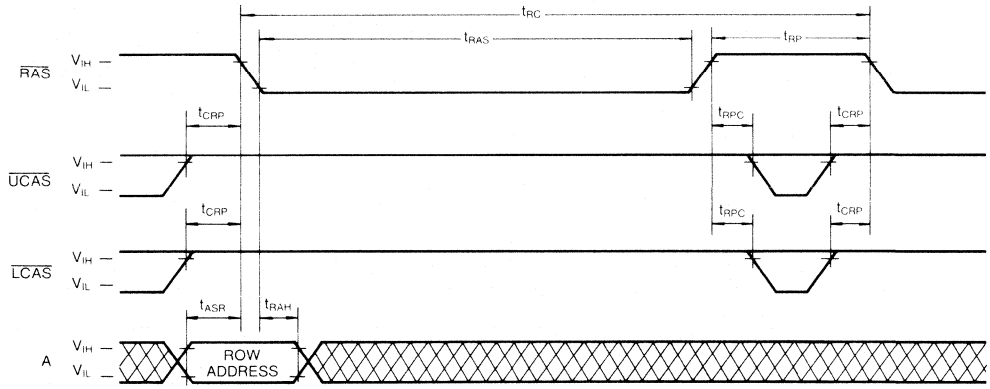
FAST PAGE MODE UPPER BYTE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

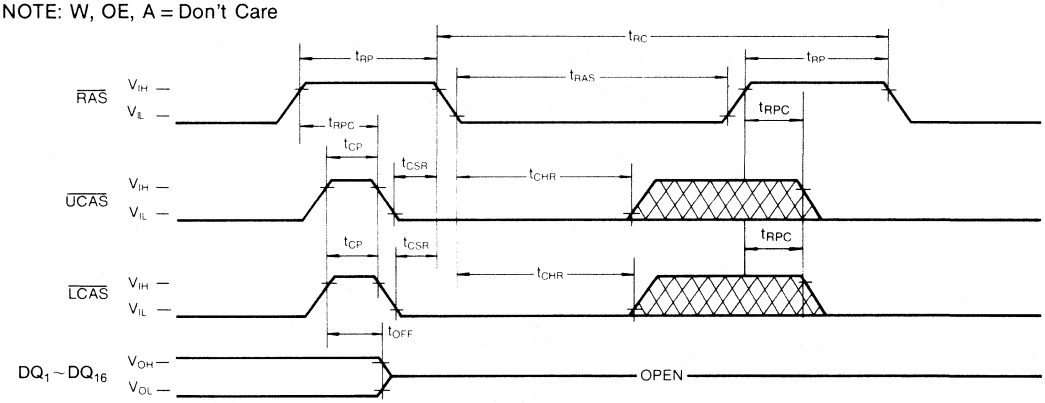
$\overline{RAS}$ ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$=Don't Care



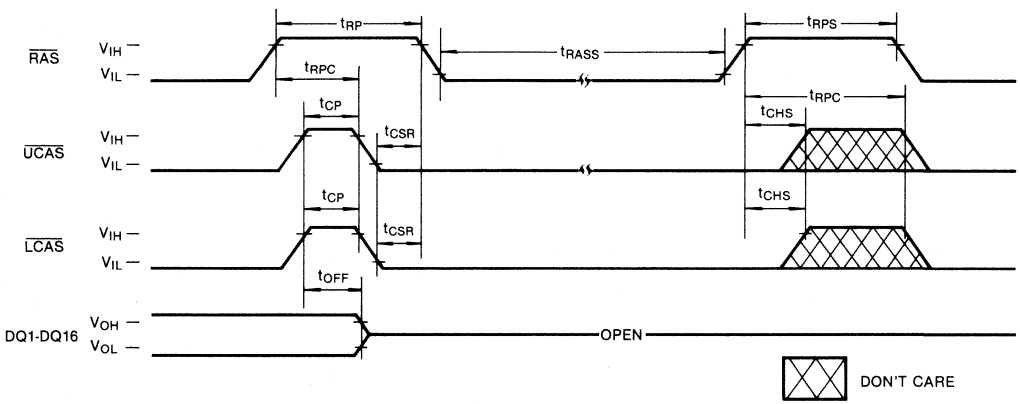
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: W, OE, A = Don't Care



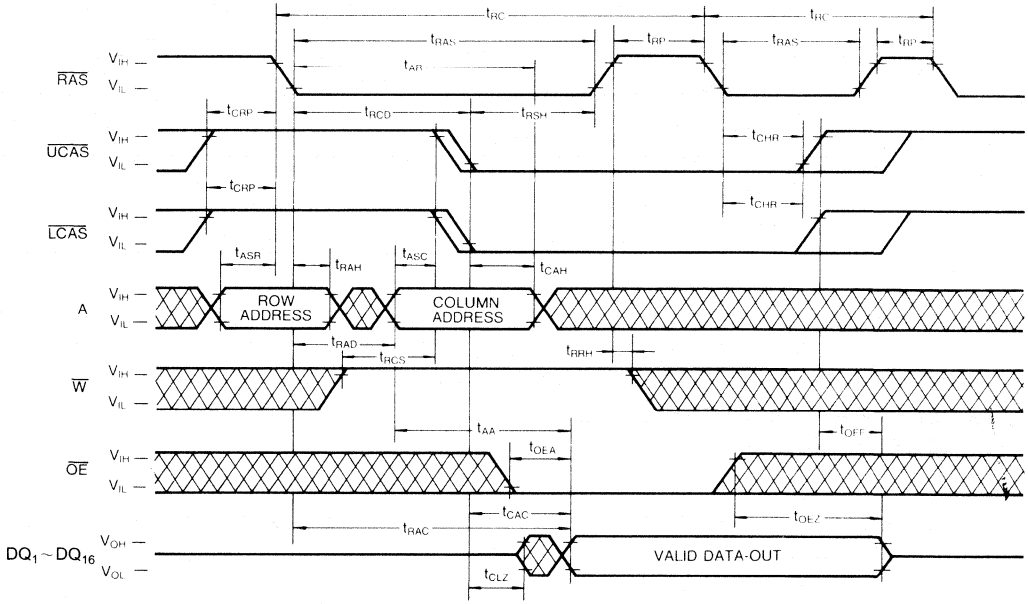
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care

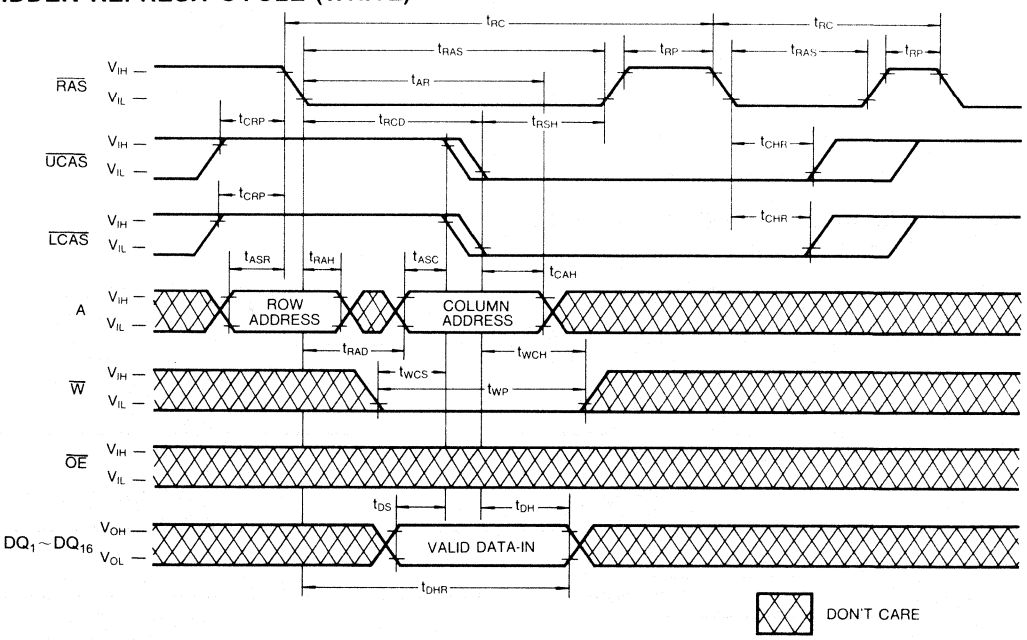


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

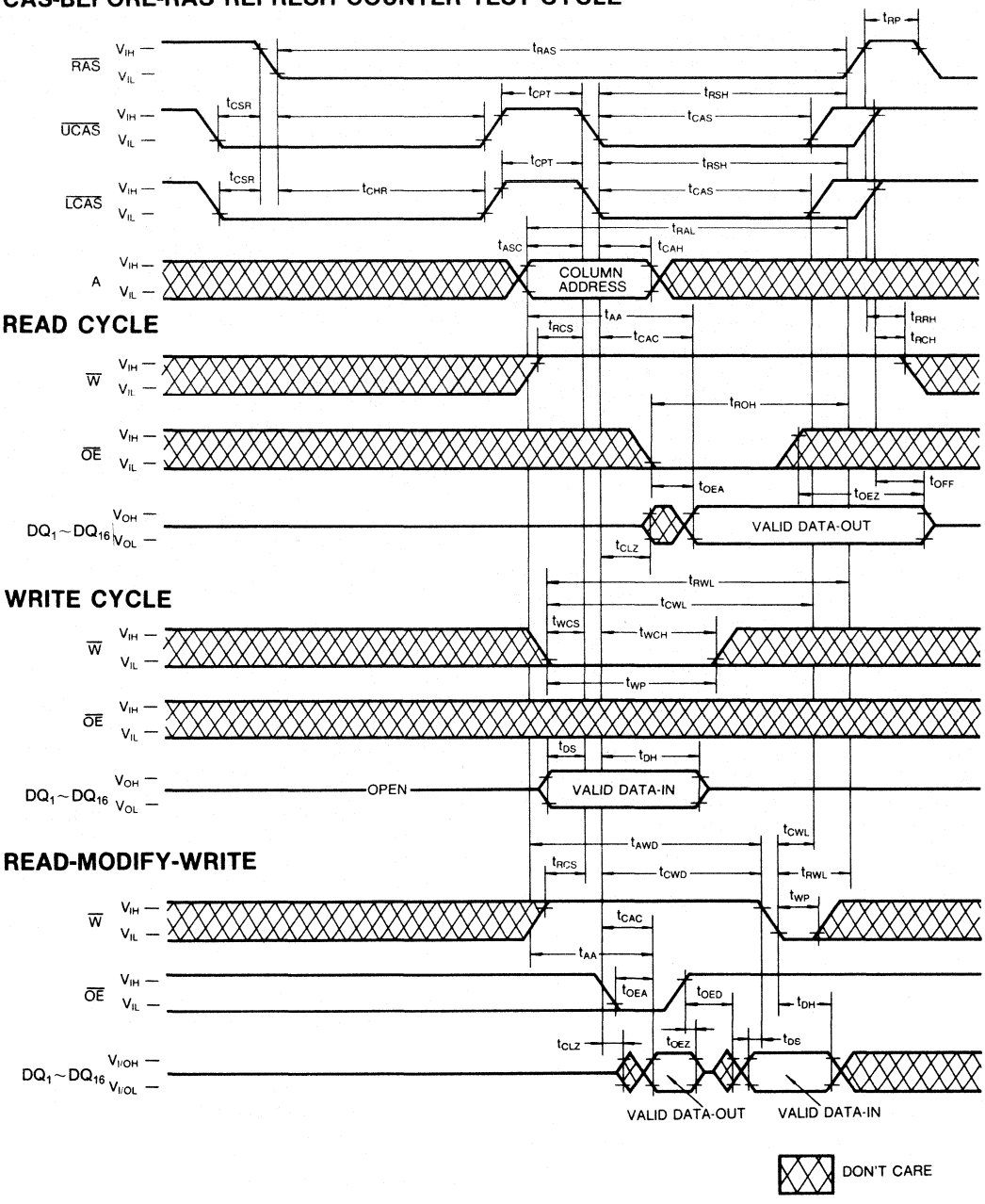


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM416C256LL contains 4,194,304 memory locations arranged in 16 groups of 262,144 x 1 bit each. Eighteen address bits are required to address a particular memory location. Since the KM416C256LL has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{LCAS}$, $\overline{UCAS}$) and the valid row and column address inputs.

Operation of the KM416C256LL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{LCAS}$ ($\overline{UCAS}$) remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{LCAS}$ ($\overline{UCAS}$). This is the beginning of any KM416C256LL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{LCAS}$ ($\overline{UCAS}$) have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM416C256LL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{xCAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{xCAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{xCAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM416C256LL can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$, $\overline{LCAS}$ and $\overline{UCAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{xCAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{xCAS}$. The 8-bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cells. This cycle is achieved by bringing W low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The $\overline{OE}$ input must be low during the time defined by t_{OEA} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM416C256LL DQ pins.

Data Output

The KM416C256LL has a three-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}), the outputs are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs enter into the low impedance state in the time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM416C256LL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} times are not met)

DEVICE OPERATION (Continued)

Refresh

The data in the KM416C256LL is stored as a charge on microscopic capacitor within each memory cell. The stored charge tends to dissipate over time and will affect data integrity if the charge is not periodically refreshed. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row address (A0-A8).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM416C256LL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{LCAS}$ or $\overline{UCAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ transitions low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending either $\overline{LCAS}$ or $\overline{UCAS}$ input active time and cycling $\overline{RAS}$. The hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Self Refresh: The self refresh is $\overline{CAS}$-before-$\overline{RAS}$ refresh to be used for long periods of standby, such as a battery back-up. In normal $\overline{CAS}$-before-$\overline{RAS}$ condition, when $\overline{RAS}$ is held low above 100μs an internal timer activates an refresh operation of consecutive row addresses in DRAM. The self refresh mode is exited when either $\overline{RAS}$ or $\overline{CAS}$ goes high(V_{IH}).

Other Refresh Methods: It is also possible to refresh the KM416C256LL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM416C256LL has Fast page mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is asserted high and then low again while $\overline{RAS}$ is asserted low, the read and write operations are enabled. In this method, the row address bits A0 through A8 are supplied by on chip refresh counter.

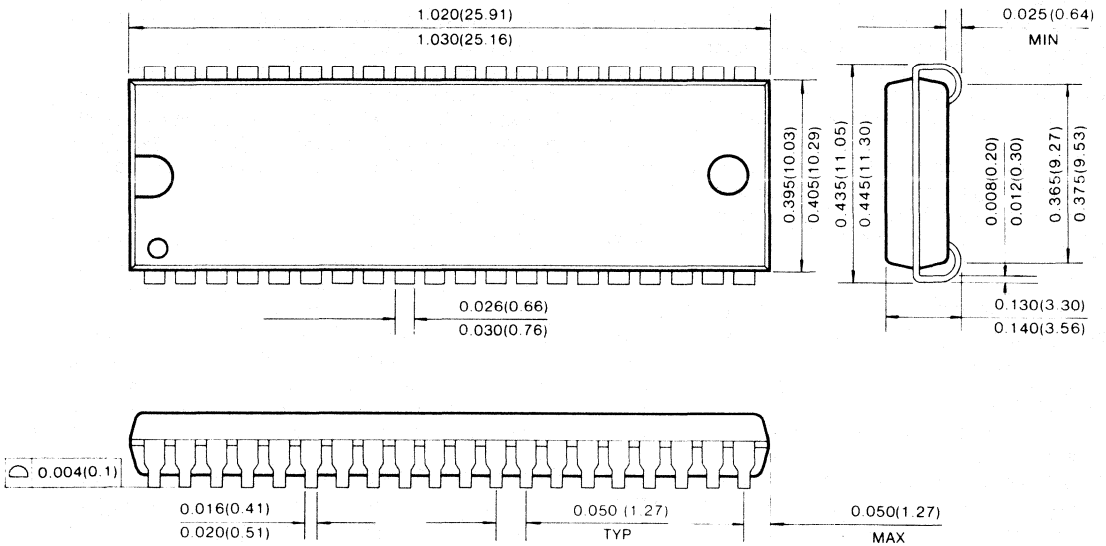
Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM416C256LL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held a valid V_{IH} in order to minimize the power-up current.

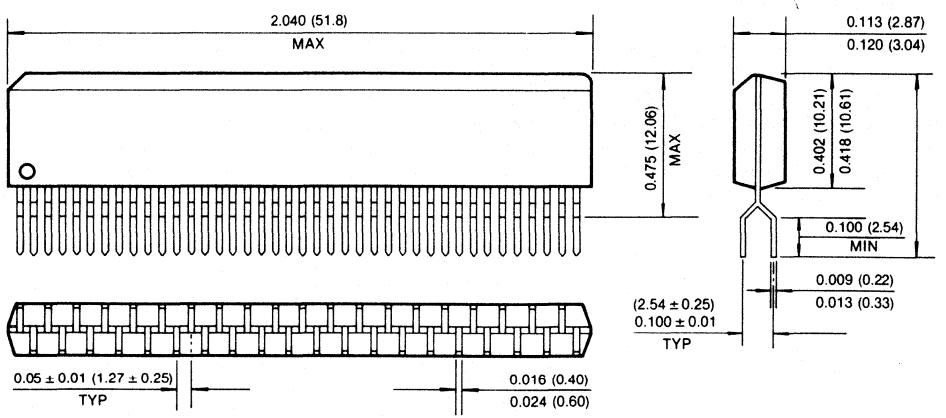
PACKAGE DIMENSION

40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



40-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



256K x 18 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM418C256/L/SL-7	70ns	20ns	130ns
KM418C256/L/SL-8	80ns	20ns	150ns
KM418C256/L/SL-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL and CMOS compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Triple +5V±10% power supply**
- **Refresh Cycle**
  - **— 512 cycle/8ms (Normal)**
  - **— 512 cycle/64ms (L-version)**
  - **— 512 cycle/128ms (SL-version)**
- **Power Dissipation**
  - **— Standby: 11mW (Normal)**
    1.1mW (L-version)
    0.55mW (SL-version)
  - **— Active (70/80/100): 825/715/605mW**
- **Available in Plastic SOJ and ZIP**
- **JEDEC Standard pinout**

GENERAL DESCRIPTION

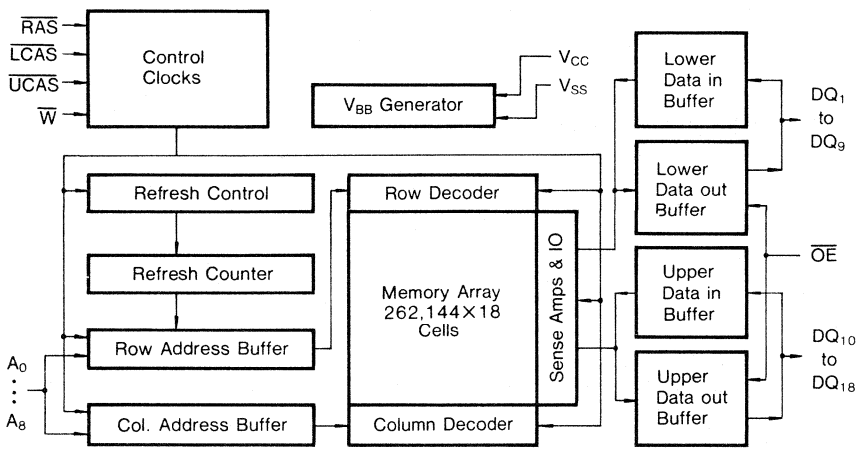
The Samsung KM418C256/L/SL is a CMOS high speed 262,144 bit x 18 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM418C256/L/SL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM418C256/L/SL is fabricated using Samsung's advanced CMOS process.

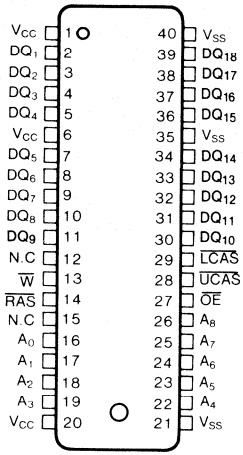
2

FUNCTIONAL BLOCK DIAGRAM



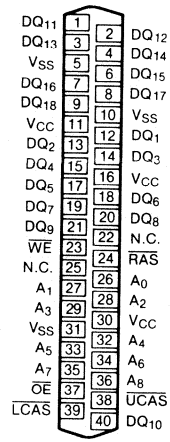
PIN CONFIGURATION (Top Views)

• **KM418C256J/LJ/SLJ**



(SOJ)

• **KM418C256Z/LZ/SLZ**



(ZIP)

Pin Name	Pin Function
A_0-A_8	Address Inputs
DQ_{1-18}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe

Pin Name	Pin Function
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power (+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$, or $\overline{LCAS}$, Address Cycling @t_{RC} = min.)	KM418C256/L/SL-7 KM418C256/L/SL-8 KM418C256/L/SL-10	I_{CC1}	— — —	150 130 110	mA mA mA
Standby Current ($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$ = $\overline{LCAS}$ = V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM418C256/L/SL-7 KM418C256/L/SL-8 KM418C256/L/SL-10	I_{CC3}	— — —	150 130 110	mA mA mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{PC} = min.)	KM418C256/L/SL-7 KM418C256/L/SL-8 KM418C256/L/SL-10	I_{CC4}	— — —	90 80 70	mA mA mA
Standby Current ($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ ≥ V_{CC} − 0.2V)	KM418C256 KM418C256L KM418C256SL	I_{CC5}	— — —	1 200 100	mA μA μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @t_{RC} = min.)	KM418C256/L/SL-7 KM418C256/L/SL-8 KM418C256/L/SL-10	I_{CC6}	— — —	150 130 110	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode Input High Voltage (V_{IH}) = V_{CC}-0.2V Input Low Voltage (V_{IL}) = 0.2V $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V D_{IN} = Don't Care T_{RC}=125μS(L-ver), T_{RC}=250μS(SL-ver), T_{RAS}=T_{RAS}min.~1μS,	KM418C256L KM418C256SL	I_{CC7}	— —	300 150	μA μA
Input Leakage Current (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$ = V_{IL}. In I_{CC4}, Address can be changed maximum once while $\overline{UCAS}$ and $\overline{UCAS}$ = V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_8)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_{18})	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC} = 5.0V ± 10%, See notes 1, 2)

Parameter	Symbol	KM418C256/L/SL-7		KM418C256/L/SL-8		KM418C256/L/SL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	180		200		240		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	55	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command set-up time	t_{WCS}	0		0		0		ns	8
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	

AC CHARACTERISTICS (Continued)

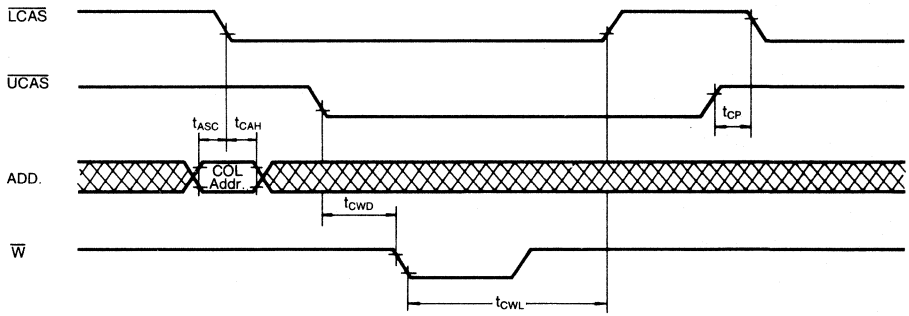
Parameter	Symbol	KM418C256/L/SL-7		KM418C256/L/SL-8		KM418C256/L/SL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (512 cycles)	t_{REF}		8		8		8	ms	
Refresh period (L-version)	t_{REF}		64		64		64	ms	
Refresh period (SL-version)	t_{REF}		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	45		45		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	95		105		130		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	60		65		75		ns	8
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3
Fast page mode cycle time	t_{PC}	45		50		55		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	95		100		115		ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
Access time from $\overline{OE}$	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data-in delay time	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

KM418C256 Truth Table

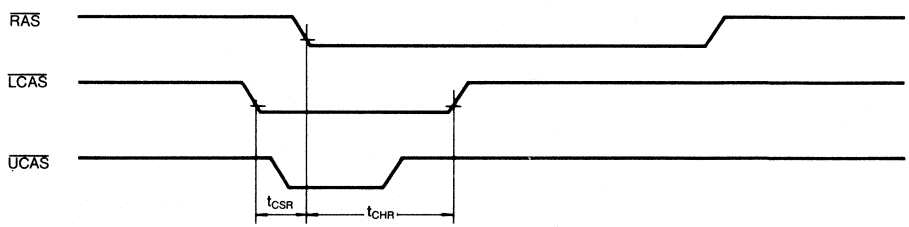
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	$DQ_{1\sim9}$	$DQ_{10\sim18}$	State
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Lower Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-In	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	—

NOTES

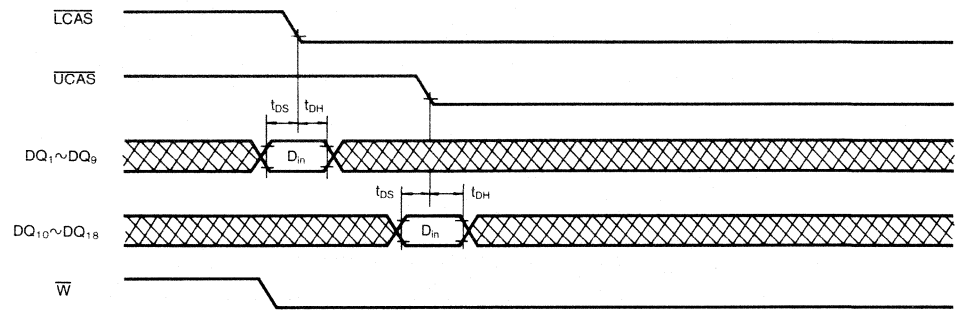
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating aprameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
17. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.

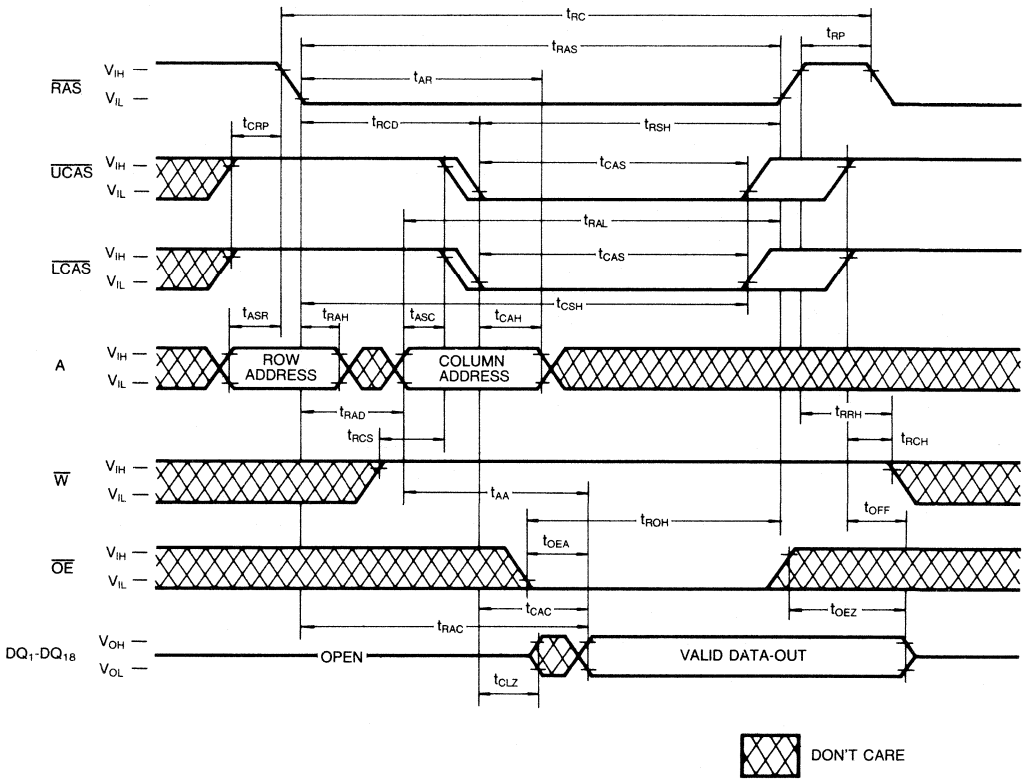


18. t_{DS}, t_{DH} is independetly specified for lower byte $D_{in(1\sim9)}$, upper byte $D_{in(10\sim18)}$.



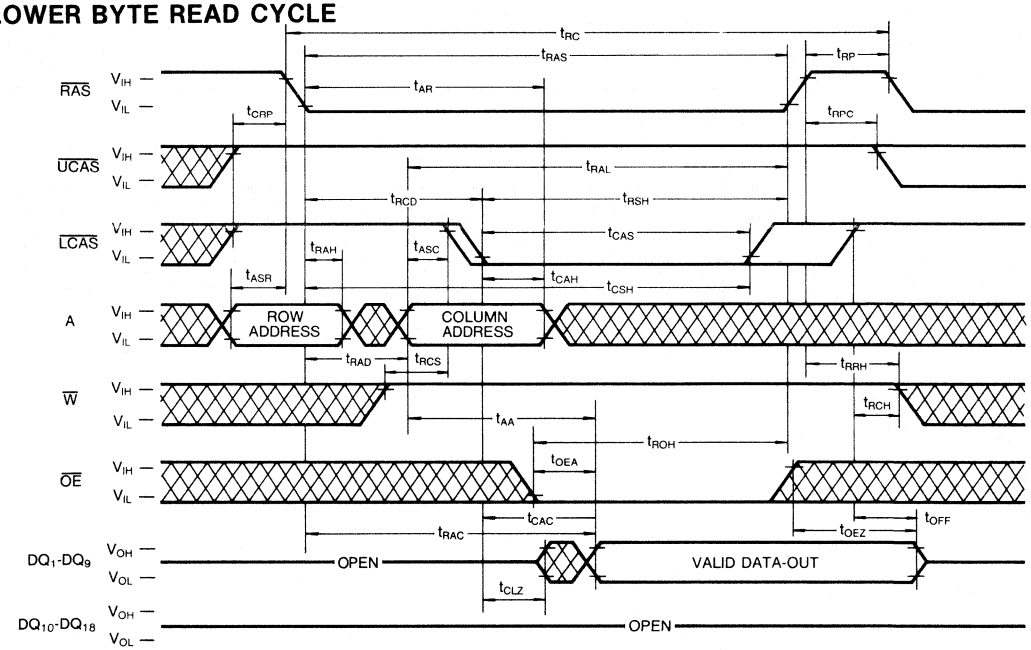
TIMING DIAGRAMS

WORD READ CYCLE

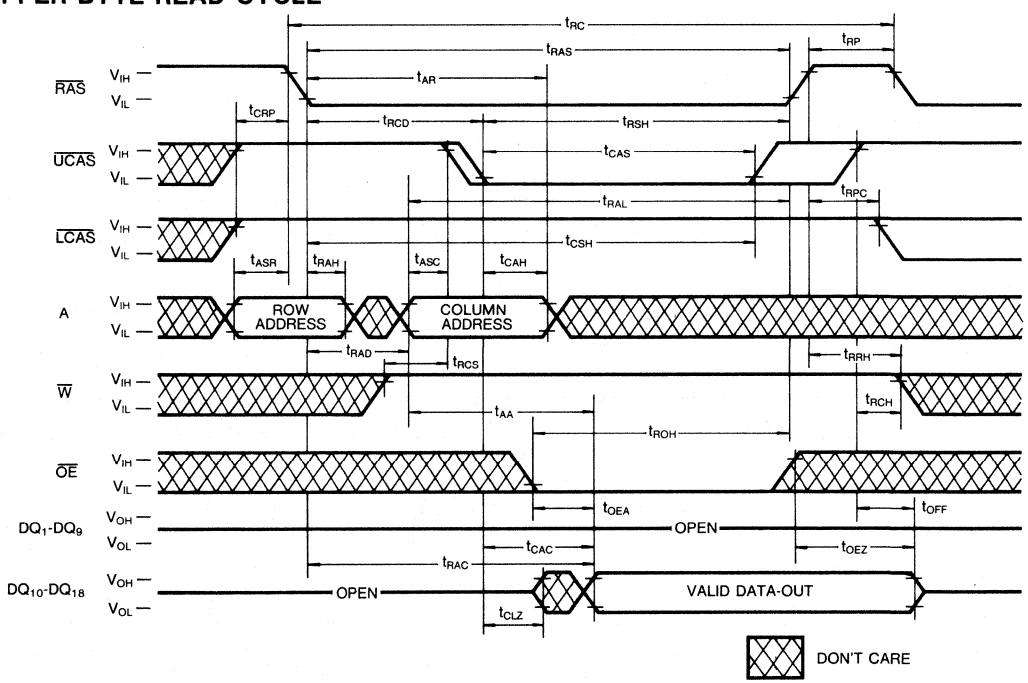


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE

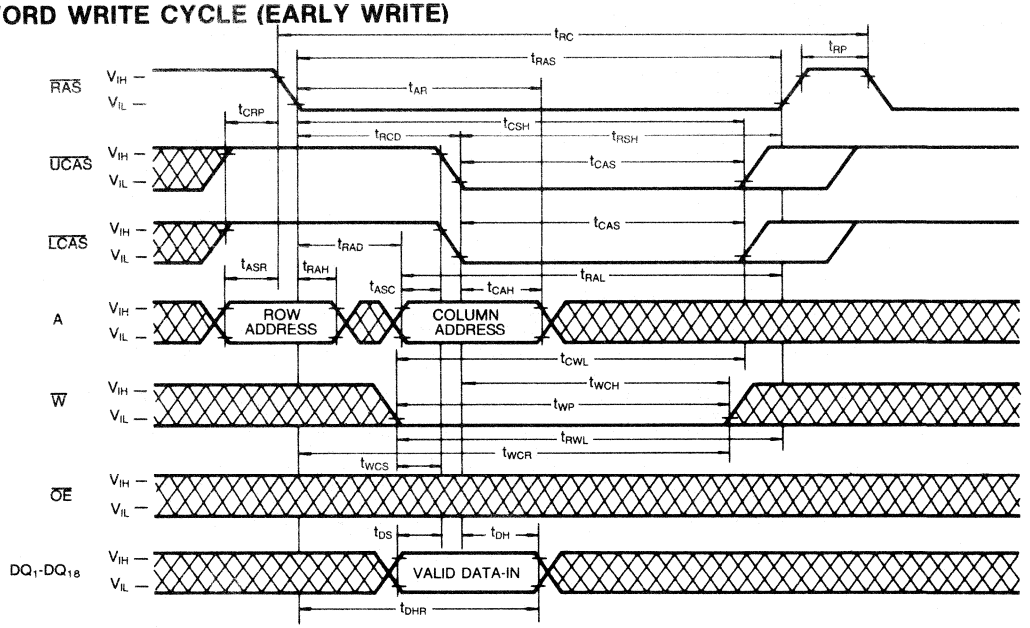


UPPER BYTE READ CYCLE

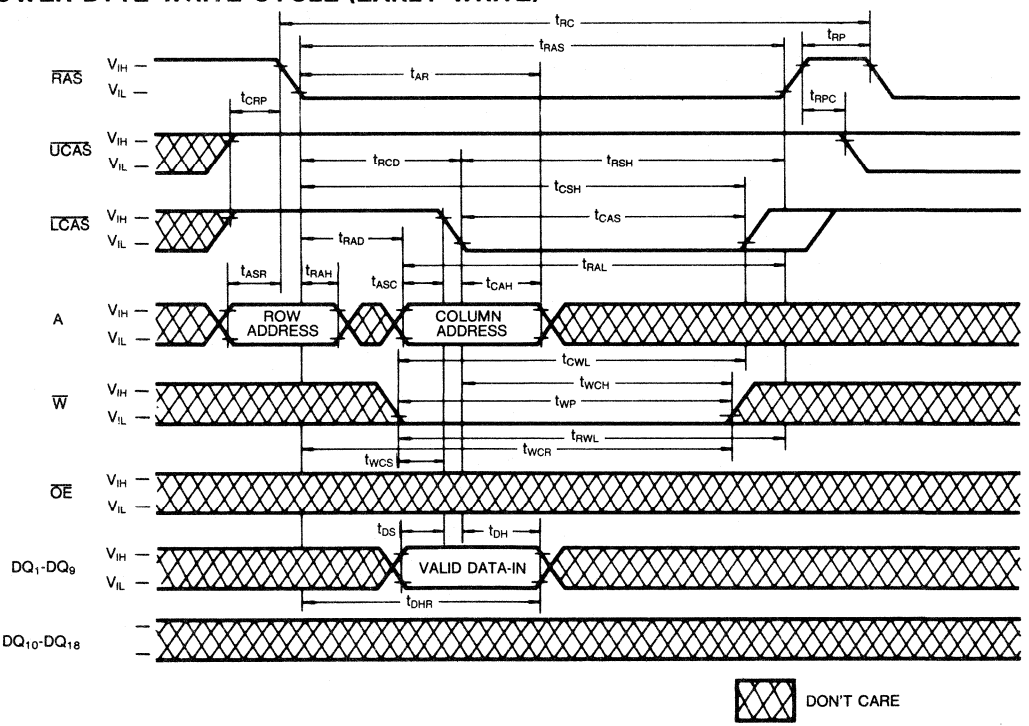


TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)

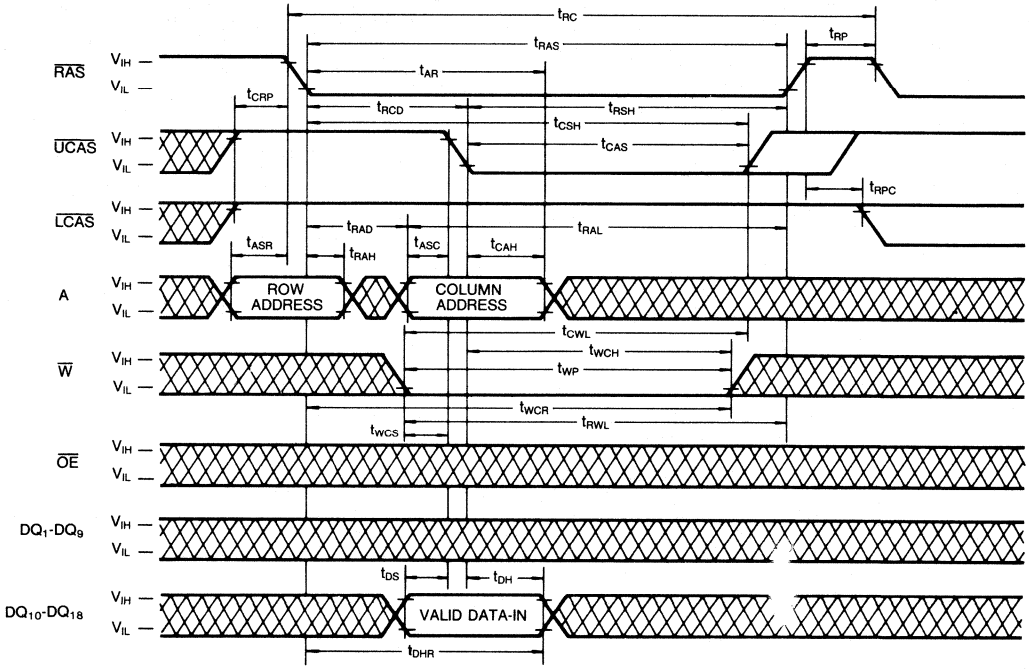


LOWER BYTE WRITE CYCLE (EARLY WRITE)

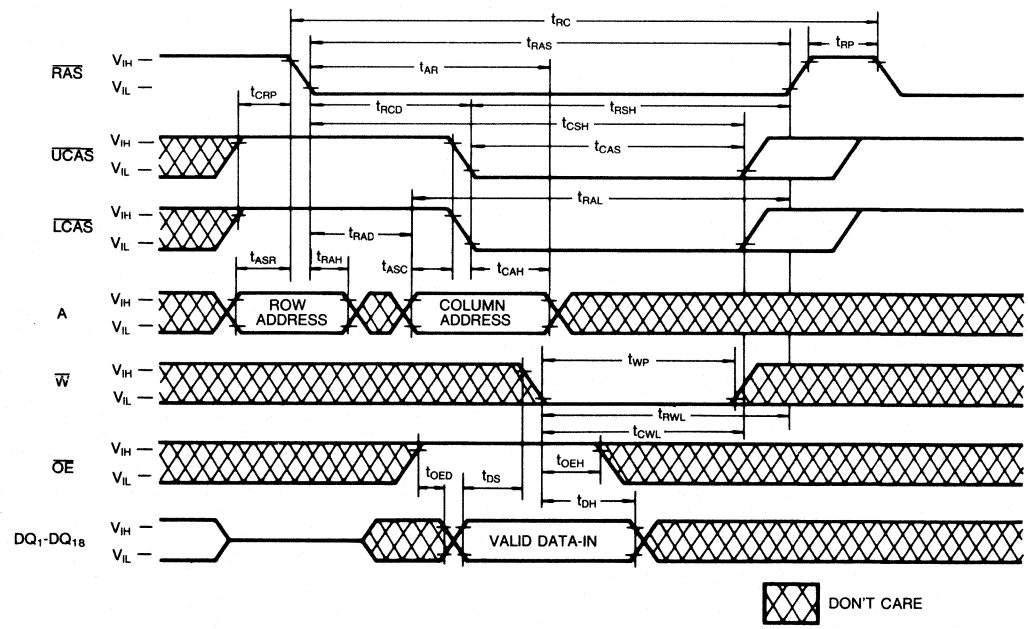


TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)

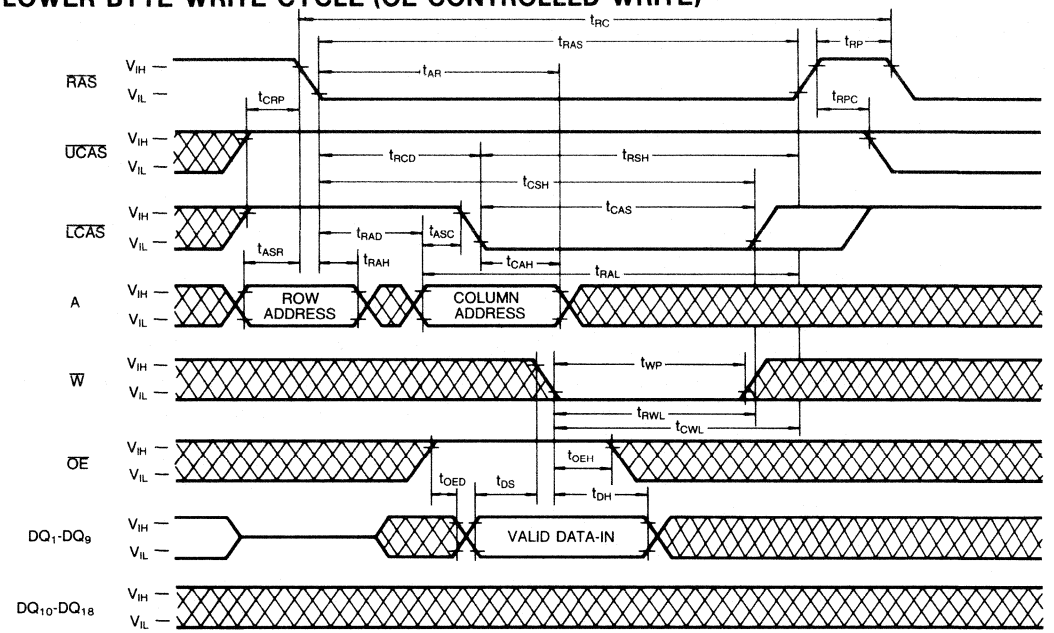


WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

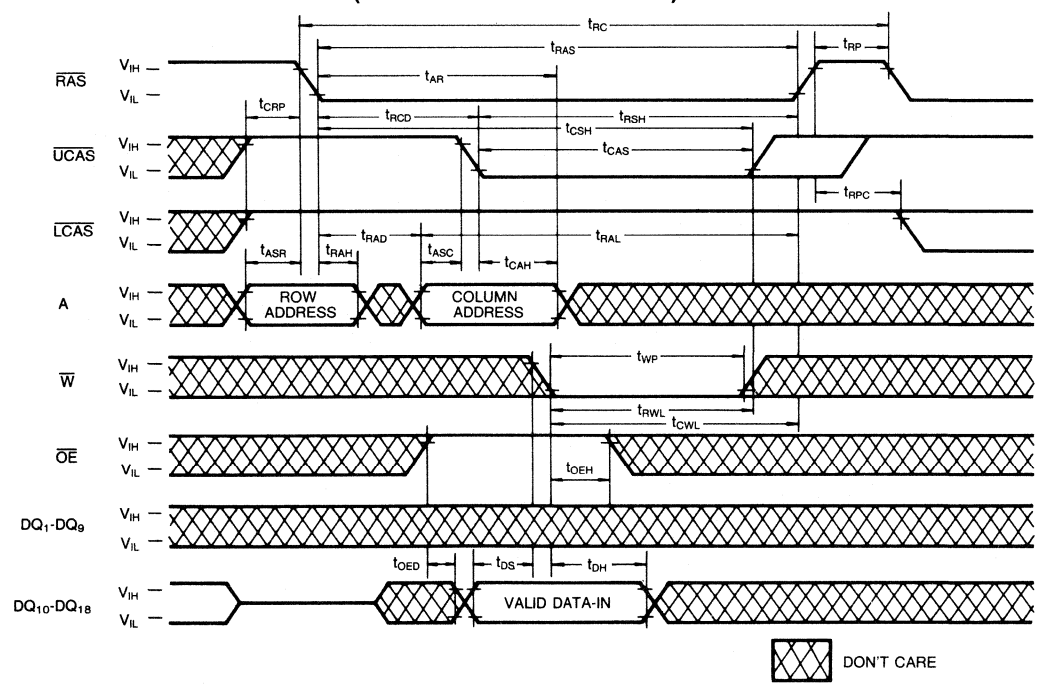


TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

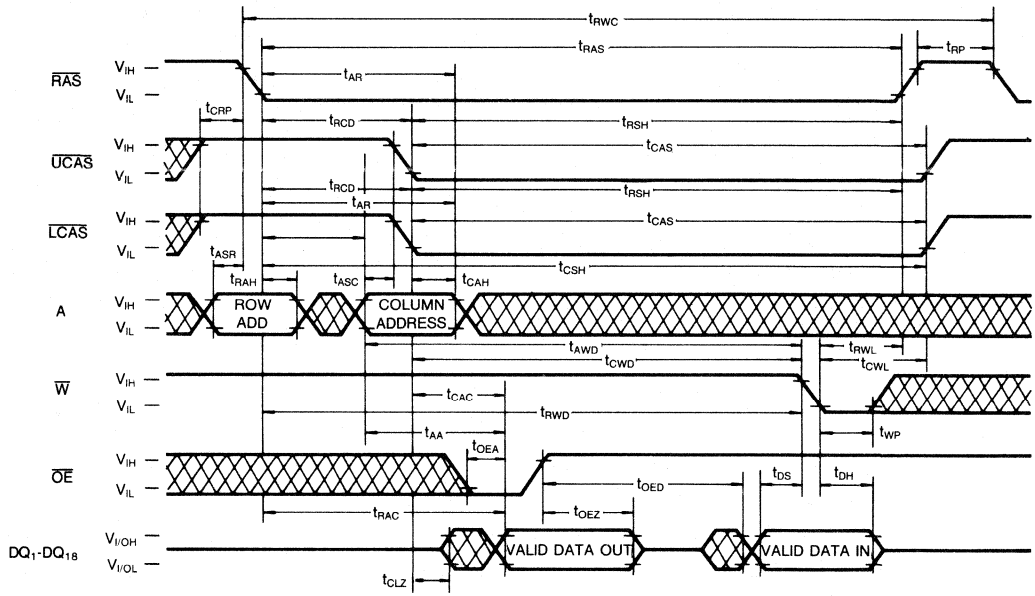


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

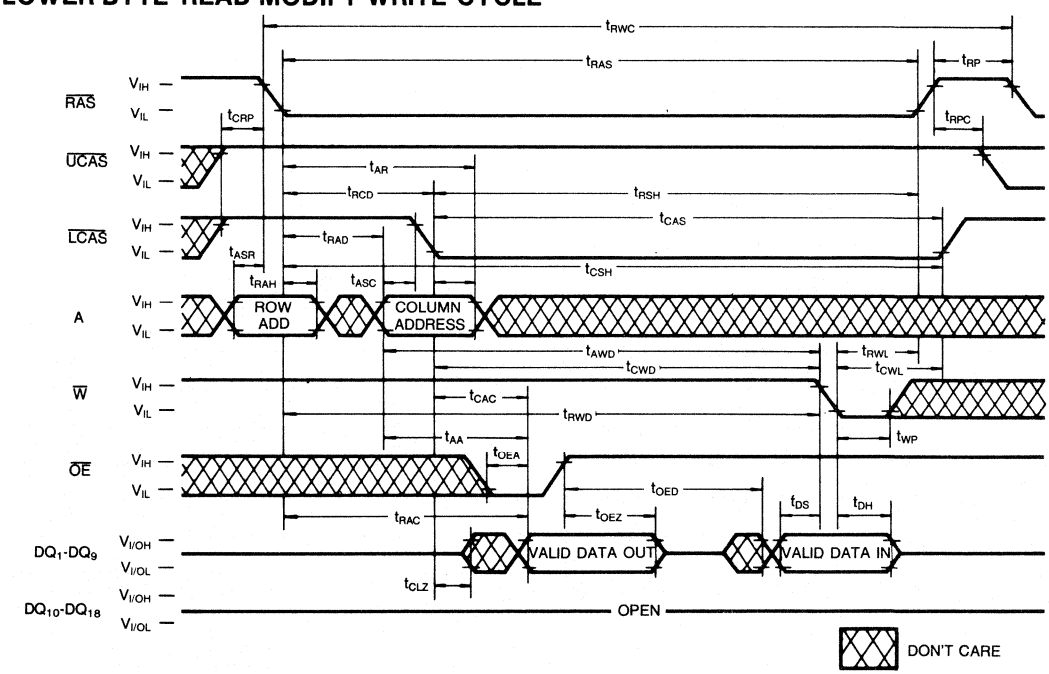


TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE

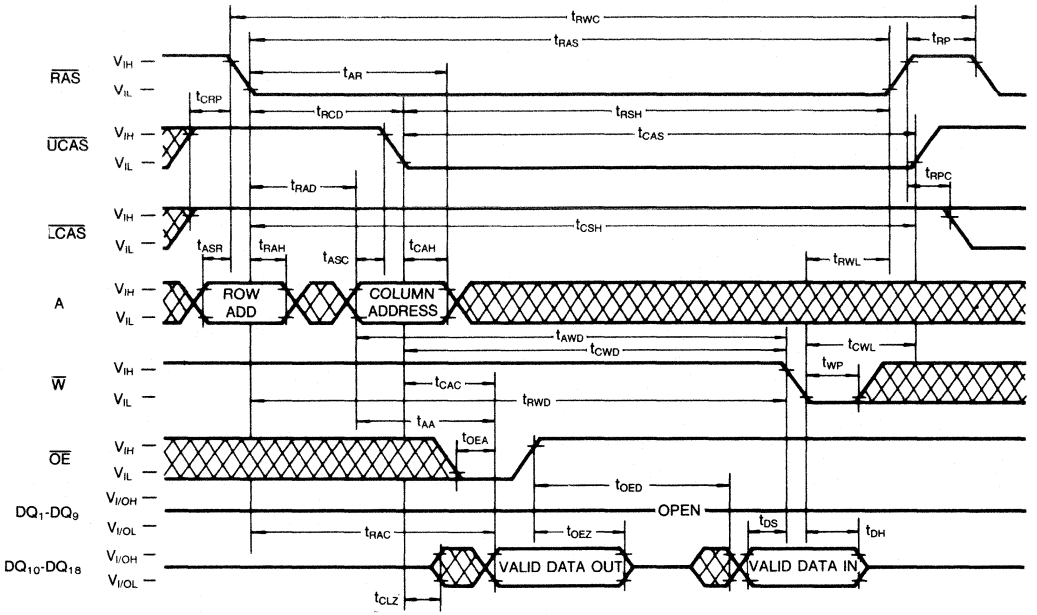


LOWER-BYTE READ-MODIFY-WRITE CYCLE

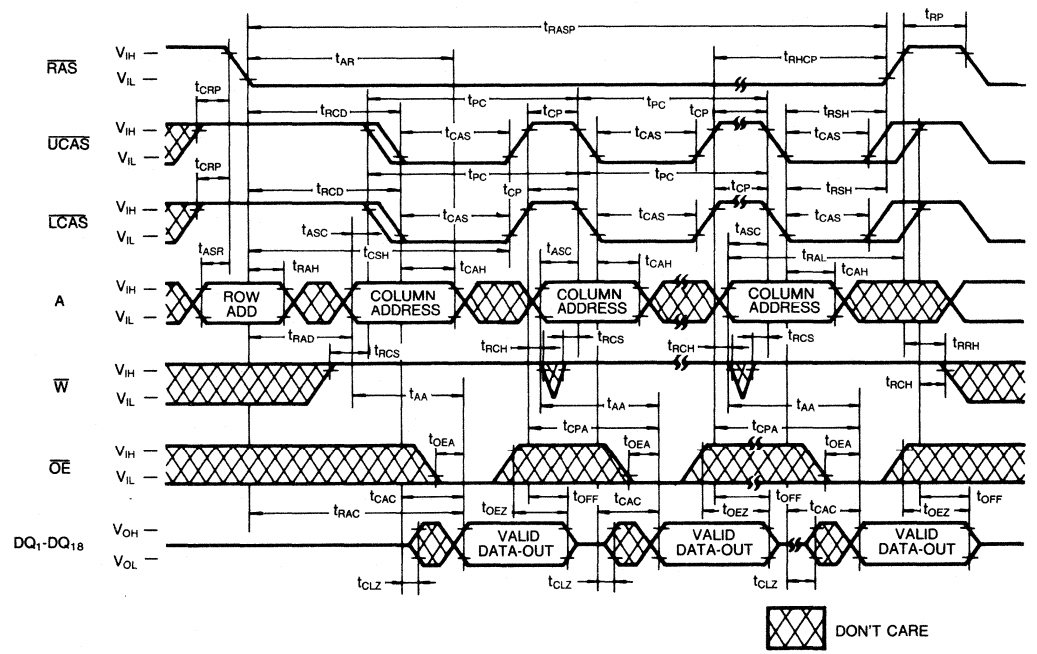


TIMING DIAGRAMS (Continued)

UPPER-BYTE READ-MODIFY-WRITE CYCLE

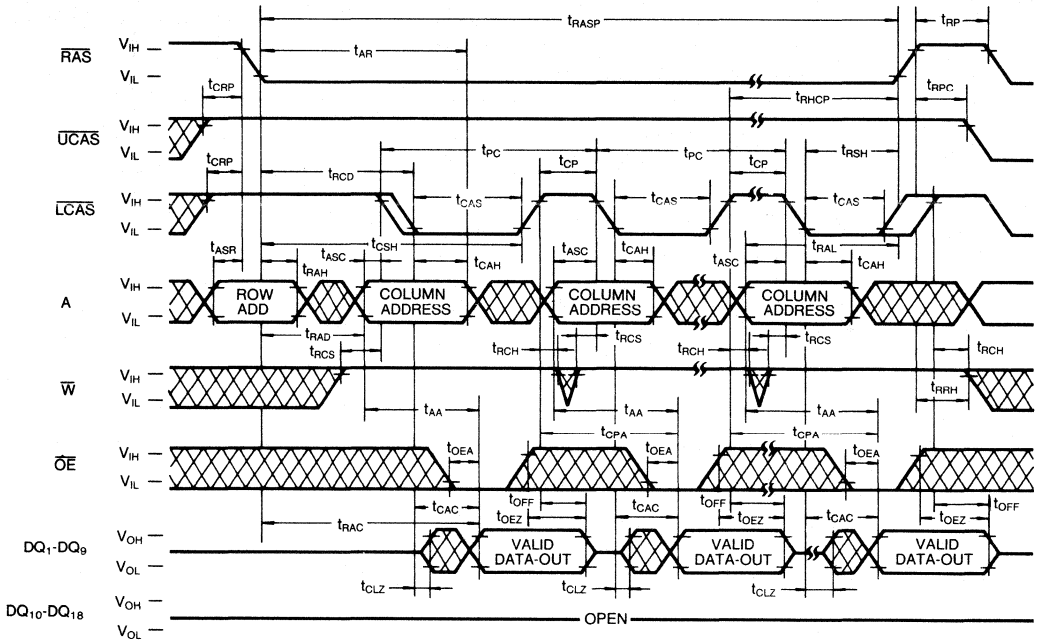


FAST PAGE MODE WORD READ CYCLE

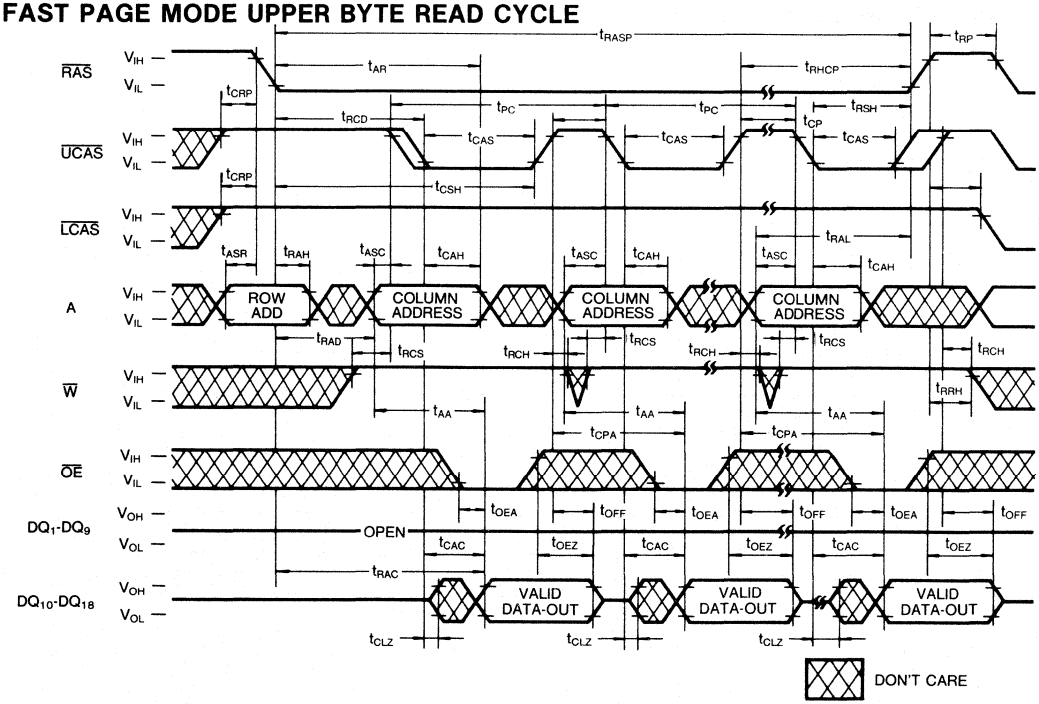


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE

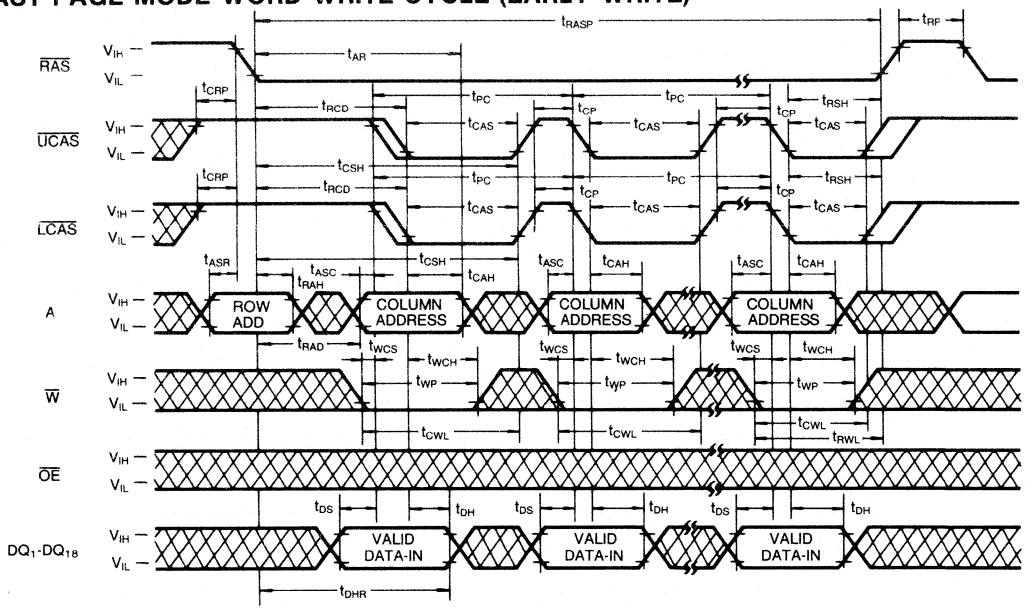


FAST PAGE MODE UPPER BYTE READ CYCLE

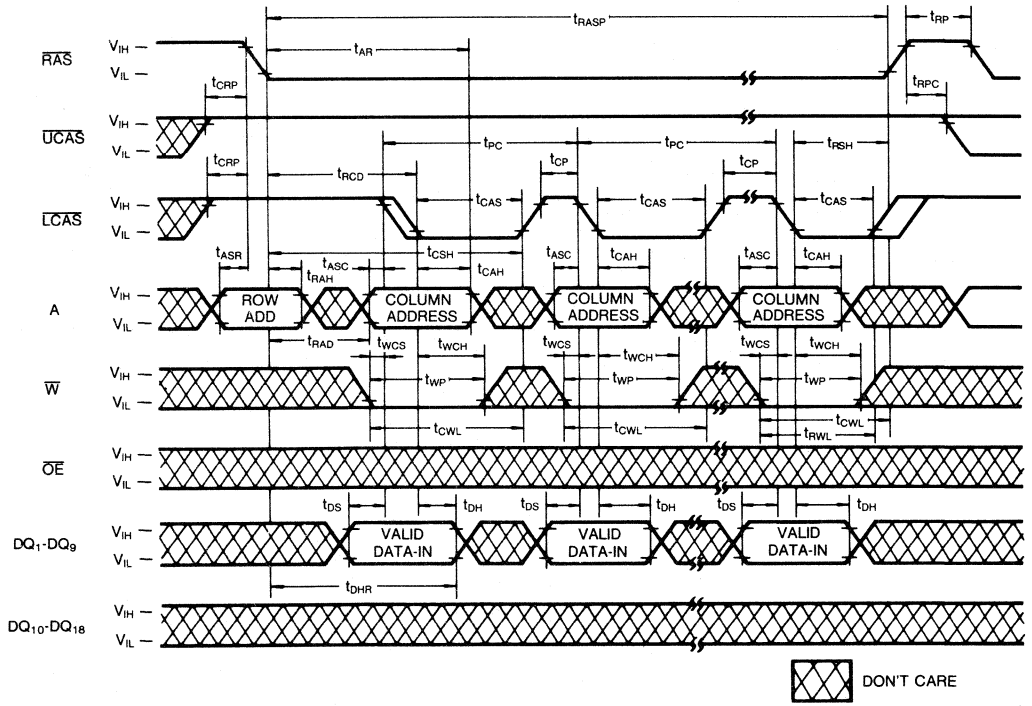


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

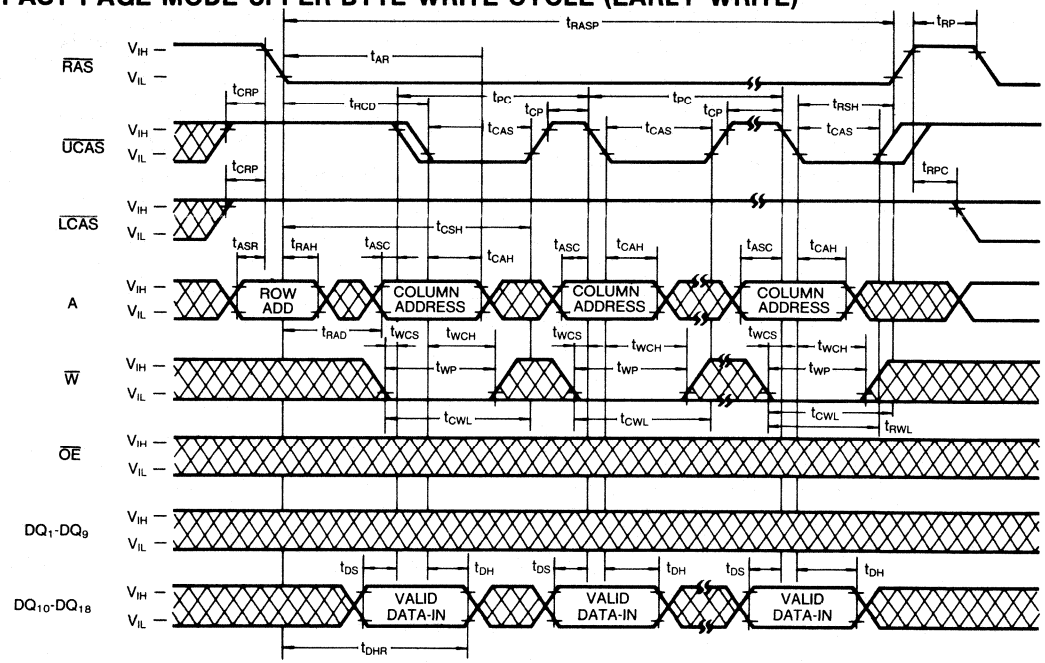


FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)

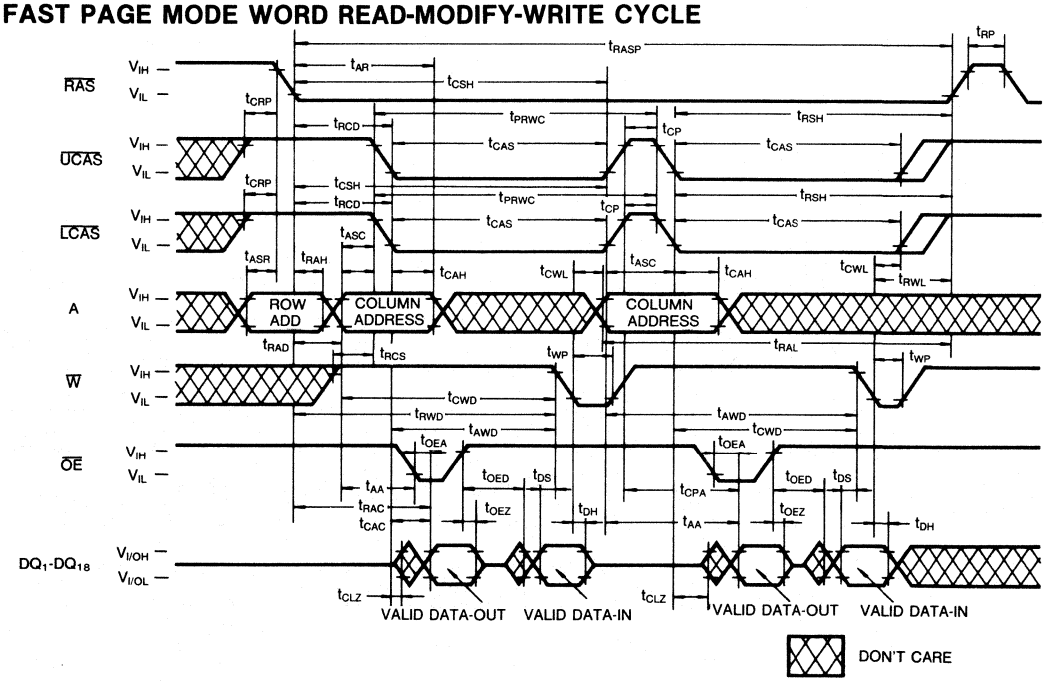


TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

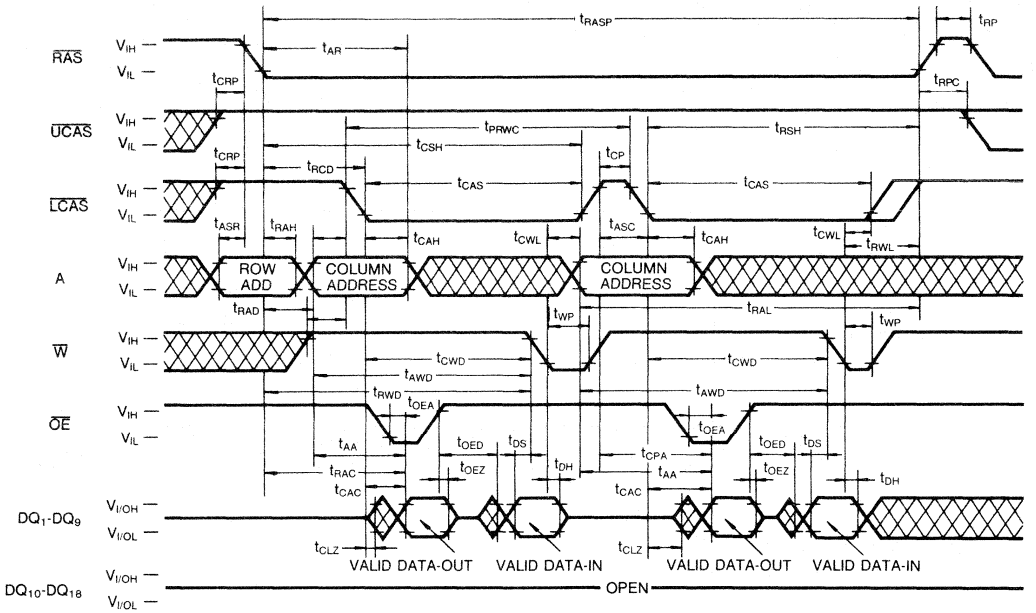


FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE

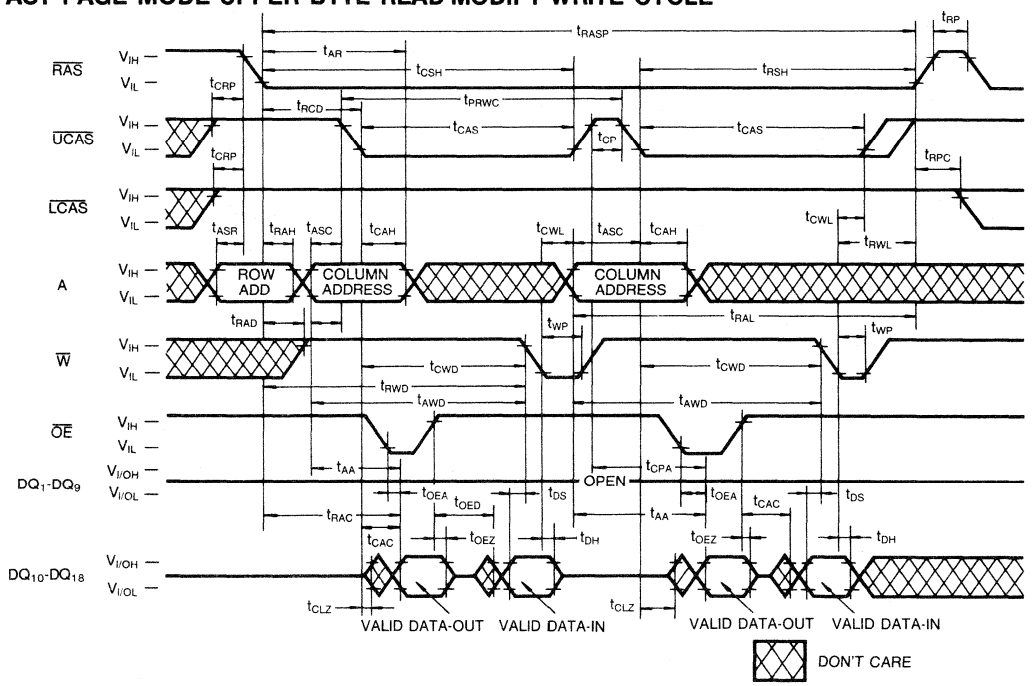


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ-MODIFY-WRITE CYCLE



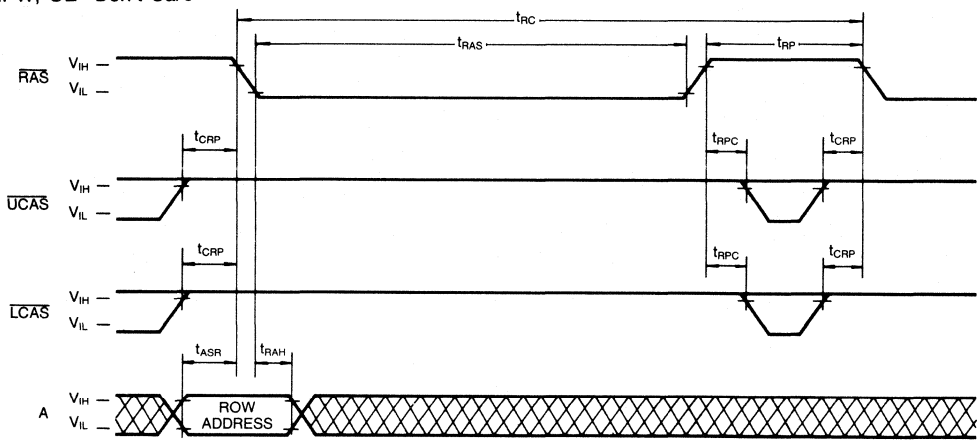
FAST PAGE MODE UPPER BYTE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

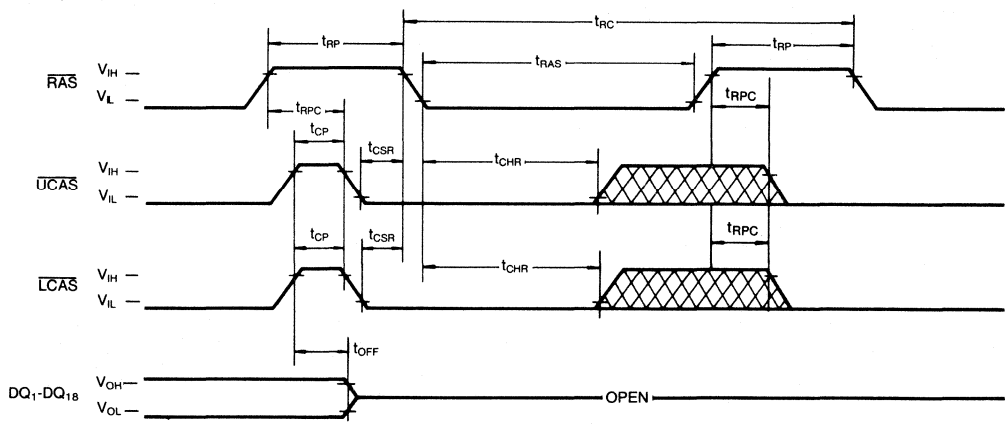
$\overline{RAS}$ ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$=Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

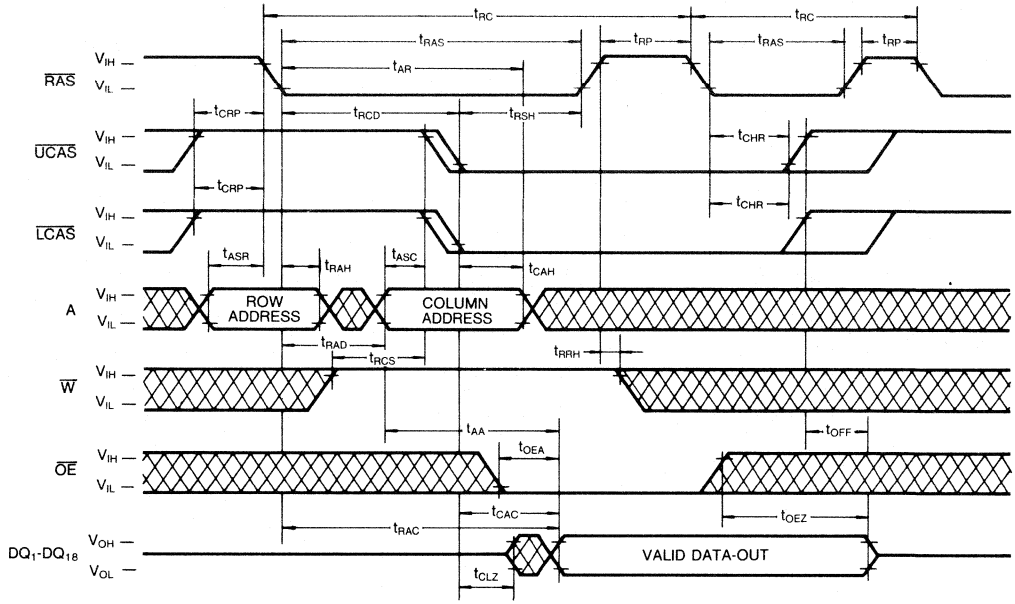
NOTE: W, OE, A = Don't Care



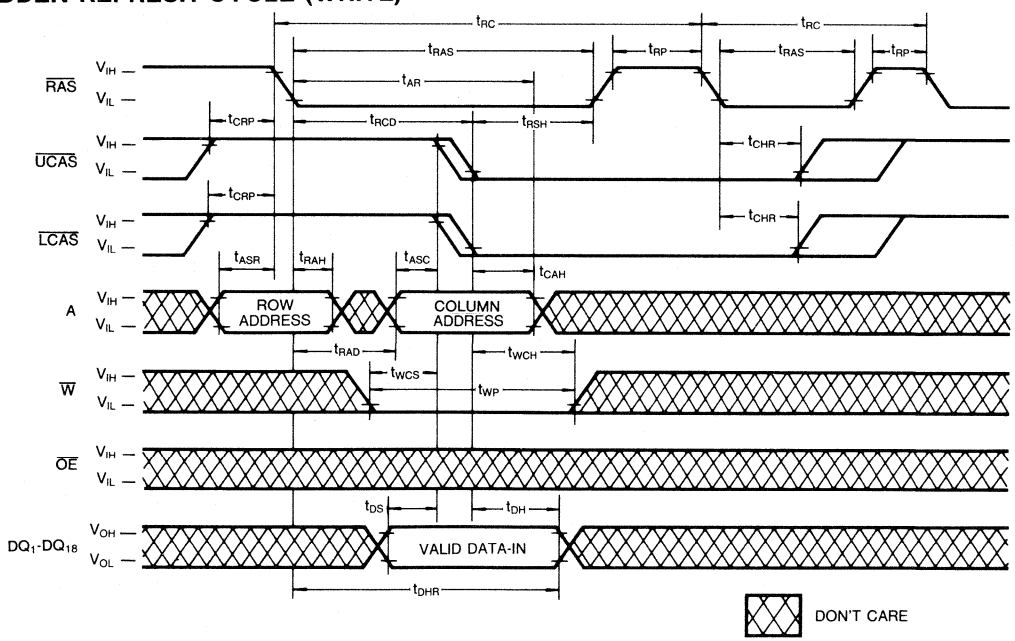
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

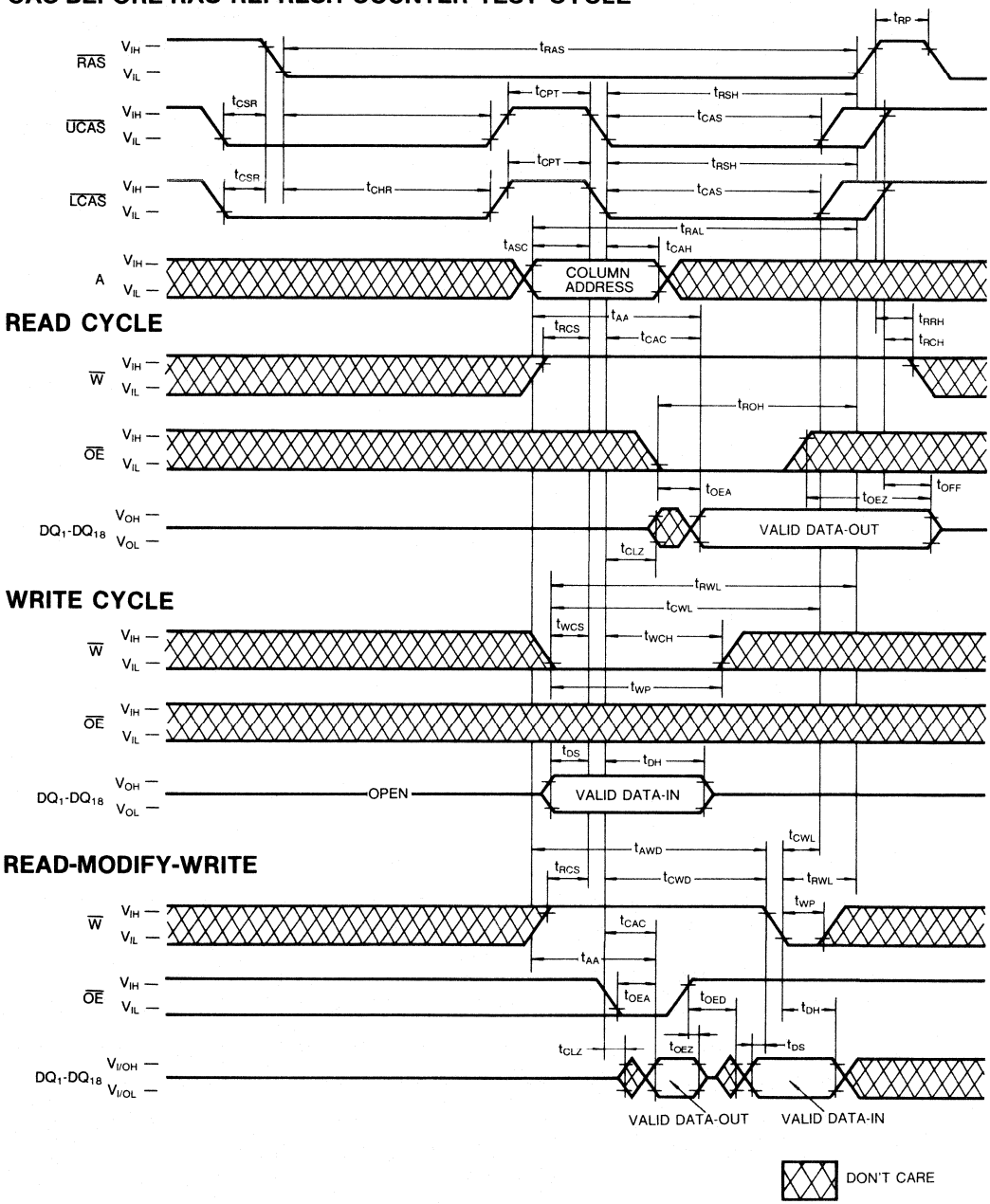


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM418C256/L/SL contains 4,718,592 memory locations arranged in 18 groups of 262,144 × 1 bit each. Eighteen address bits are required to address a particular memory location. Since the KM418C256/L/SL has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{LCAS}$, $\overline{UCAS}$) and the valid row and column address inputs.

Operation of the KM418C256/L/SL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{LCAS}$ ($\overline{UCAS}$) remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{LCAS}$ ($\overline{UCAS}$). This is the beginning of any KM418C256/L/SL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{LCAS}$ ($\overline{UCAS}$) have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM418C256/L/SL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{xCAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{xCAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{xCAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM418C256/L/SL can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$, $\overline{LCAS}$ and $\overline{UCAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{xCAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing W low before $\overline{xCAS}$. The 18-bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cells. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The $\overline{OE}$ input must be low during the time defined by t_{OEA} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM418C256/L/SL DQ pins.

Data Output

The KM418C256/L/SL has a three-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}), the outputs are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs enter into the low impedance state in the time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM418C256/L/SL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} times are not met)

DEVICE OPERATION (Continued)

Refresh

The data in the KM418C256/L/SL is stored as a charge on microscopic capacitor within each memory cell. The stored charge tends to dissipate over time and will affect data integrity if the charge is not periodically refreshed. Refresh of the individual storage cells is accomplished by accessing all rows within the refresh period (t_{REF}) off within 8ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row address (A0-A8).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM418C256/L/SL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If either $\overline{LCAS}$ or $\overline{UCAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ transitions low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending either $\overline{LCAS}$ or $\overline{UCAS}$ input active time and cycling $\overline{RAS}$. The hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM418C256/L/SL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM418C256/L/SL has Fast page mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is asserted high and then low again while $\overline{RAS}$ is asserted low, the read and write operations are enabled. In this method, the row address bits A0 through A8 are supplied by on chip refresh counter.

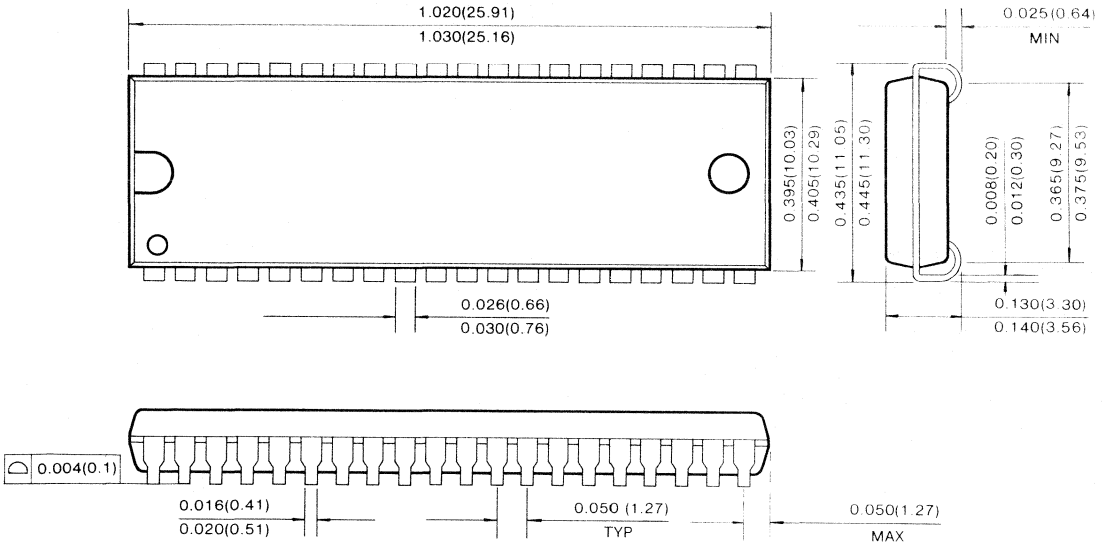
Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM418C256/L/SL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held a valid V_{IH} in order to minimize the power-up current.

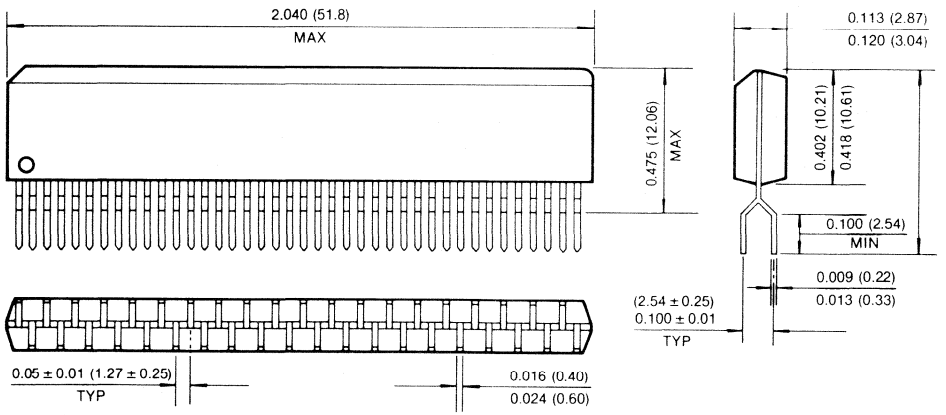
PACKAGE DIMENSION

40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



40-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



256K x 18 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM418C256LL-7	70ns	20ns	130ns
KM418C256LL-8	80ns	20ns	150ns
KM418C256LL-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Self refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Triple +5V ± 10% power supply**
- **Refresh Cycle**
  - **512 cycle/128ms (self-refresh)**
- **Power Dissipation**
  - **Standby: 11mW (Normal)**
    0.55mW (self-refresh)
  - **Active (70/80/100): 825/715/605mW**
- **JEDEC Standard pinout**
- **Available in Plastic SOJ and ZIP**

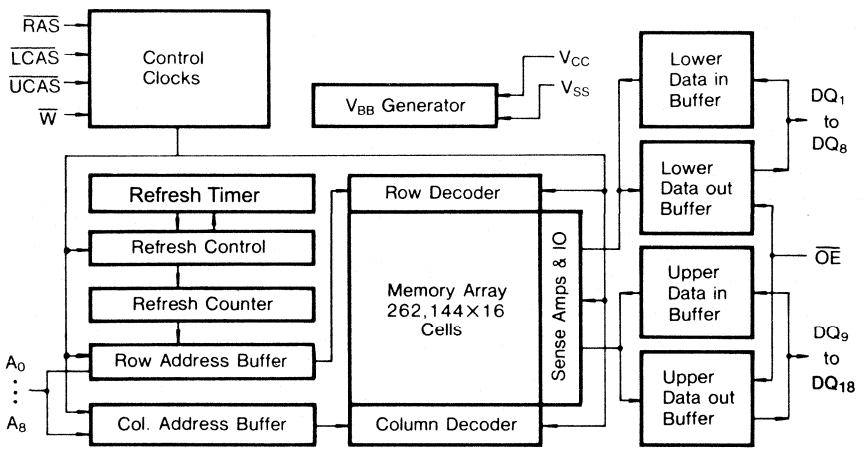
GENERAL DESCRIPTION

The Samsung KM418C256LL is a CMOS high speed 262,144 bit x 18 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM418C256LL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

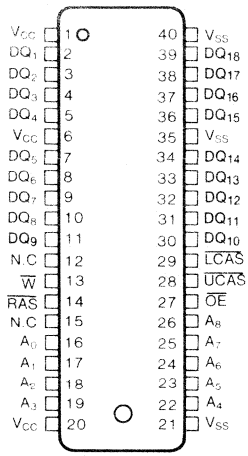
The KM418C256LL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



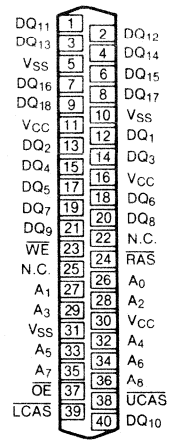
PIN CONFIGURATION (Top Views)

• KM418C256LLJ



(SOJ)

• KM418C256LLZ



(ZIP)

Pin Name	Pin Function	Pin Name	Pin Function
A_0-A_8	Address Inputs	$\overline{LCAS}$	Lower Column Address Strobe
DQ_{1-18}	Data In/Out	$\overline{W}$	Read/Write Input
V_{SS}	Ground	$\overline{OE}$	Data Output Enable
$\overline{RAS}$	Row Address Strobe	V_{CC}	Power (+5V)
$\overline{UCAS}$	Upper Column Address Strobe	N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage refer ce to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$, or $\overline{LCAS}$, Address Cycling @t_{RC} = min.)	KM418C256LL-7	I_{CC1}	—	150	mA
	KM418C256LL-8		—	130	mA
	KM418C256LL-10		—	110	mA
Standby Current ($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$ = $\overline{LCAS}$, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM418C256LL-7	I_{CC3}	—	150	mA
	KM418C256LL-8		—	130	mA
	KM418C256LL-10		—	110	mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{PC} = min.)	KM418C256LL-7	I_{CC4}	—	90	mA
	KM418C256LL-8		—	80	mA
	KM418C256LL-10		—	70	mA
Standby Current ($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ ≥ V_{CC} − 0.2V)		I_{CC5}	—	100	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @t_{RC} = min.)	KM418C256LL-7	I_{CC6}	—	150	mA
	KM418C256LL-8		—	130	mA
	KM418C256LL-10		—	110	mA
Self Refresh Current $\overline{RAS}$ = $\overline{CAS}$ = V_{IL} $\overline{WE}$ = $\overline{OE}$ = A0 ~ A8 = V_{CC}-0.2V or 0.2V DQ1 ~ 18 = V_{CC}-0.2V, 0.2V or OPEN		I_{CC5}	—	200	μA
Input Leakage Current (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$ = V_{IL}. In I_{CC4}, Address can be changed maximum once while $\overline{UCAS}$ and $\overline{UCAS}$ = V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_8)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_{18})	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1, 2)

Parameter	Symbol	KM418C256LL-7		KM418C256LL-8		KM418C256LL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	180		200		240		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	55	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command set-up time	t_{WCS}	0		0		0		ns	8
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	

AC CHARACTERISTICS (Continued)

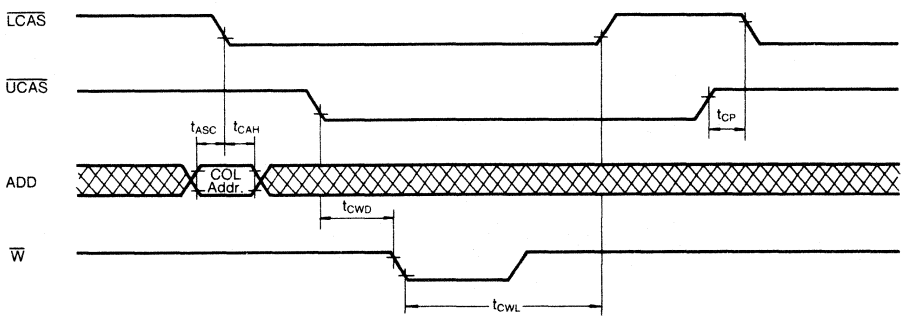
Parameter	Symbol	KM418C256LL-7		KM418C256LL-8		KM418C256LL-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (self-version)	t_{REF}		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	45		45		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	95		105		130		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	60		65		75		ns	8
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge time (C-B-R counter test cycle)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3
Fast page mode cycle time	t_{PC}	45		50		55		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	95		100		115		ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
Access time from $\overline{OE}$	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data-in delay time	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	
$\overline{RAS}$ pulse width (C-B-R self refresh)	t_{RASS}	100		100		100		μs	
$\overline{RAS}$ precharge time (C-B-R self refresh)	t_{RPS}	130		150		180		ns	
$\overline{CAS}$ hold time (C-B-R self refresh)	t_{CHS}	0		0		0		ns	

KM418C256 Truth Table

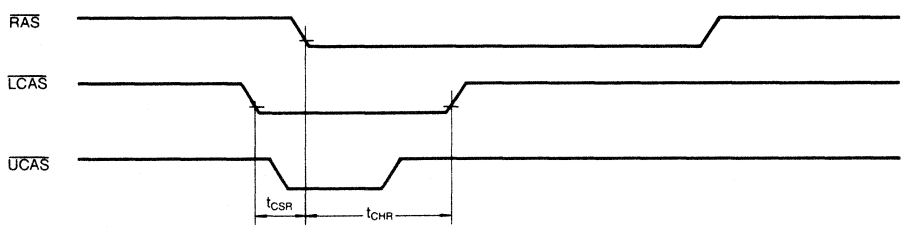
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	$DQ_{1\sim9}$	$DQ_{10\sim18}$	State
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Lower Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-In	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	—

NOTES

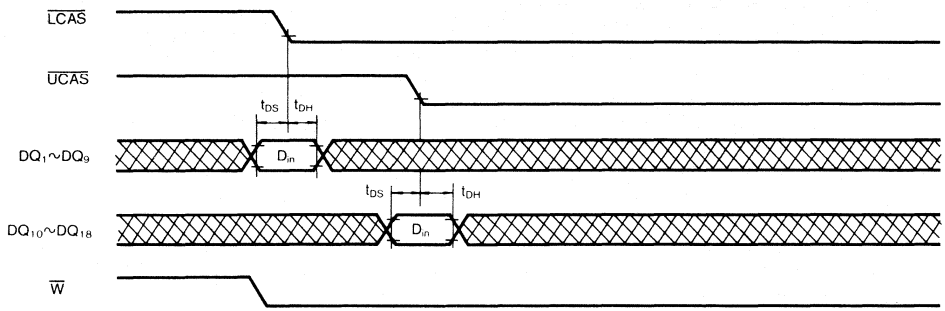
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating aprameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
17. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.

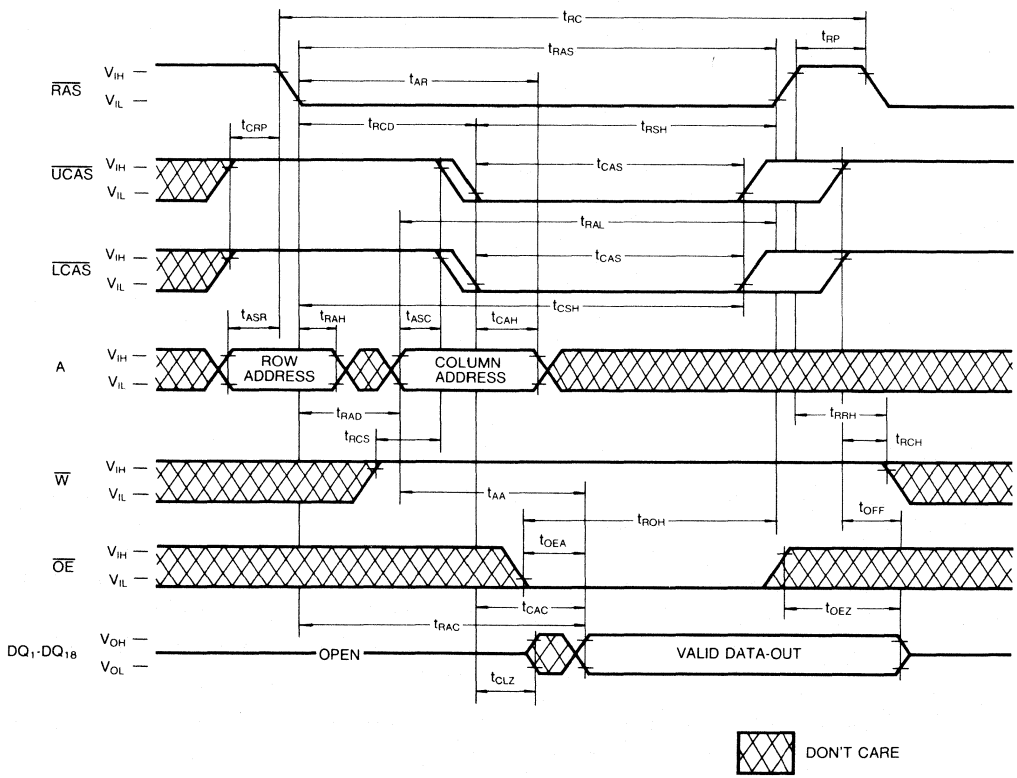


18. t_{DS}, t_{DH} is independetly specified for lower byte $D_{in(1\sim9)}$, upper byte $D_{in(10\sim18)}$.



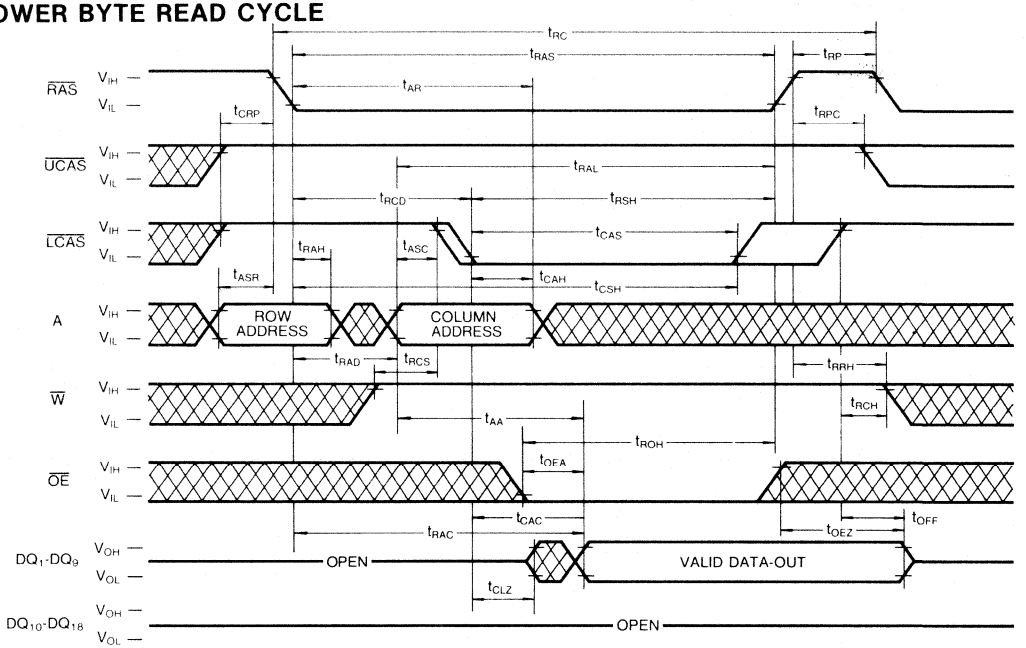
TIMING DIAGRAMS

WORD READ CYCLE

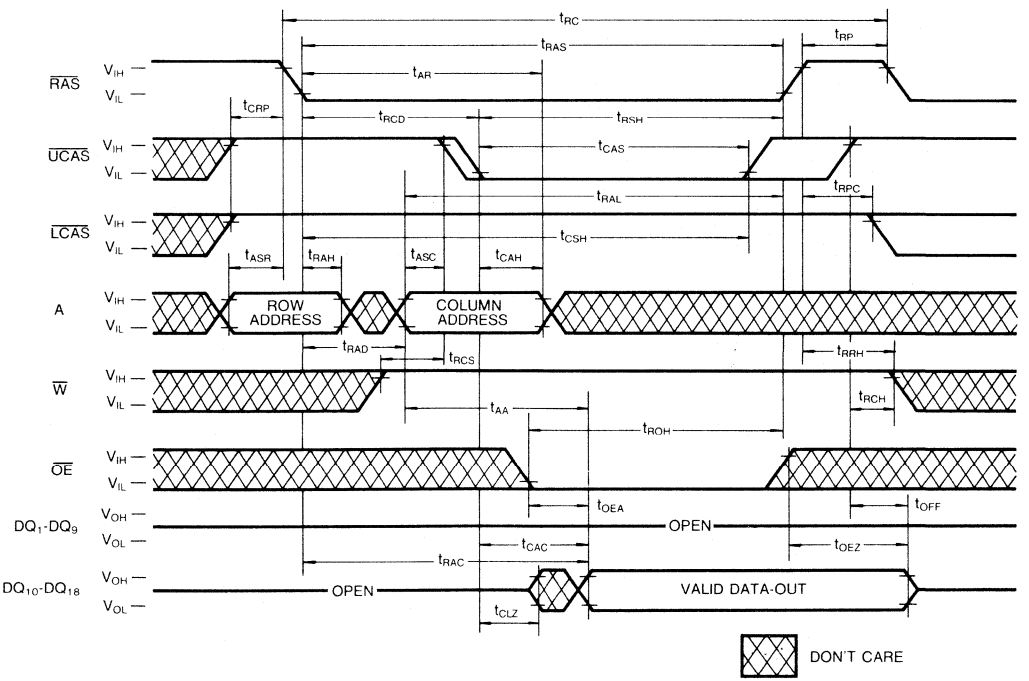


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE

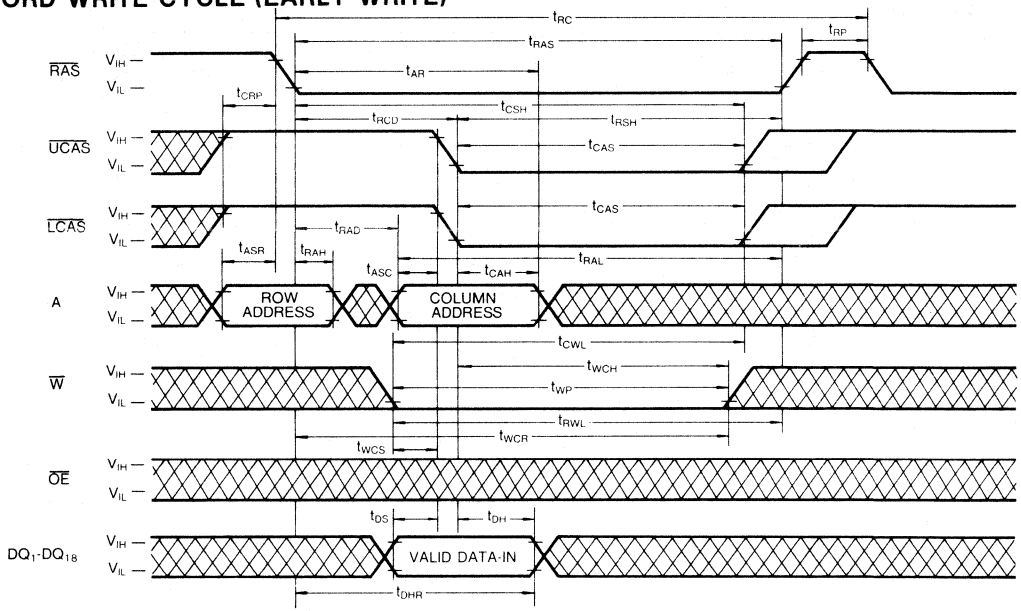


UPPER BYTE READ CYCLE

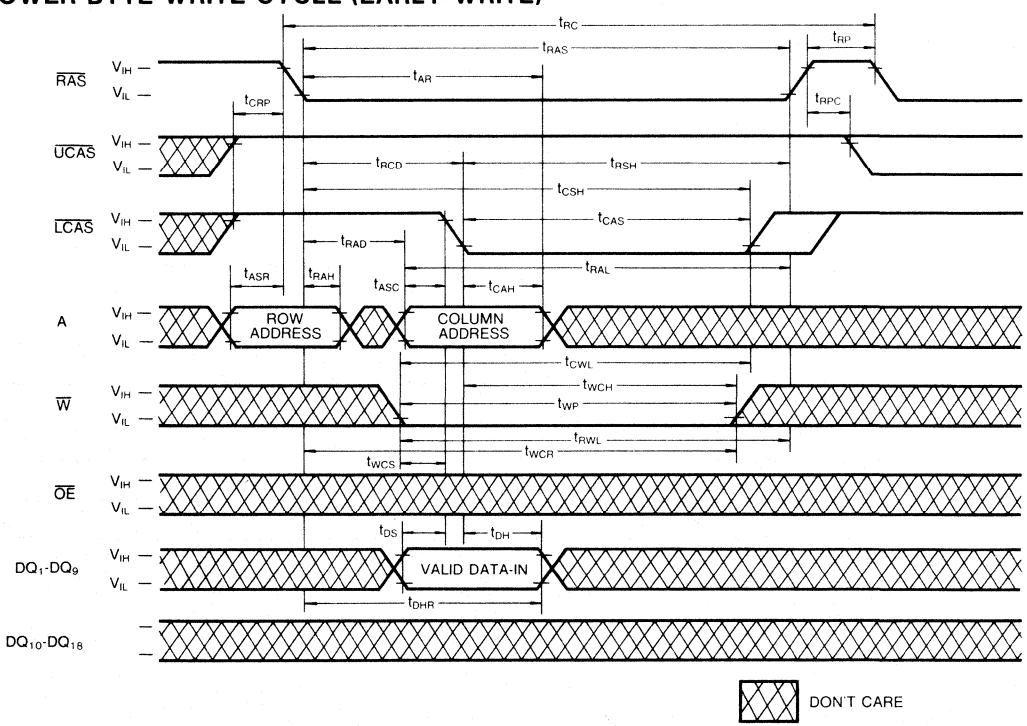


TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)

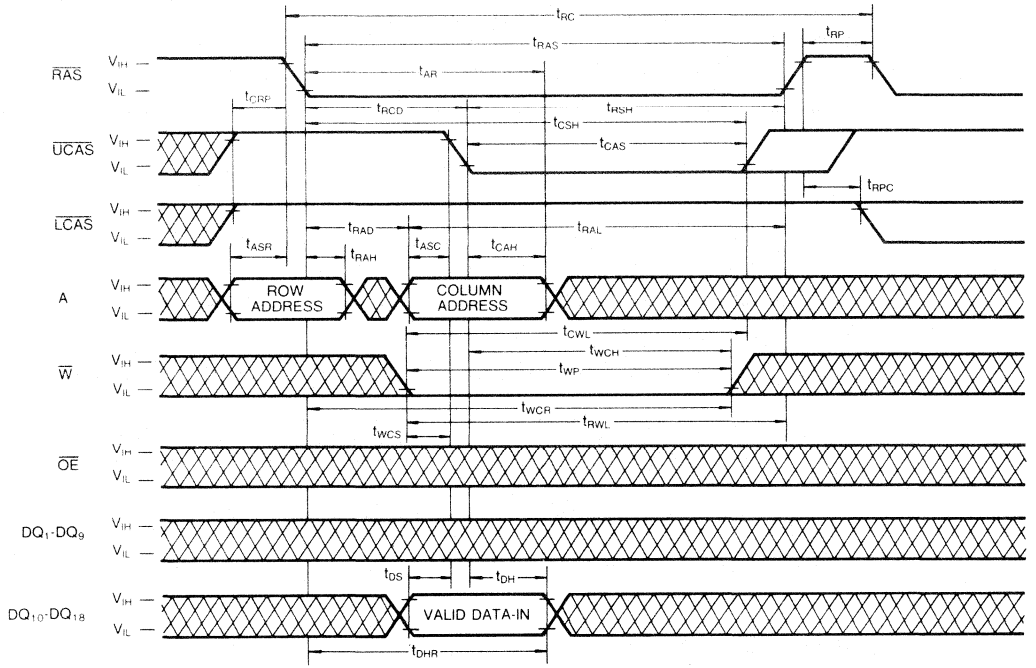


LOWER BYTE WRITE CYCLE (EARLY WRITE)

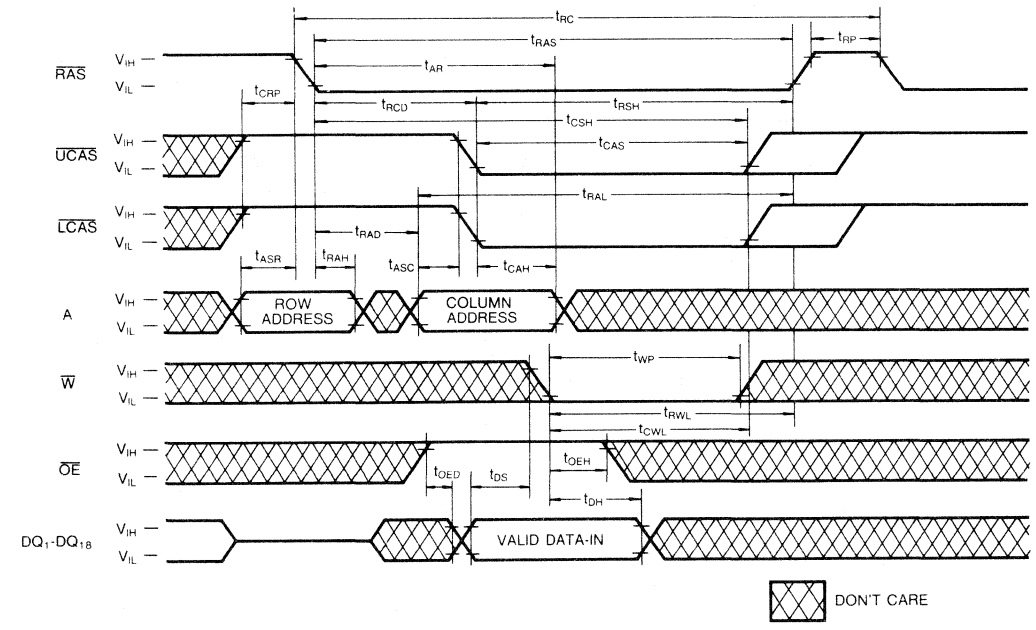


TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)

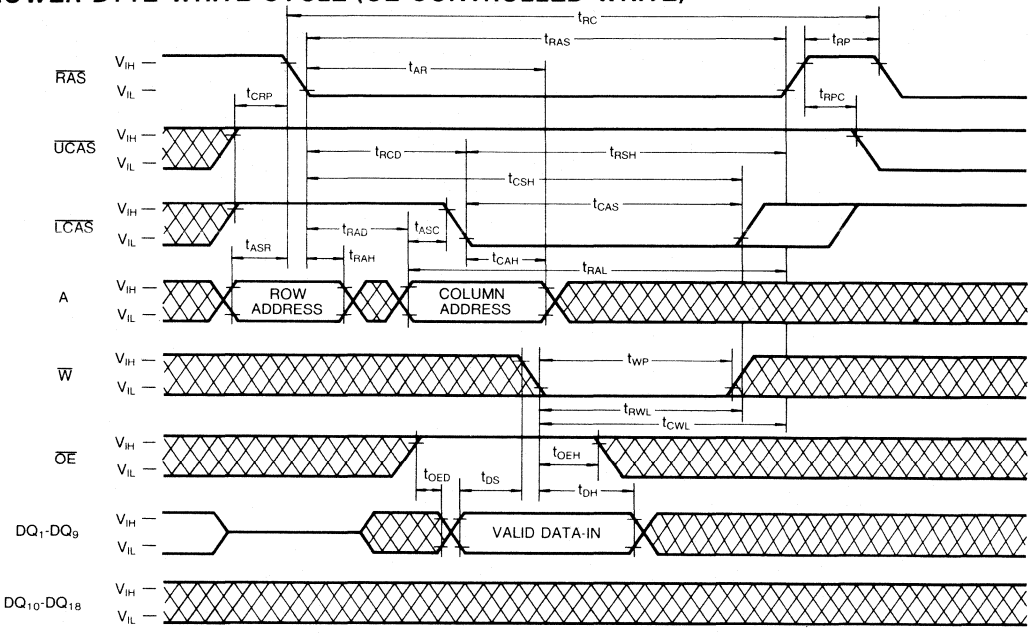


WORD WRITE CYCLE (OE CONTROLLED WRITE)

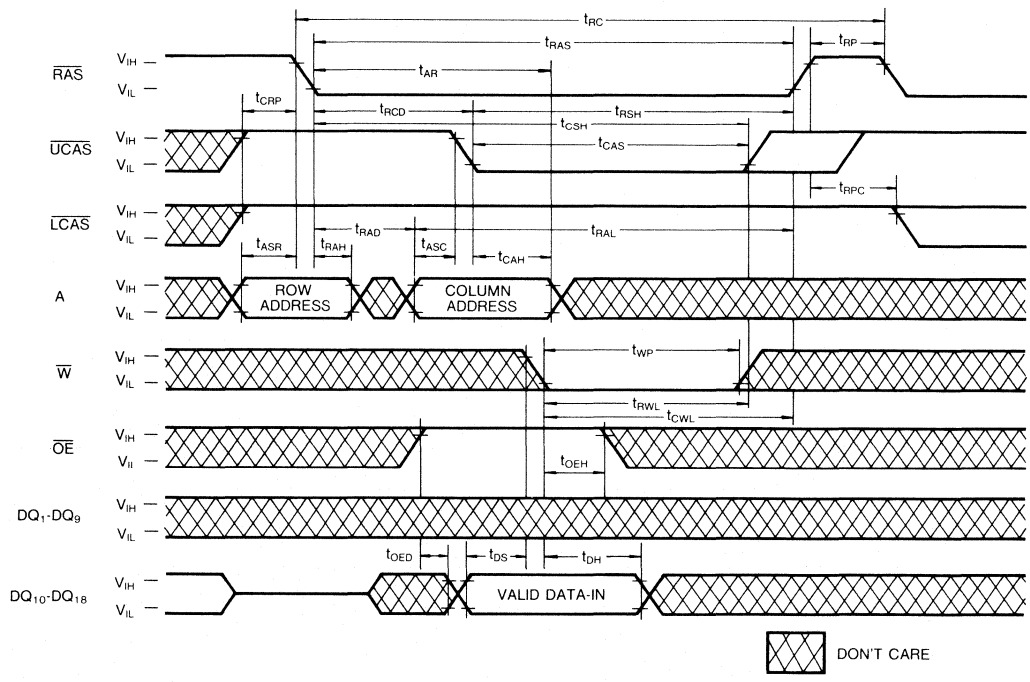


TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

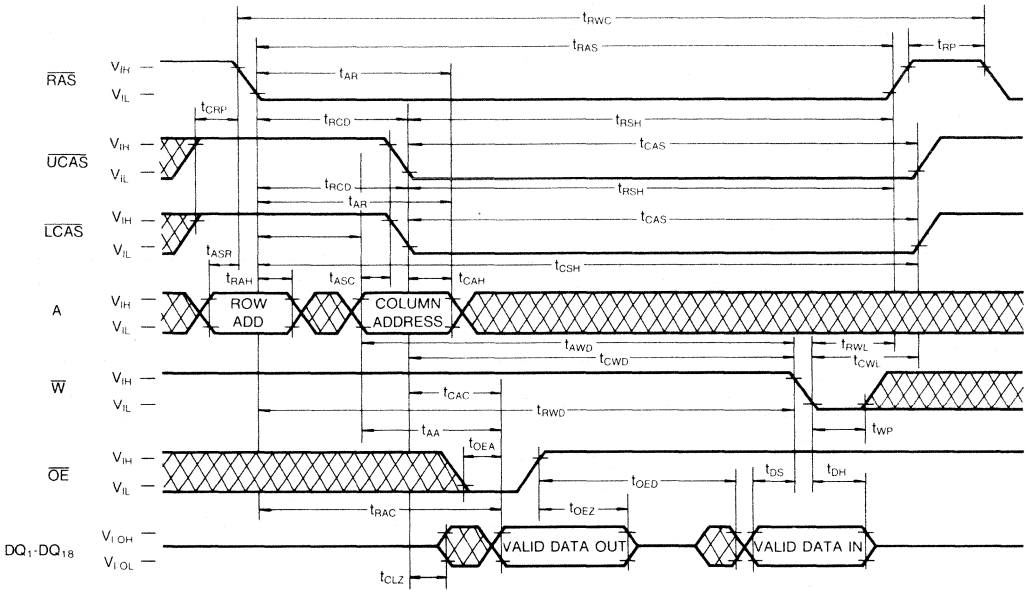


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

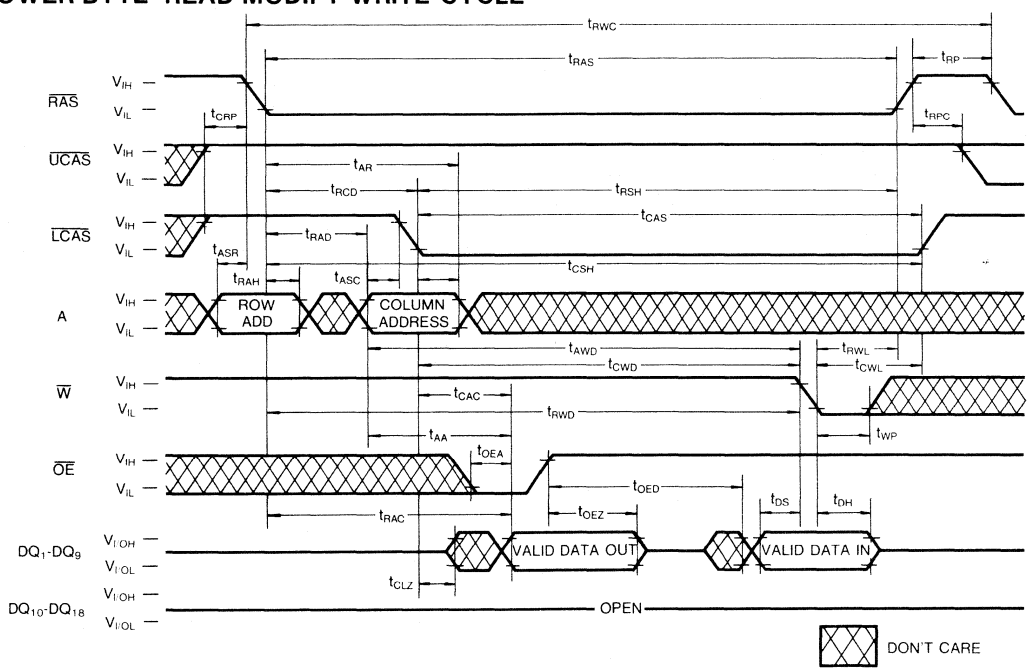


TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE

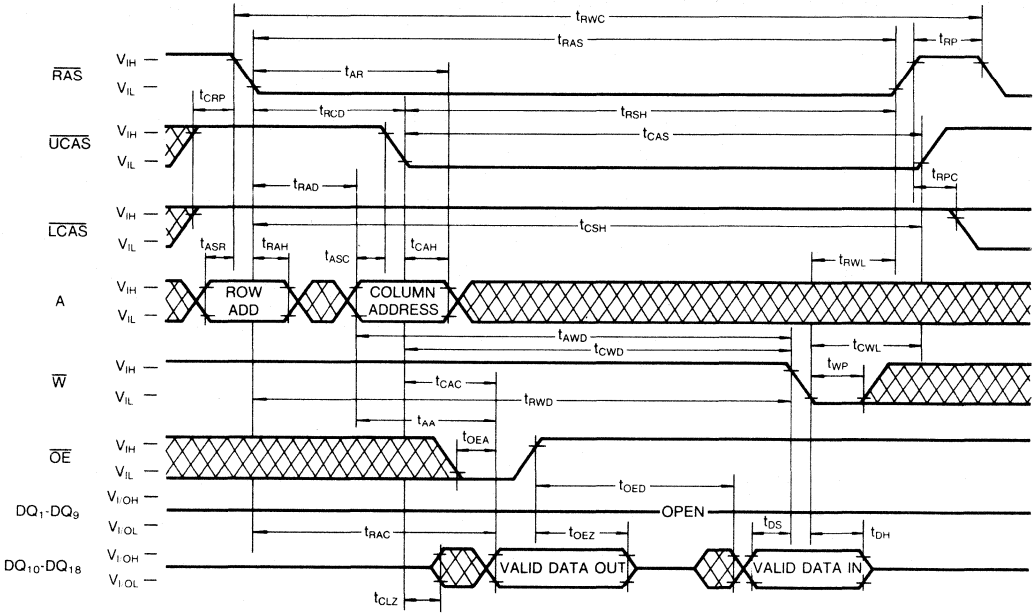


LOWER-BYTE READ-MODIFY-WRITE CYCLE

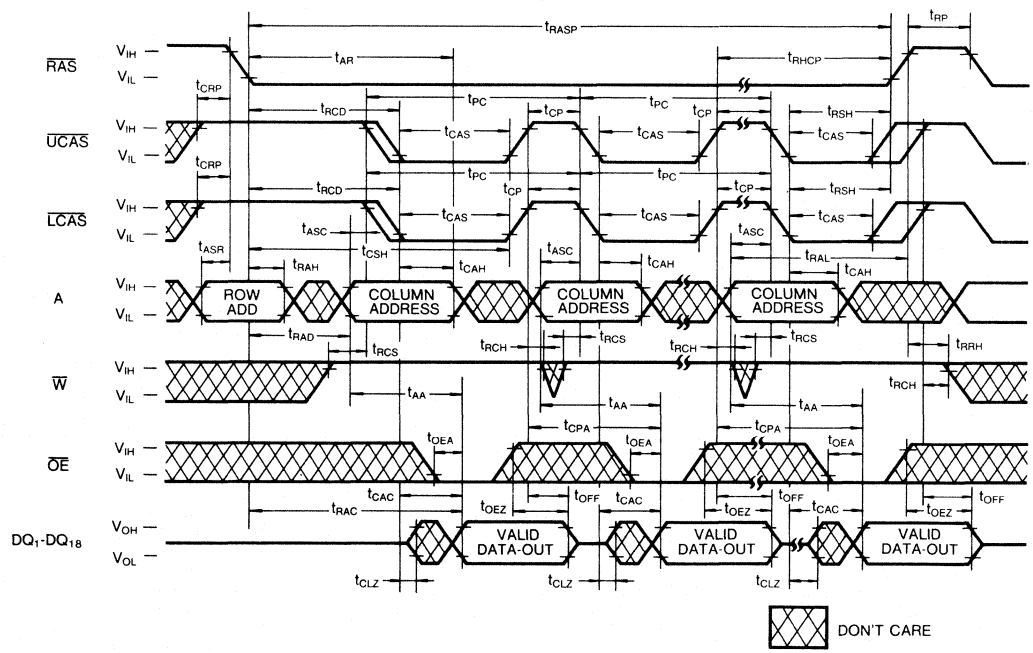


TIMING DIAGRAMS (Continued)

UPPER-BYTE READ-MODIFY-WRITE CYCLE

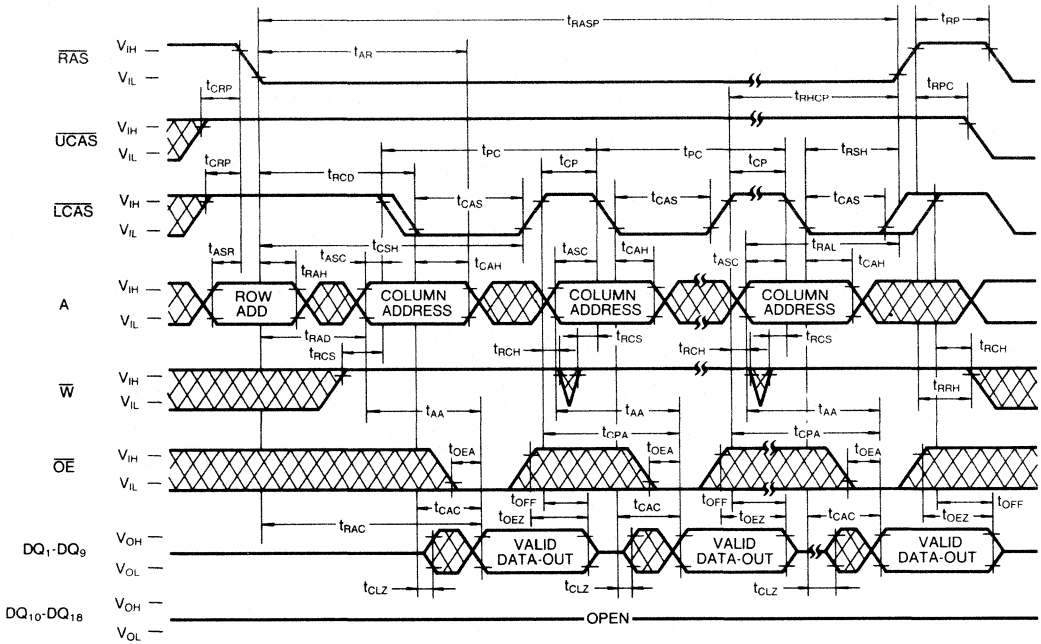


FAST PAGE MODE WORD READ CYCLE

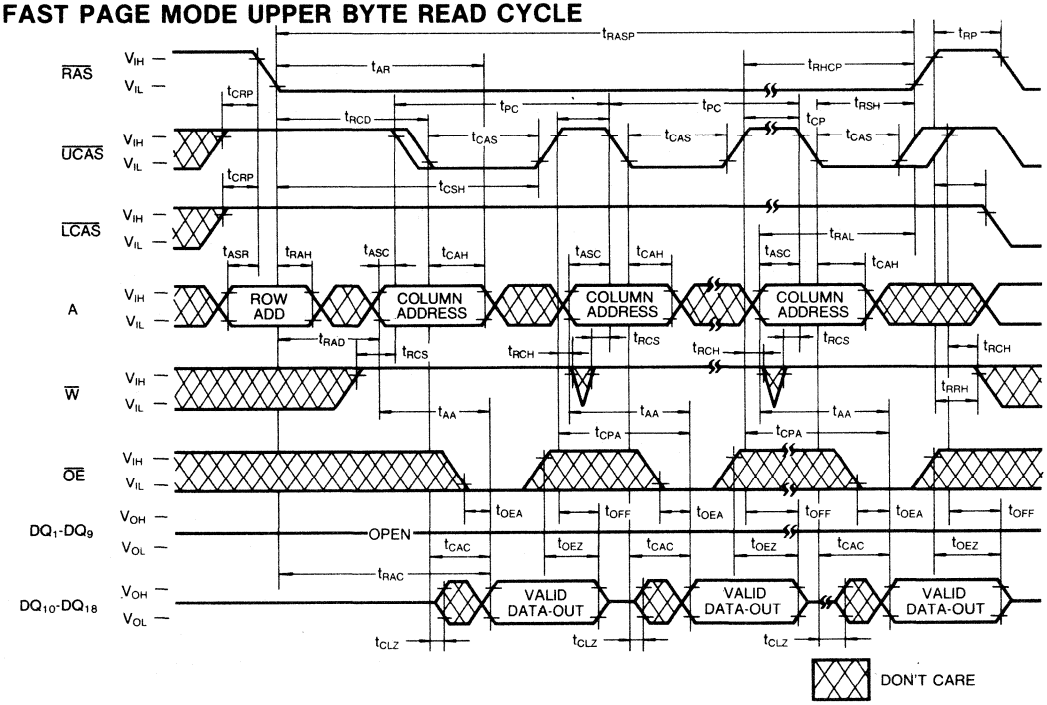


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE

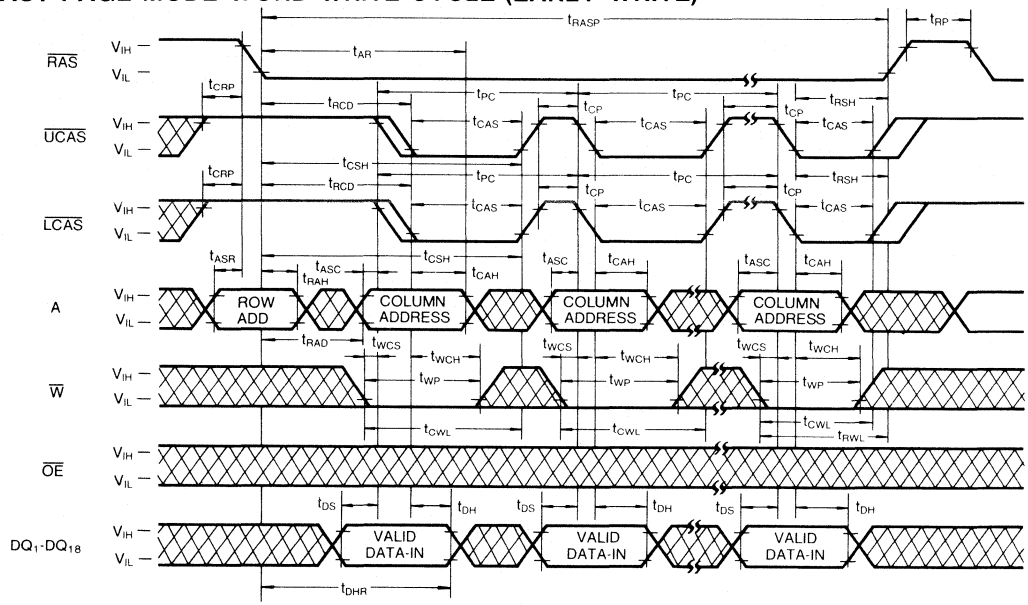


FAST PAGE MODE UPPER BYTE READ CYCLE

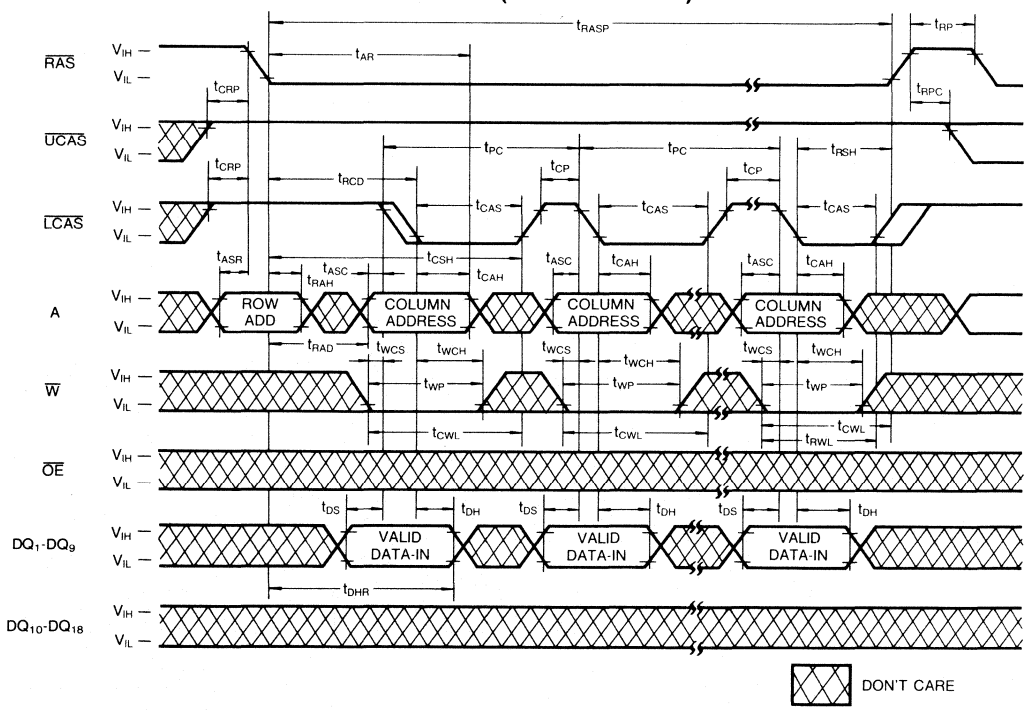


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

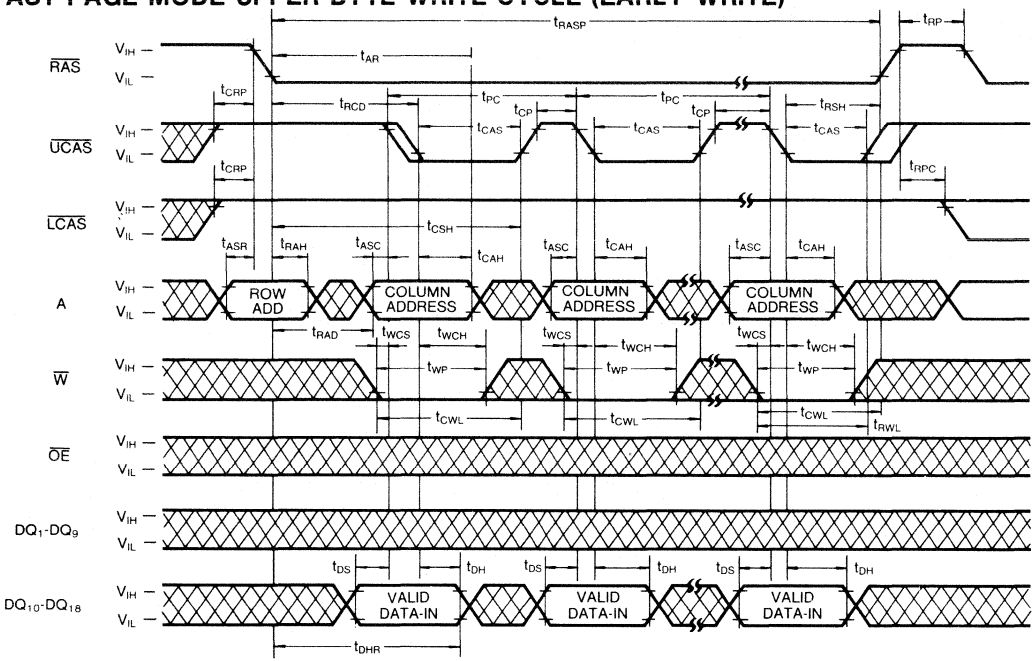


FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)

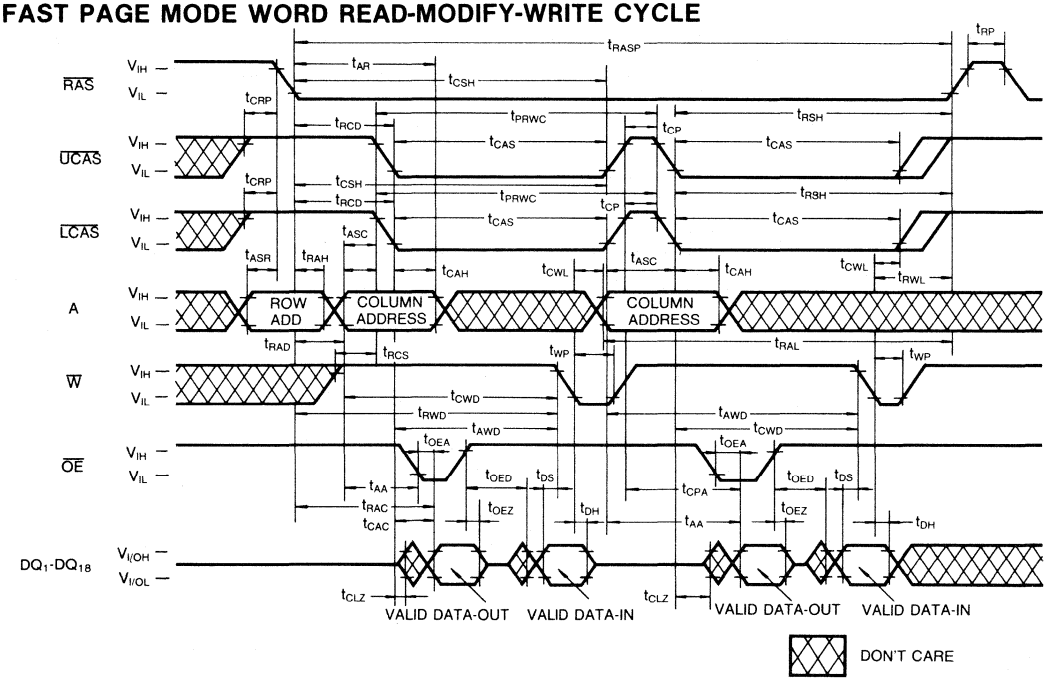


TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

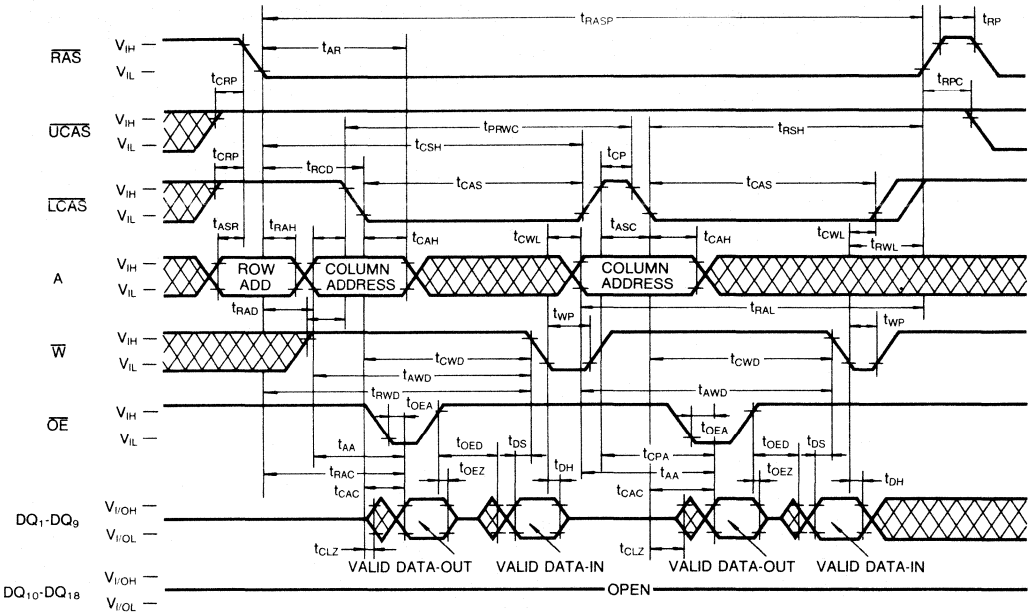


FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE

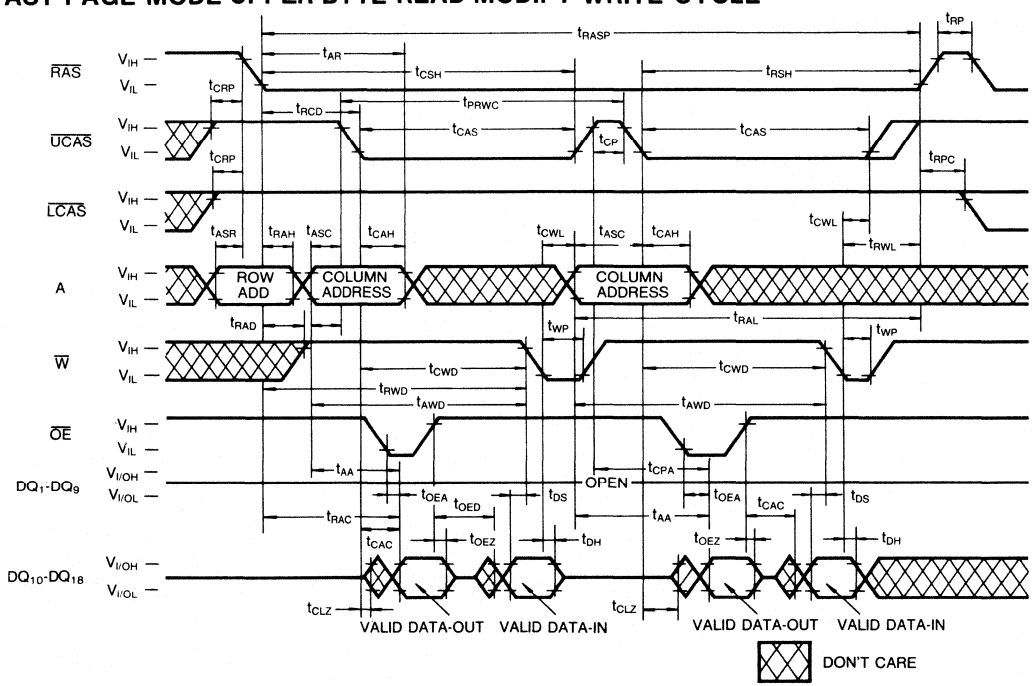


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER-BYTE READ-MODIFY-WRITE CYCLE



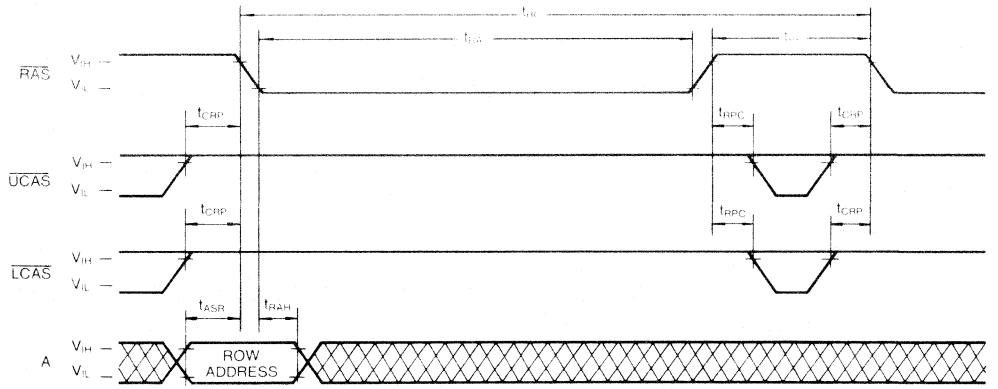
FAST PAGE MODE UPPER-BYTE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

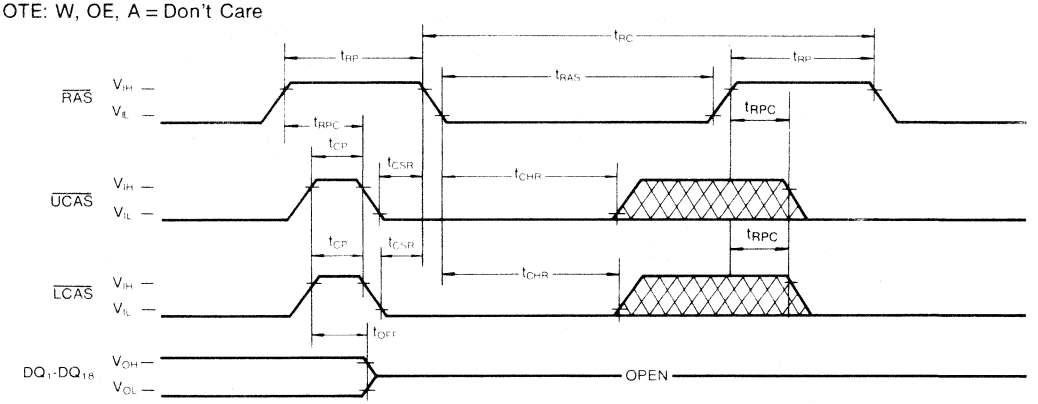
$\overline{RAS}$ ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$=Don't Care



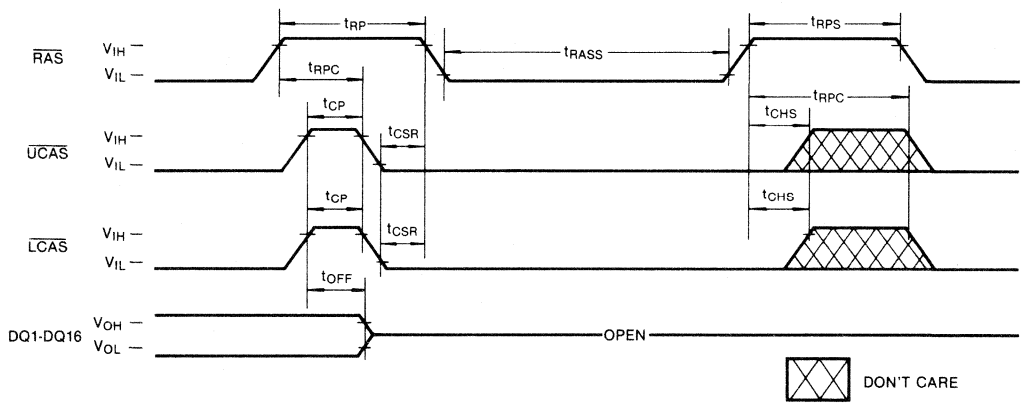
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: W, OE, A = Don't Care



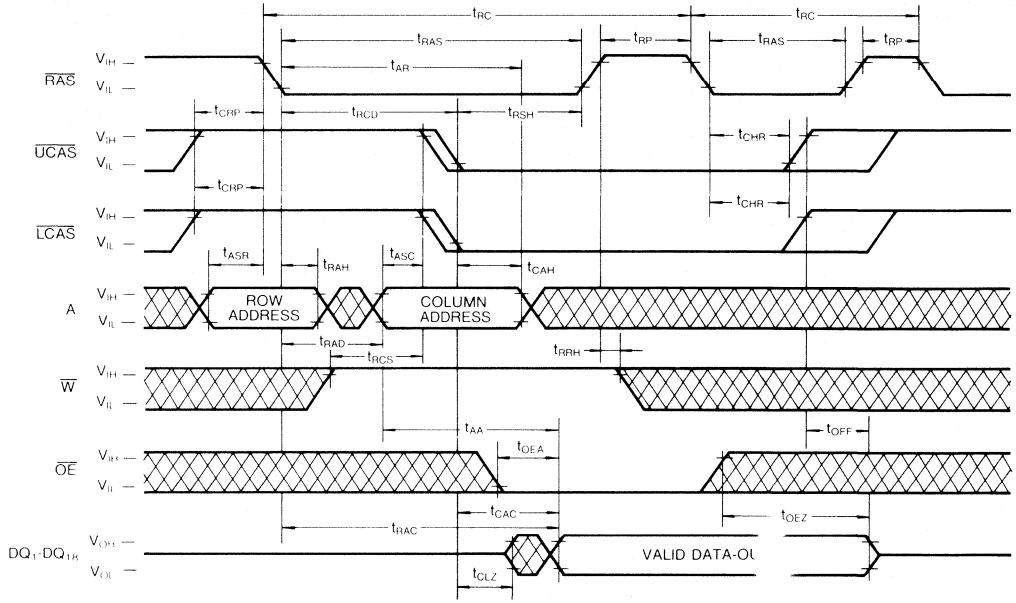
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$, A = Don't Care

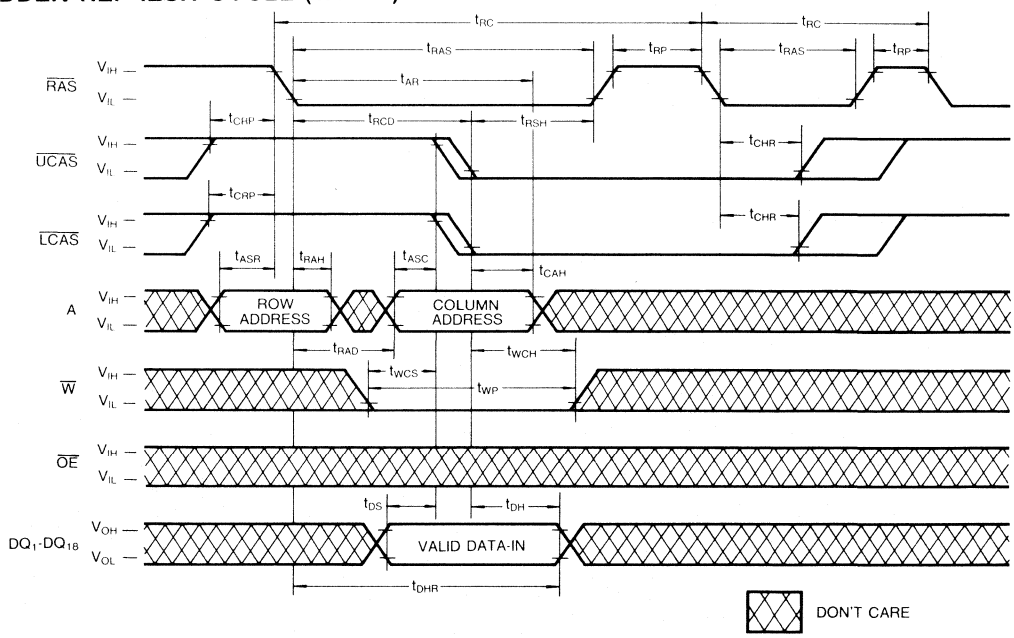


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

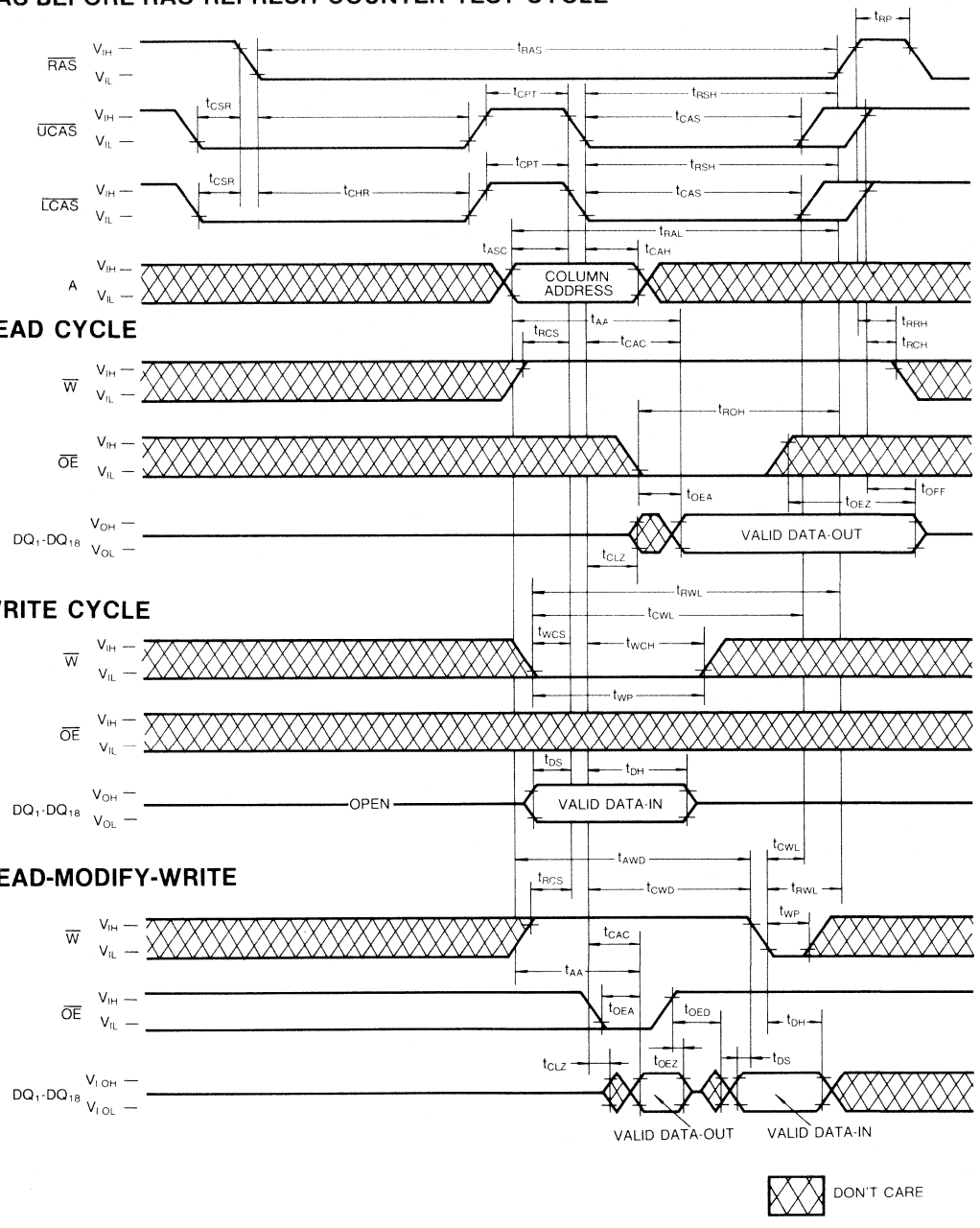


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM418C256LL contains 4,718,592 memory locations arranged in 18 groups of 262,144 × 1 bit each. Eighteen address bits are required to address a particular memory location. Since the KM418C256LL has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{LCAS}$, $\overline{UCAS}$) and the valid row and column address inputs.

Operation of the KM418C256LL begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{LCAS}$ ($\overline{UCAS}$) remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{LCAS}$ ($\overline{UCAS}$). This is the beginning of any KM418C256LL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{LCAS}$ ($\overline{UCAS}$) have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM418C256LL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/x$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If x$\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if x$\overline{CAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM418C256LL can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$, $\overline{LCAS}$ and $\overline{UCAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or x$\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before x$\overline{CAS}$. The 18-bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cells. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The $\overline{OE}$ input must be low during the time defined by t_{OEA} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM418C256LL DQ pins.

Data Output

The KM418C256LL has a three-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}), the outputs are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs enter into the low impedance state in the time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM418C256LL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} times are not met)

DEVICE OPERATION (Continued)

Refresh

The data in the KM418C256LL is stored as a charge on microscopic capacitor within each memory cell. The stored charge tends to dissipate over time and will affect data integrity if the charge is not periodically refreshed. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 512 row address (A0-A8).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM418C256LL has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{LCAS}$ or $\overline{UCAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ transitions low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending either $\overline{LCAS}$ or $\overline{UCAS}$ input active time and cycling $\overline{RAS}$. The hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Self Refresh: The self refresh is $\overline{CAS}$-before-$\overline{RAS}$ refresh to be used for long periods of standby, such as a battery back-up. In normal $\overline{CAS}$-before-$\overline{RAS}$ condition, when $\overline{RAS}$ is held low above 100μs an internal timer activates an refresh operation of consecutive row addresses in DRAM. The self refresh mode is exited when either $\overline{RAS}$ or $\overline{CAS}$ goes high(V_{IH}).

Other Refresh Methods: It is also possible to refresh the KM418C256LL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM418C256LL has Fast page mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is asserted high and then low again while $\overline{RAS}$ is asserted low, the read and write operations are enabled. In this method, the row address bits A0 through A8 are supplied by on chip refresh counter.

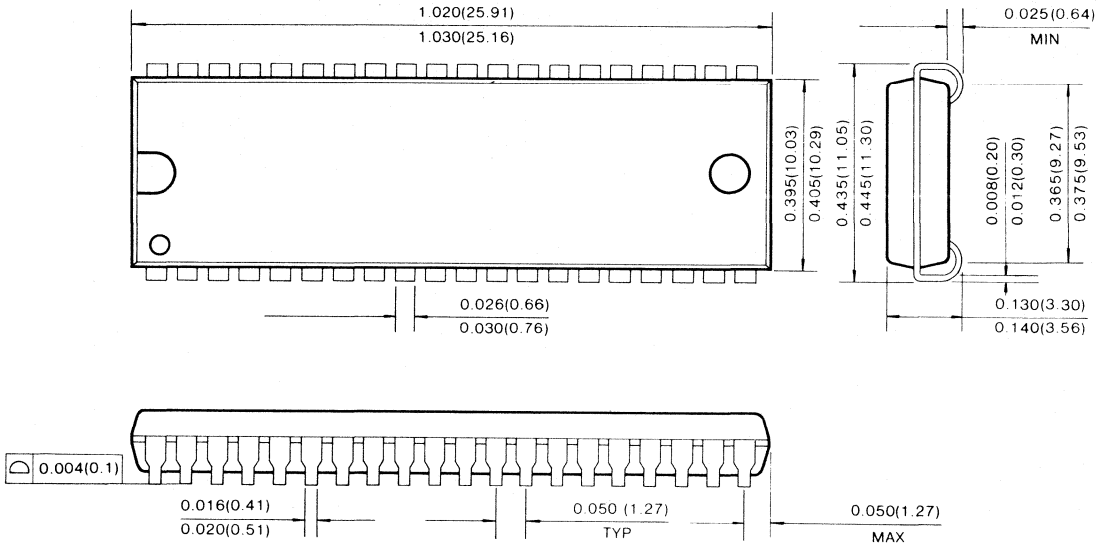
Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM418C256LL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held a valid V_{IH} in order to minimize the power-up current.

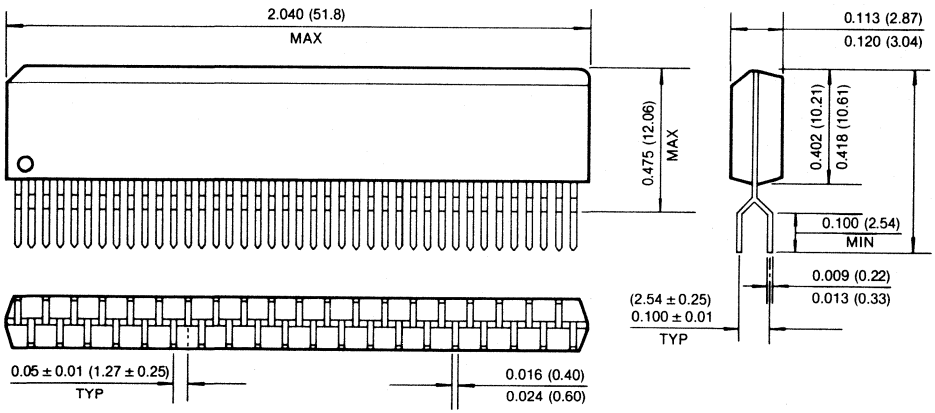
PACKAGE DIMENSION

40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



40-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



16MX1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C16000-6	60ns	15ns	110ns
KM41C16000-7	70ns	20ns	130ns
KM41C16000-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Wirte**
- **Double +5V±10% power supply**
- **4096 cycles/64ms refresh**
- **JEDEC standard pinout**
- **Available in plastic SOJ, TSOP (II) packages**

GENERAL DESCRIPTION

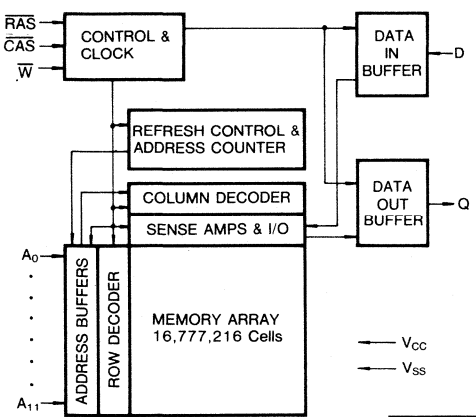
The Samsung KM41C16000 is a high speed CMOS 16,777,216×1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C16000 features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

The KM41C16000 is fabricated using Samsung's advanced CMOS process.

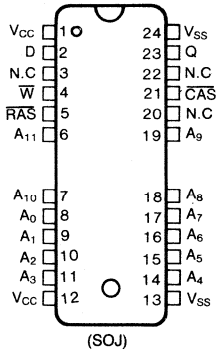
2

FUNCTIONAL BLOCK DIAGRAM



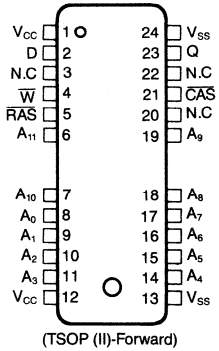
PIN CONFIGURATION (Top Views)

- **KM41C16000J**



(SOJ)

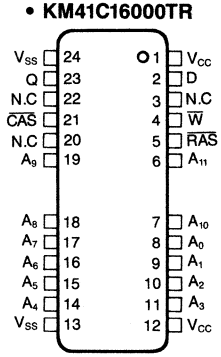
- **KM41C16000T**



(TSOP (II)-Forward)

Pin Name	Pin Function
A0-A11	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

- **KM41C16000TR**



(TSOP (II)-Reverse)

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM41C16000-6	I_{CC1}	—	90	mA
	KM41C16000-7		—	80	mA
	KM41C16000-8		—	70	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @ t_{RC}=min.)	KM41C16000-6	I_{CC3}	—	90	mA
	KM41C16000-7		—	80	mA
	KM41C16000-8		—	70	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @ t_{PC}=min.)	KM41C16000-6	I_{CC4}	—	80	mA
	KM41C16000-7		—	70	mA
	KM41C16000-8		—	60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM41C16000-6	I_{CC6}	—	90	mA
	KM41C16000-7		—	80	mA
	KM41C16000-8		—	70	mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL}, D_{OUT} Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} address transition should be changed only once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address transition should be changed only once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	—	5	pF
Input Capacitance (A_0-A_{11})	C_{IN2}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN3}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	KM41C16000-6		KM41C16000-7		KM41C16000-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	130		155		175		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

Parameter	Symbol	KM41C16000-6		KM41C16000-7		KM41C16000-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (4,096 cycles)	t_{REF}		64		64		64	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	15		20		20		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	60		70		80		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	30		35		40		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	60		70		75		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
Write command set-up time (test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ cycle)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ cycle)	t_{WRH}	10		10		10		ns	

TEST MODE CYCLE

(Note. 12)

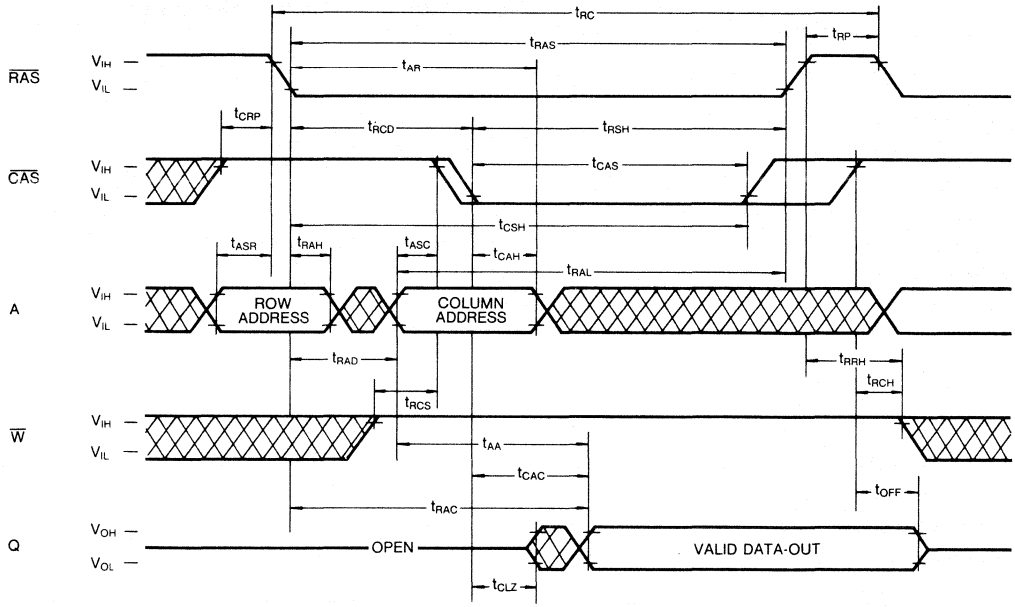
Parameter	Symbol	KM41C16000-6		KM41C16000-7		KM41C16000-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	135		160		180		ns	
Access time from $\overline{RAS}$	t_{RAC}		65		75		85	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,10
$\overline{RAS}$ pulse width	t_{RAS}	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		45		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	20		25		25		ns	7
$\overline{RAS}$ to write enable delay	t_{RWD}	65		75		85		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		45		ns	7
Fast mode cycle time	t_{PC}	45		50		55		ns	
Fast page mode read-modefy-write	t_{PRWC}	65		75		80		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3

NOTES

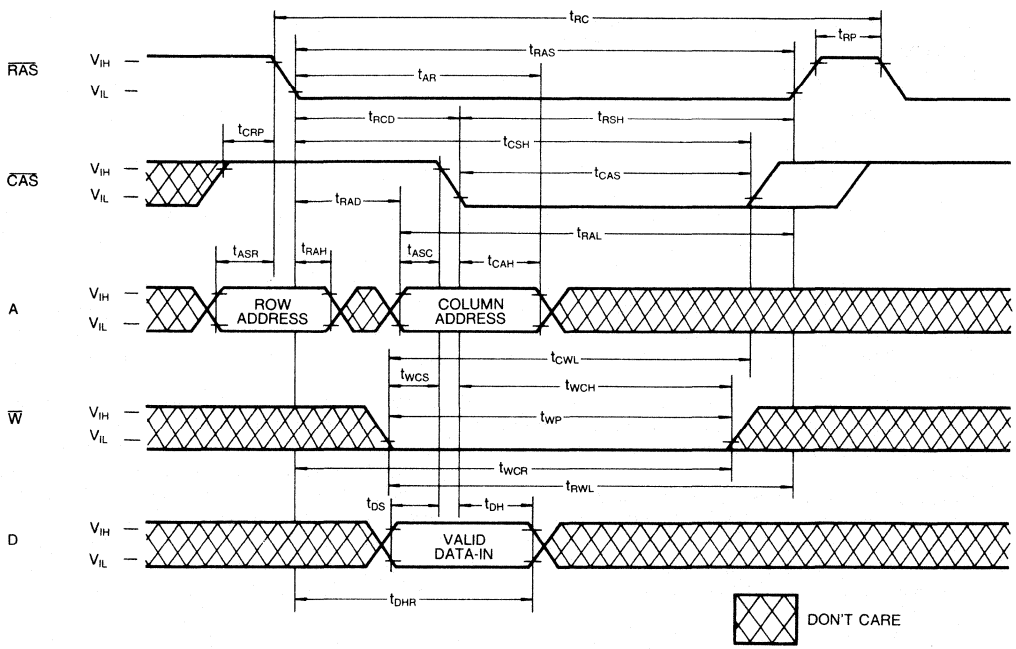
1. An initial pause of 200μs is required after power up followed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only Refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF(max)}$ and $t_{OEZ(max)}$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

TIMING DIAGRAMS

READ CYCLE

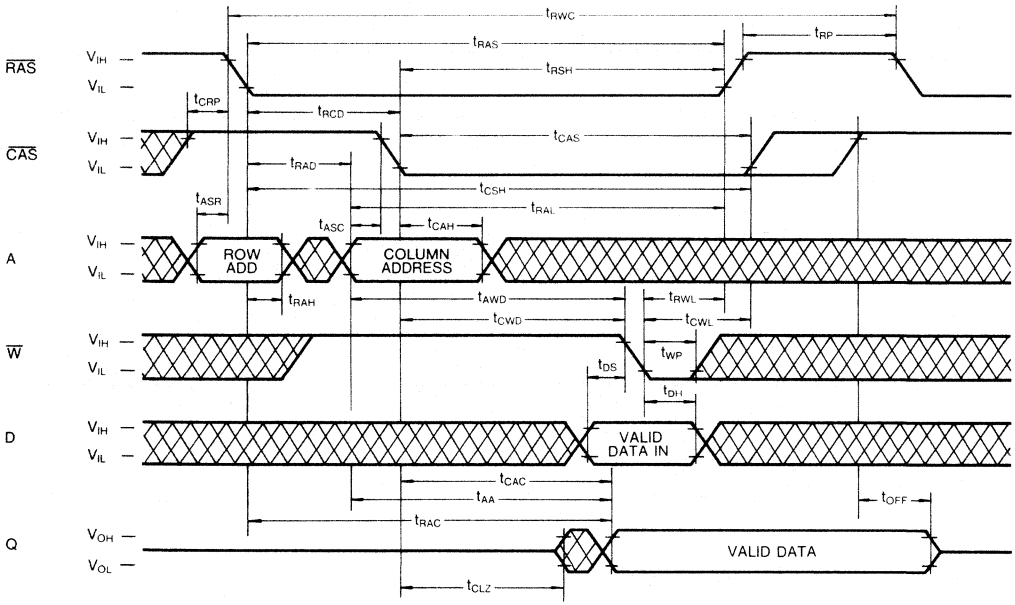


WRITE CYCLE (EARLY WRITE)

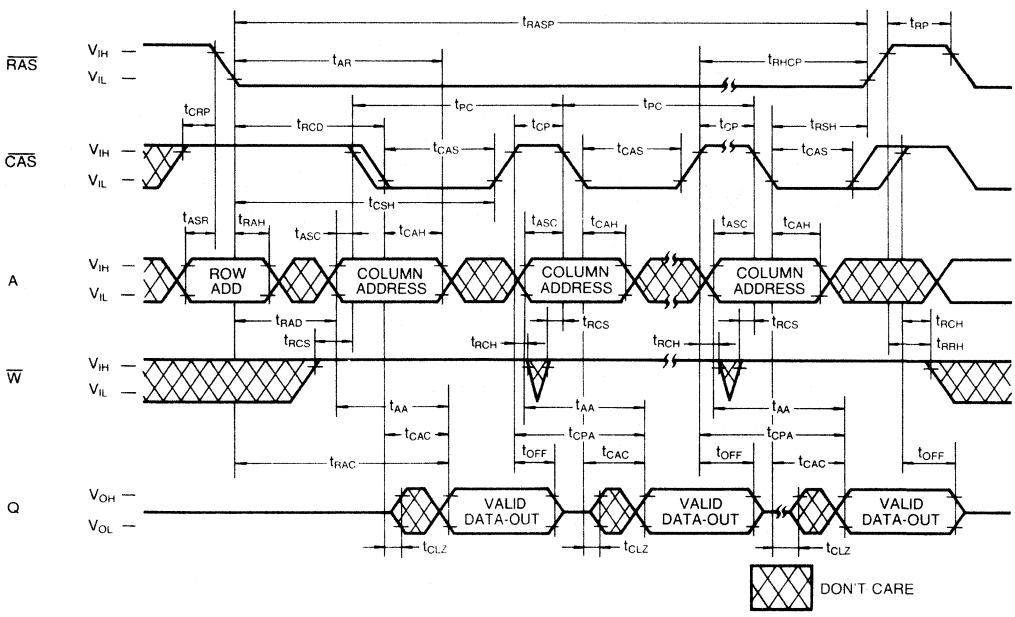


TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

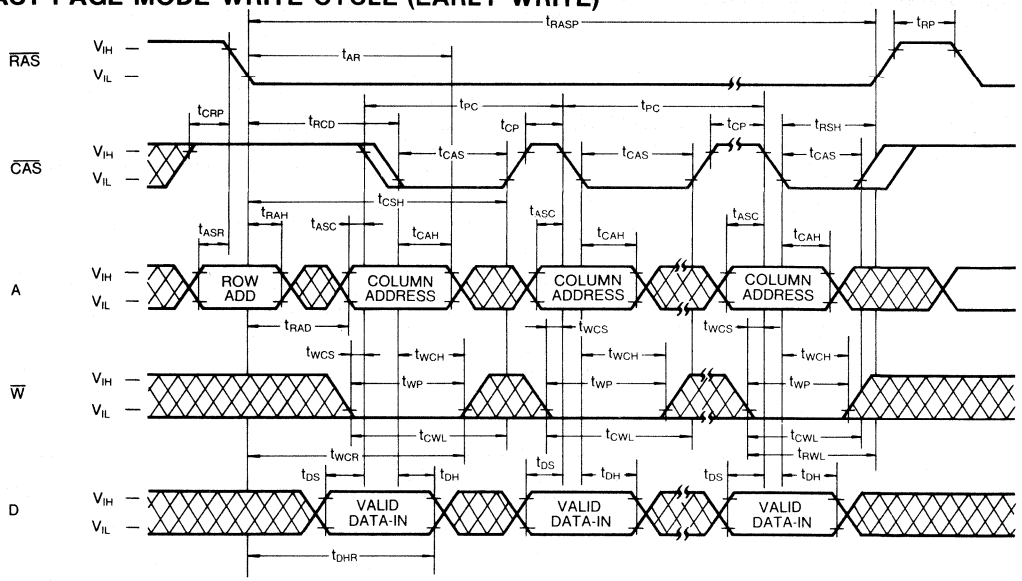


FAST PAGE MODE READ CYCLE

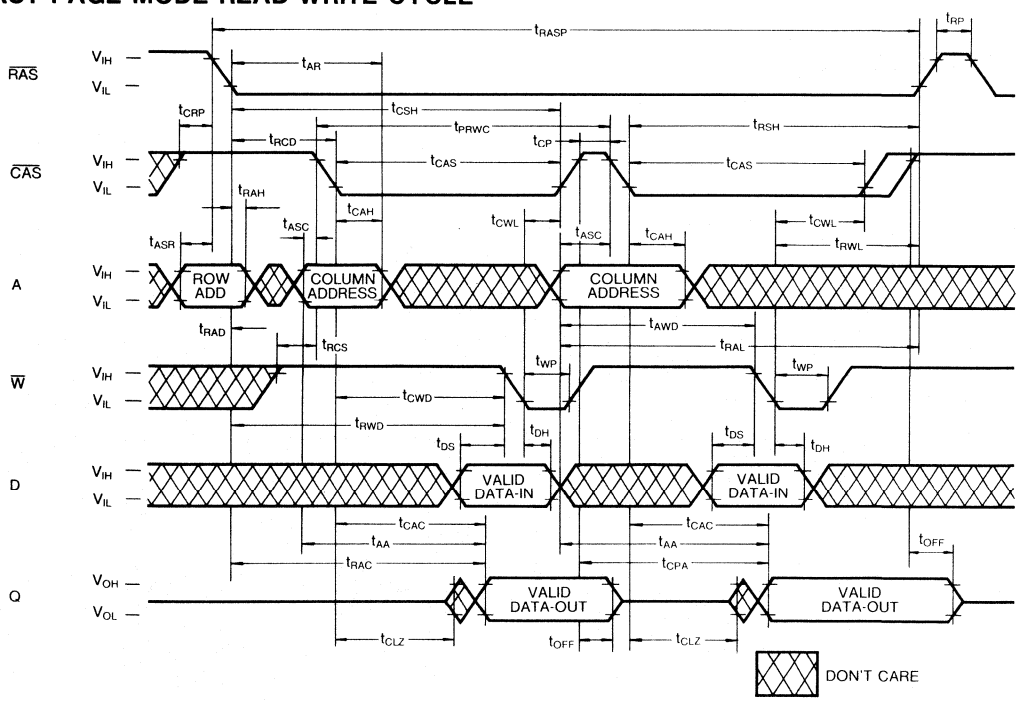


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



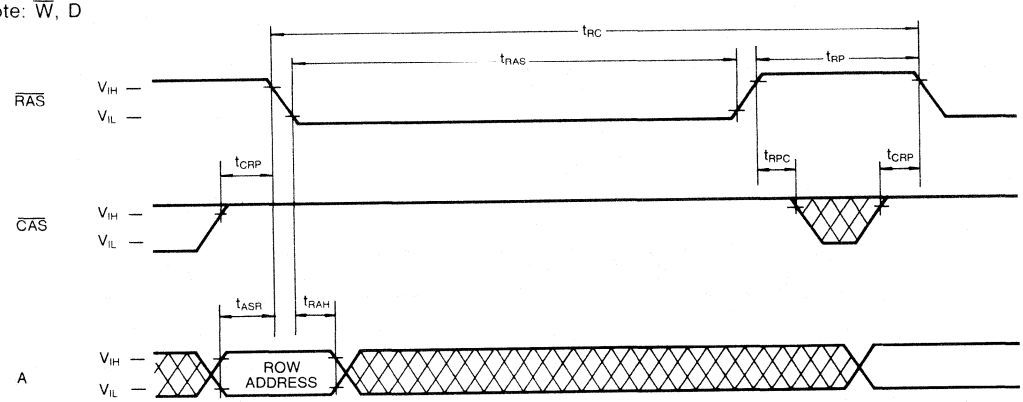
FAST PAGE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

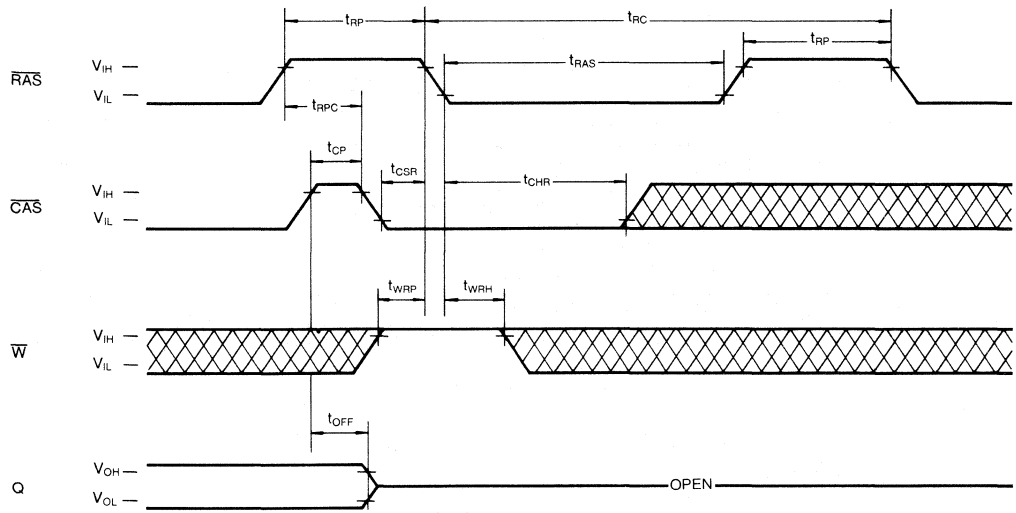
$\overline{RAS}$ ONLY REFRESH CYCLE

Note: $\overline{W}$, D



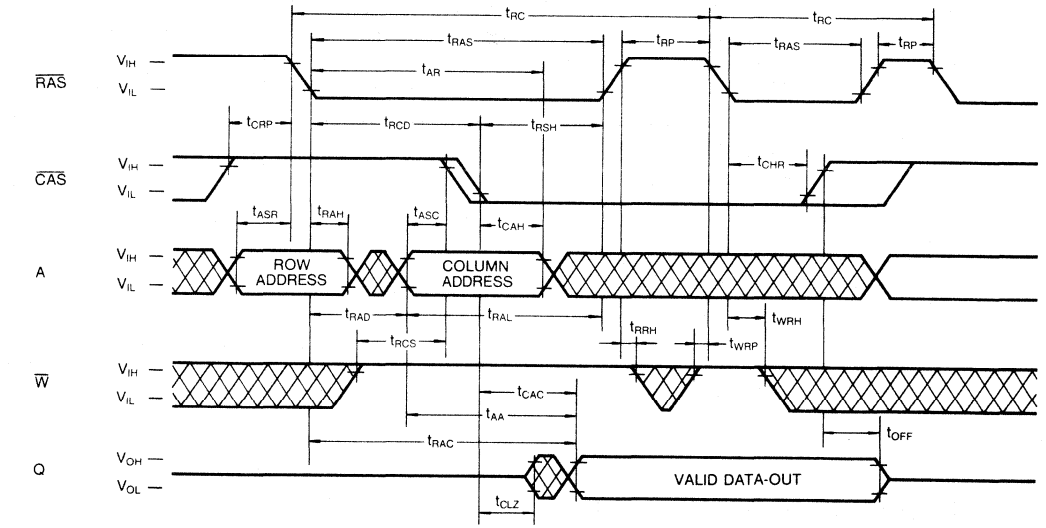
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: Address=Don't Care

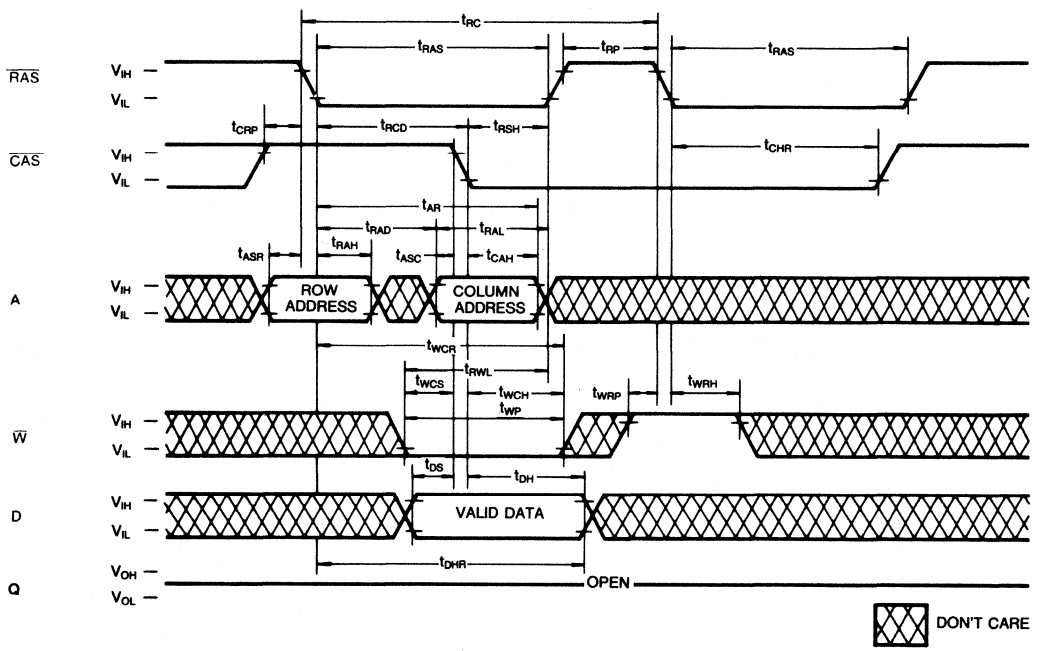


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

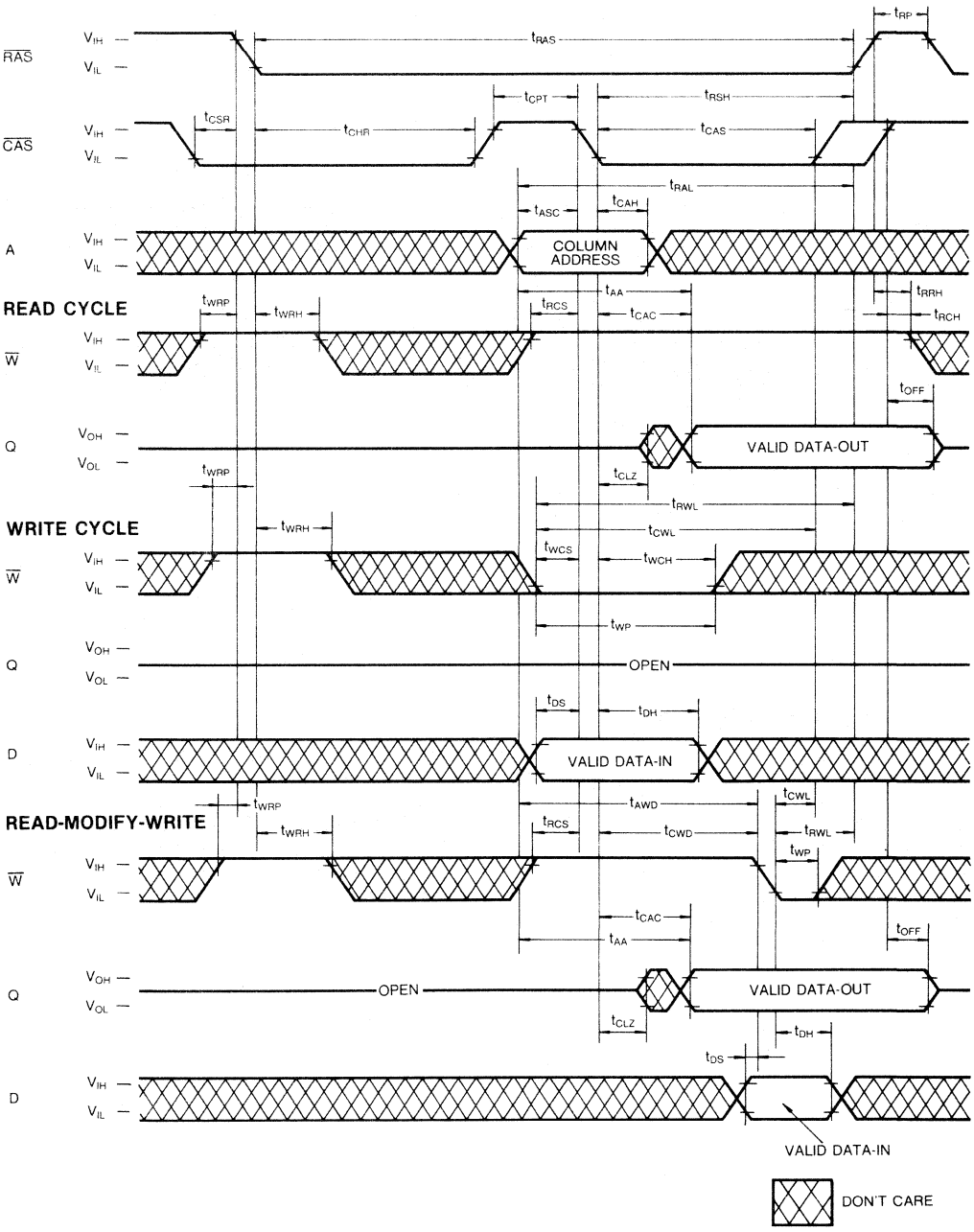


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

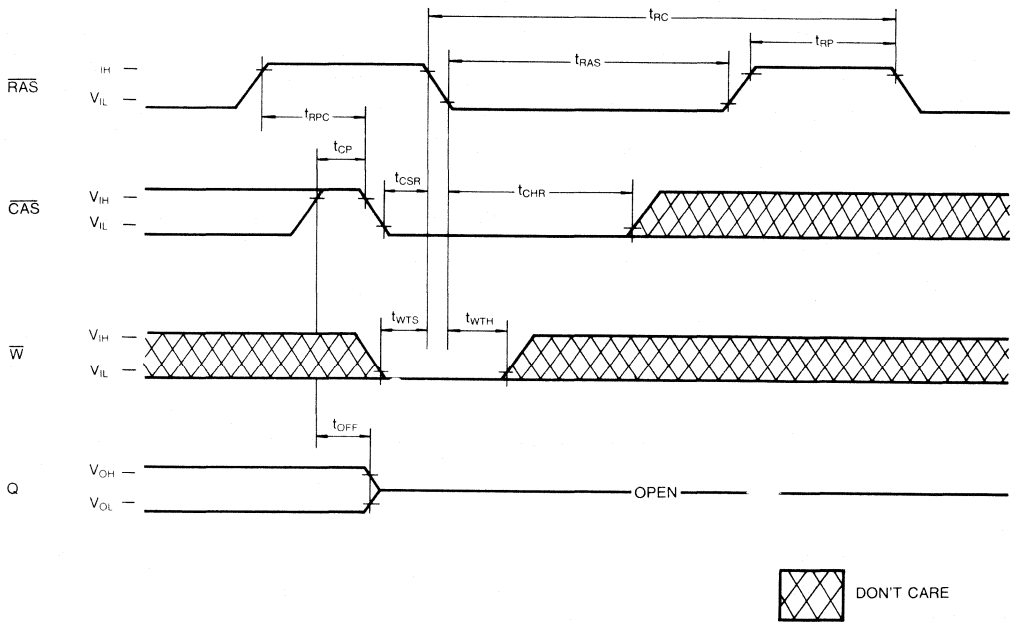
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: D, Address: Don't Care



TEST MODE DESCRIPTION

The KM41C16000 is the RAM organized 16,777,216 words by 1 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0, A_1, A_{10} and $A_{11}$are not used. If, upon reading, 16 bits are equal (all "1"s or "0"s) the Q pin indicates a "1".

If they were not equal, the Q pin would indicate a "0"

In "Test Mode", the 16M DRAM can be tested as if it were a 1M×1 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE "or" "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/16 in cases of N test pattern).

DEVICE OPERATIONS

The KM41C16000 contains 16,777,216 memory locations. Twenty four address bits are required to address a particular memory location. Since the KM41C16000 has only 12 address input pins, time multiplexed addressing is used to input 12 row and 12 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM41C16000 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 12 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C16000 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C16000 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41C16000 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C16000 has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C16000 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C16000 is stored on a tiny capacitor within each memory cell. Due to leakage the

DEVICE OPERATION (Continued)

data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 64 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C16000 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuity is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C16000 hidden refresh cycle is actually a $\overline{CAS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C16000 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM41C16000 has Fast Page mode capability. Fast Page mode capability. Fast Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In Fast Page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A fast Page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page. Up to 4096 memory cells can be accessed with the same row address.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 12 row address bits and 12 column address bits defined as follows:

Row Address—Bits A_0 through A_{11} are supplied by the on-chip refresh counter.

Column Address—Bits A_0 through A_{11} are strobedin by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 4096 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 4096 times so that highs are written into the 4096 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

If $\overline{RAS}$-V_{SS} during power-up, the KM41C16000 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 64 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41C16000

DEVICE OPERATION (Continued)

inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C16000 input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

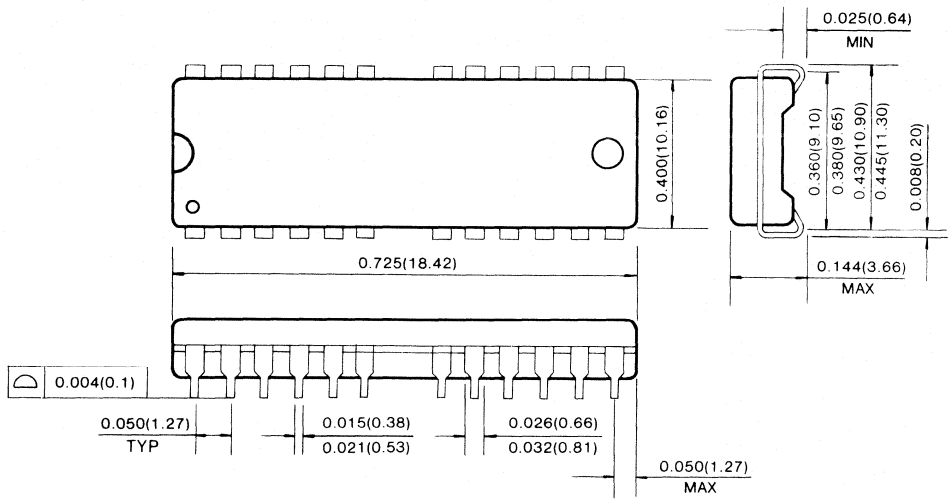
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM41C16000 u;sing the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C16000 and they supply much of the current used by the KM41C16000 during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantlum capacitor around the memory array.

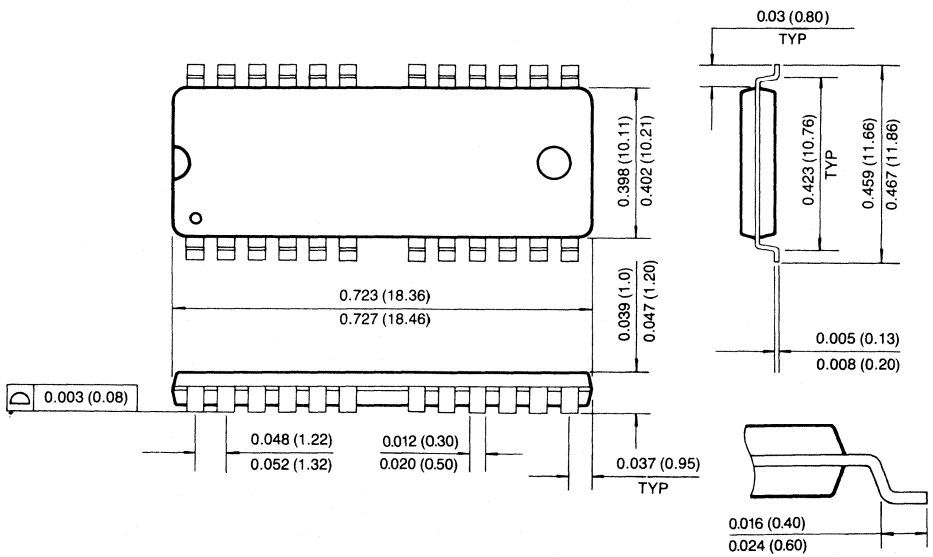
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (Forward and Reverse Type)



16M×1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C16000L-6	60ns	15ns	110ns
KM41C16000L-7	70ns	20ns	130ns
KM41C16000L-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Wirte**
- **Double +5V±10% power supply**
- **4096 cycles/256ms refresh**
- **JEDEC standard pinout**
- **Available in plastic SOJ, TSOP (II) packages**

GENERAL DESCRIPTION

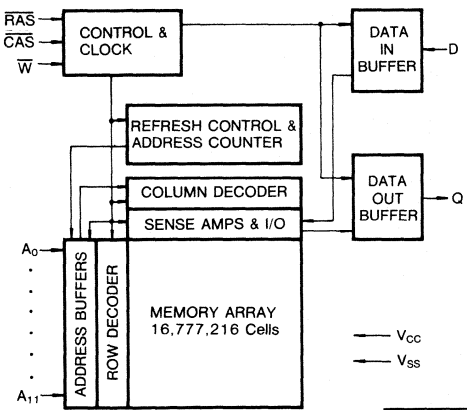
The Samsung KM41C16000L is a CMOS high speed 16,777,216 × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C16000L features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM41C16000L is fabricated using Samsung's advanced CMOS process.

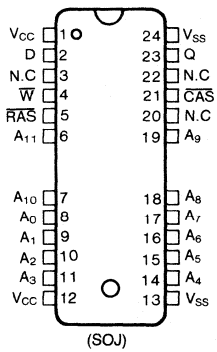
2

FUNCTIONAL BLOCK DIAGRAM



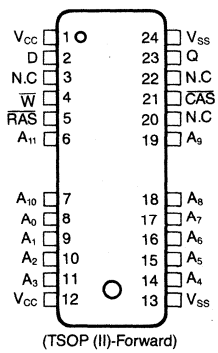
PIN CONFIGURATION (Top Views)

• **KM41C16000LJ**



(SOJ)

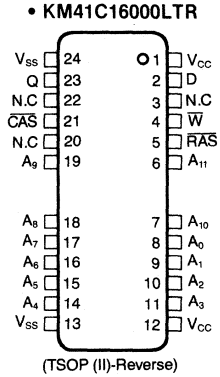
• **KM41C16000LT**



(TSOP (II)-Forward)

Pin Name	Pin Function
A0-A11	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

• **KM41C16000LTR**



(TSOP (II)-Reverse)

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC} = min.)	KM41C16000L-6	I_{CC1}	—	90	mA
	KM41C16000L-7		—	80	mA
	KM41C16000L-8		—	70	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM41C16000L-6	I_{CC3}	—	90	mA
	KM41C16000L-7		—	80	mA
	KM41C16000L-8		—	70	mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC} = min.)	KM41C16000L-6	I_{CC4}	—	80	mA
	KM41C16000L-7		—	70	mA
	KM41C16000L-8		—	60	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		I_{CC5}	—	300	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min.)	KM41C16000L-6	I_{CC6}	—	90	mA
	KM41C16000L-7		—	80	mA
	KM41C16000L-8		—	70	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH}) = V_{CC}-0.2V Input Low Voltage (V_{IL}) = 0.2V $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V DQ_{1-4} = Don't Care T_{RC} = 62.5μs, T_{RAS} = t_{RAS} min. ~ 1μs		I_{CC7}	—	500	μA
Standby Current ($\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{OUT} Enable)		I_{CC8}	—	5	mA
Input Leakage Current (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$ = V_{IL}. In I_{CC4}, Address can be changed maximum once while $\overline{CAS}$ = V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	—	5	pF
Input Capacitance (A_0-A_{11})	C_{IN2}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN3}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	KM41C16000L-6		KM41C16000L-7		KM41C16000L-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	130		155		175		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

Parameter	Symbol	KM41C16000L-6		KM41C16000L-7		KM41C16000L-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (4,096 cycles)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	15		20		20		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	60		70		80		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	30		35		40		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	60		70		75		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
Write command set-up time (test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ cycle)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ cycle)	t_{WRH}	10		10		10		ns	

TEST MODE CYCLE

(Note. 12)

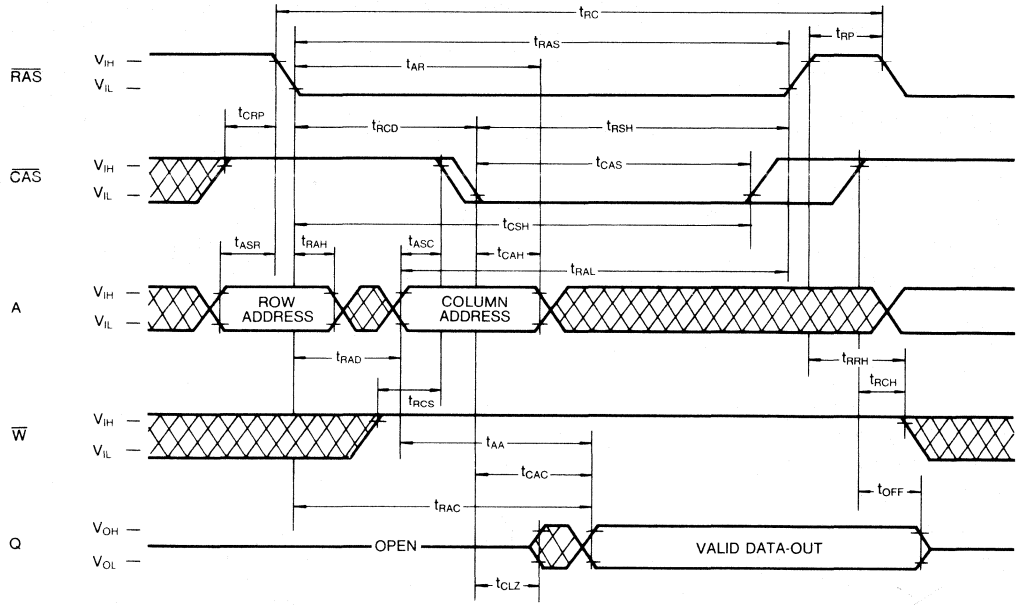
Parameter	Symbol	KM41C16000L-6		KM41C16000L-7		KM41C16000L-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	135		160		180		ns	
Access time from $\overline{RAS}$	t_{RAC}		65		75		85	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,10
$\overline{RAS}$ pulse width	t_{RAS}	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		45		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	20		25		25		ns	7
$\overline{RAS}$ to write enable delay	t_{RWD}	65		75		85		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		45		ns	7
Fast mode cycle time	t_{PC}	45		50		55		ns	
Fast page mode read-modefy-write	t_{PRWC}	65		75		80		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3

NOTES

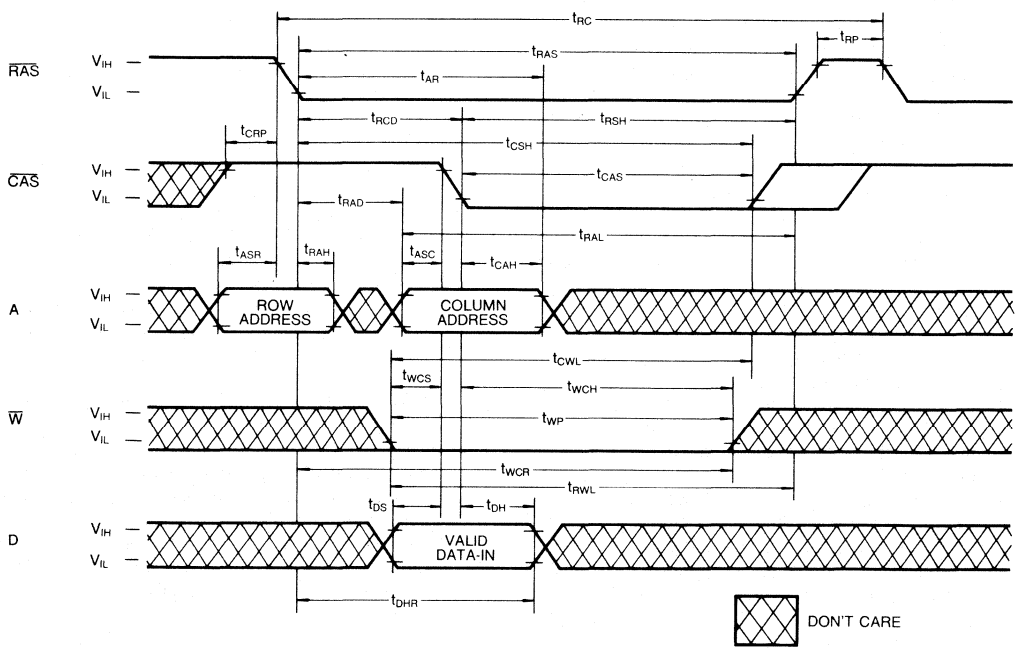
1. An initial pause of 200μs is required after power up followed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only Refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF(max)}$ and $t_{OEZ(max)}$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

TIMING DIAGRAMS

READ CYCLE

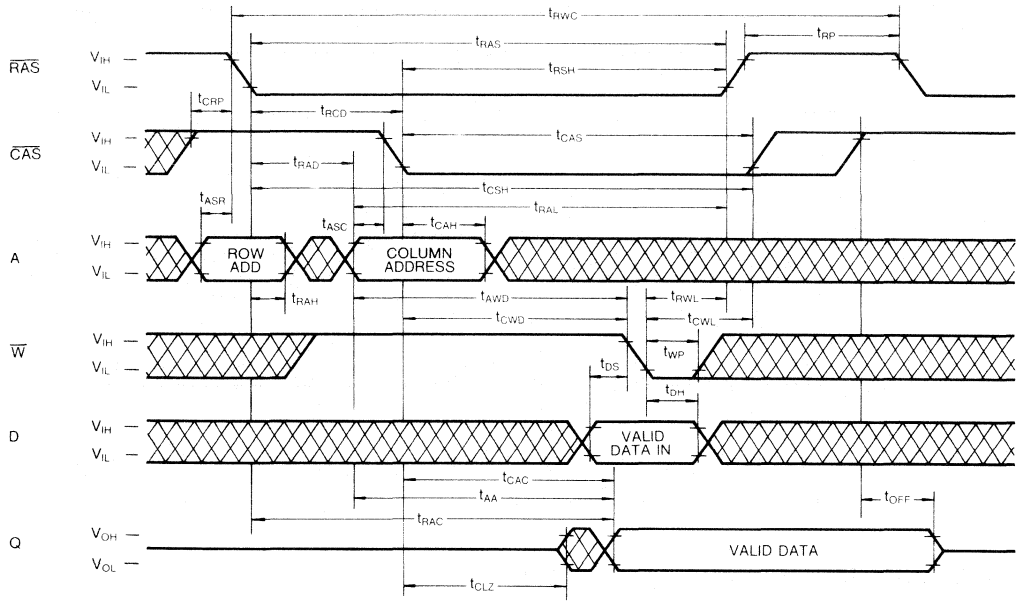


WRITE CYCLE (EARLY WRITE)

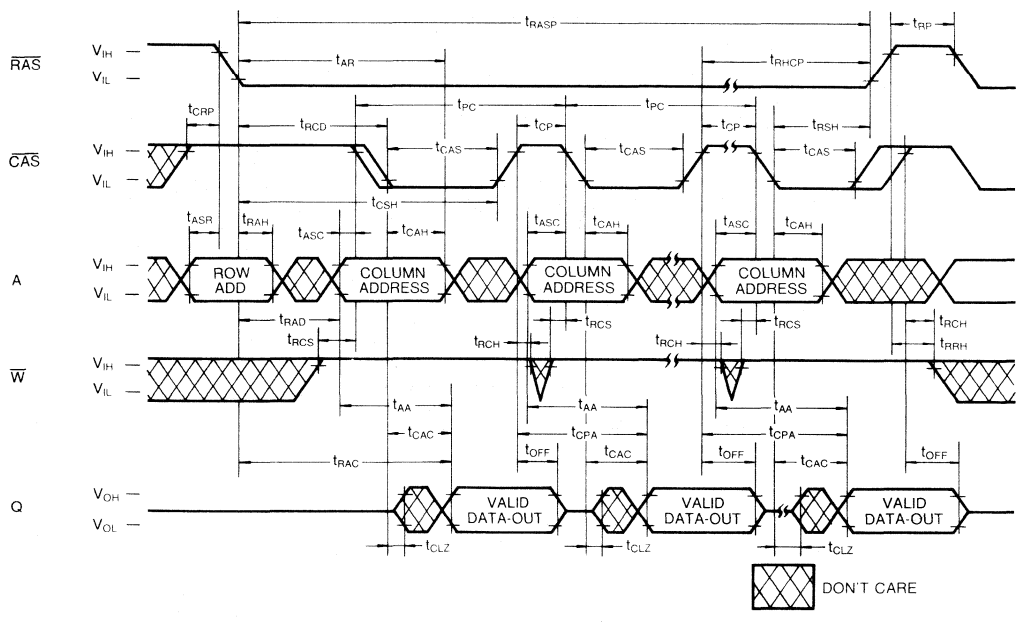


TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

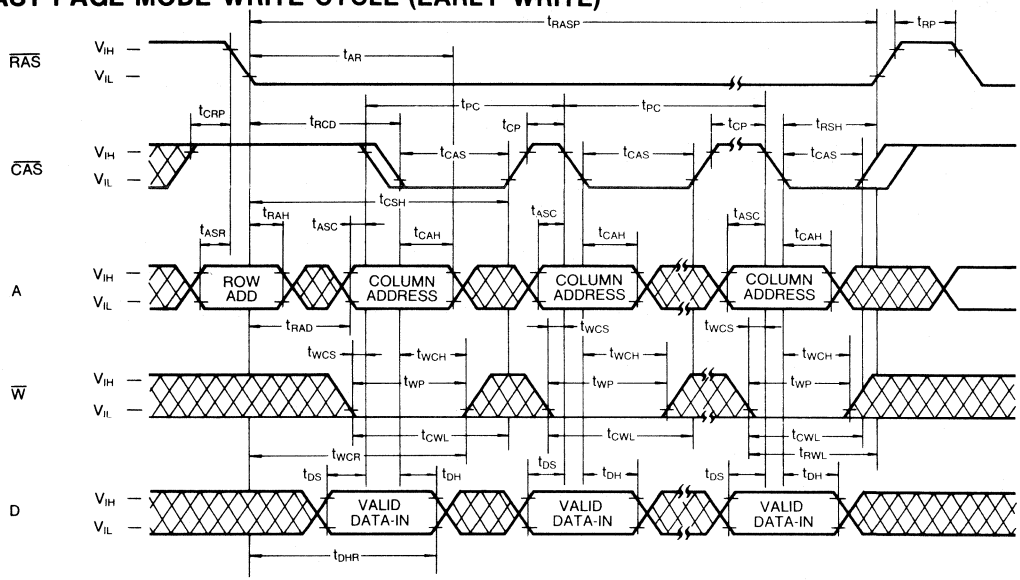


FAST PAGE MODE READ CYCLE

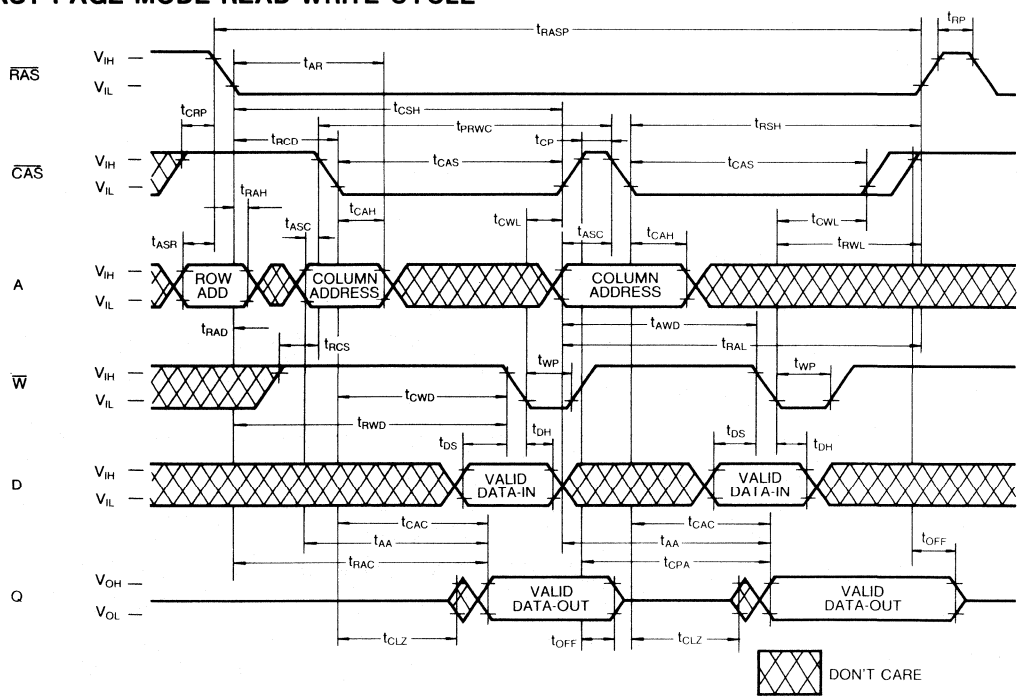


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



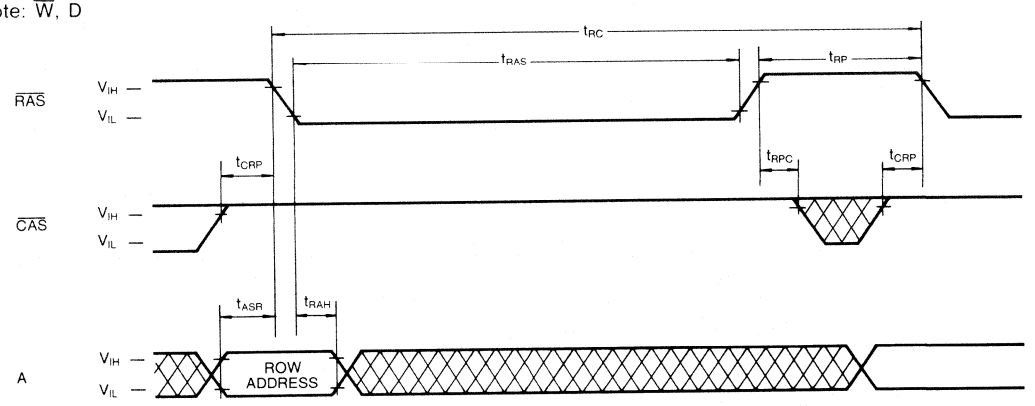
FAST PAGE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

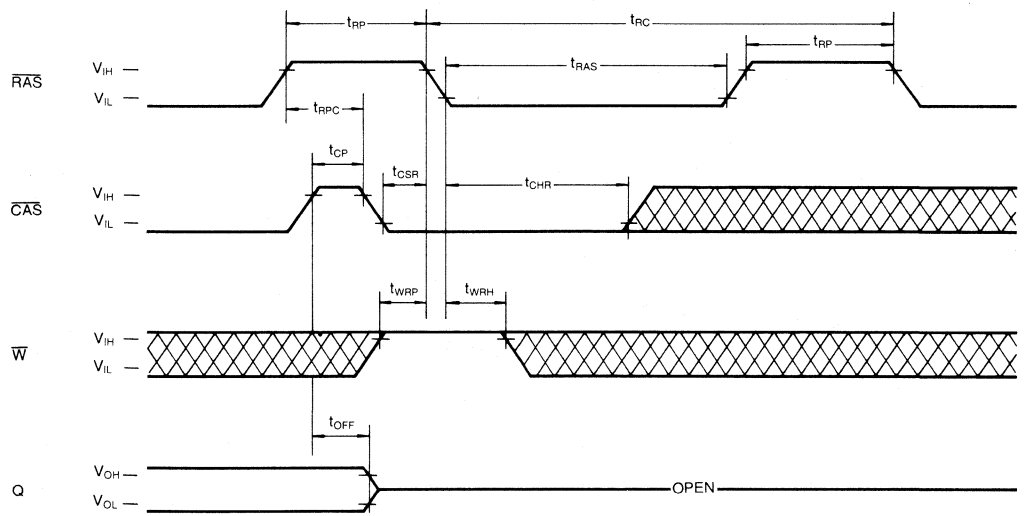
$\overline{RAS}$ ONLY REFRESH CYCLE

Note: $\overline{W}$, D



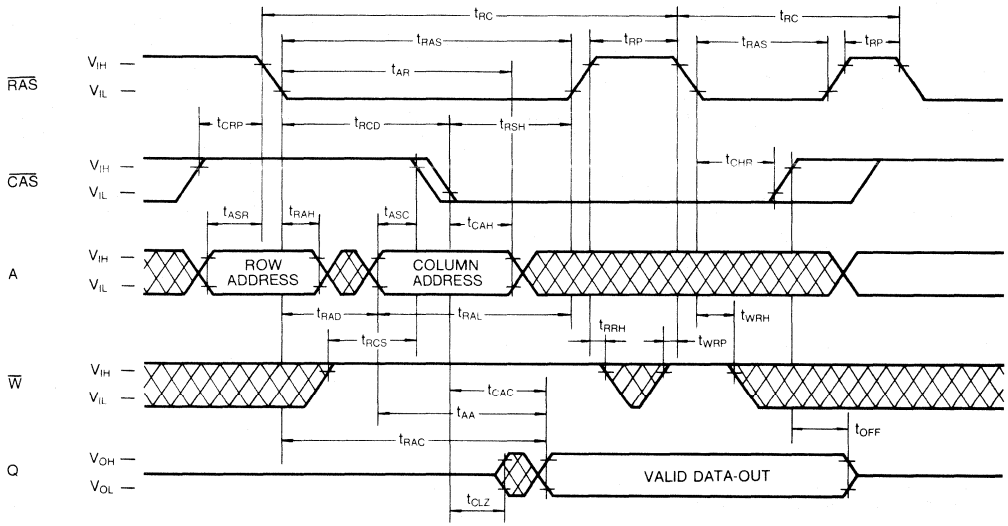
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: Address=Don't Care

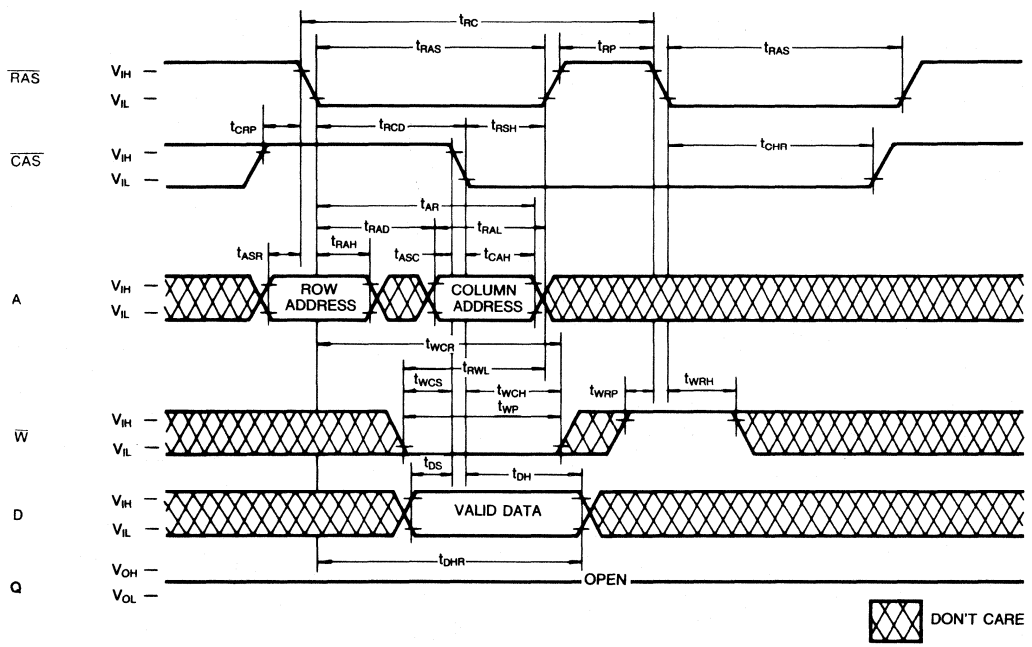


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

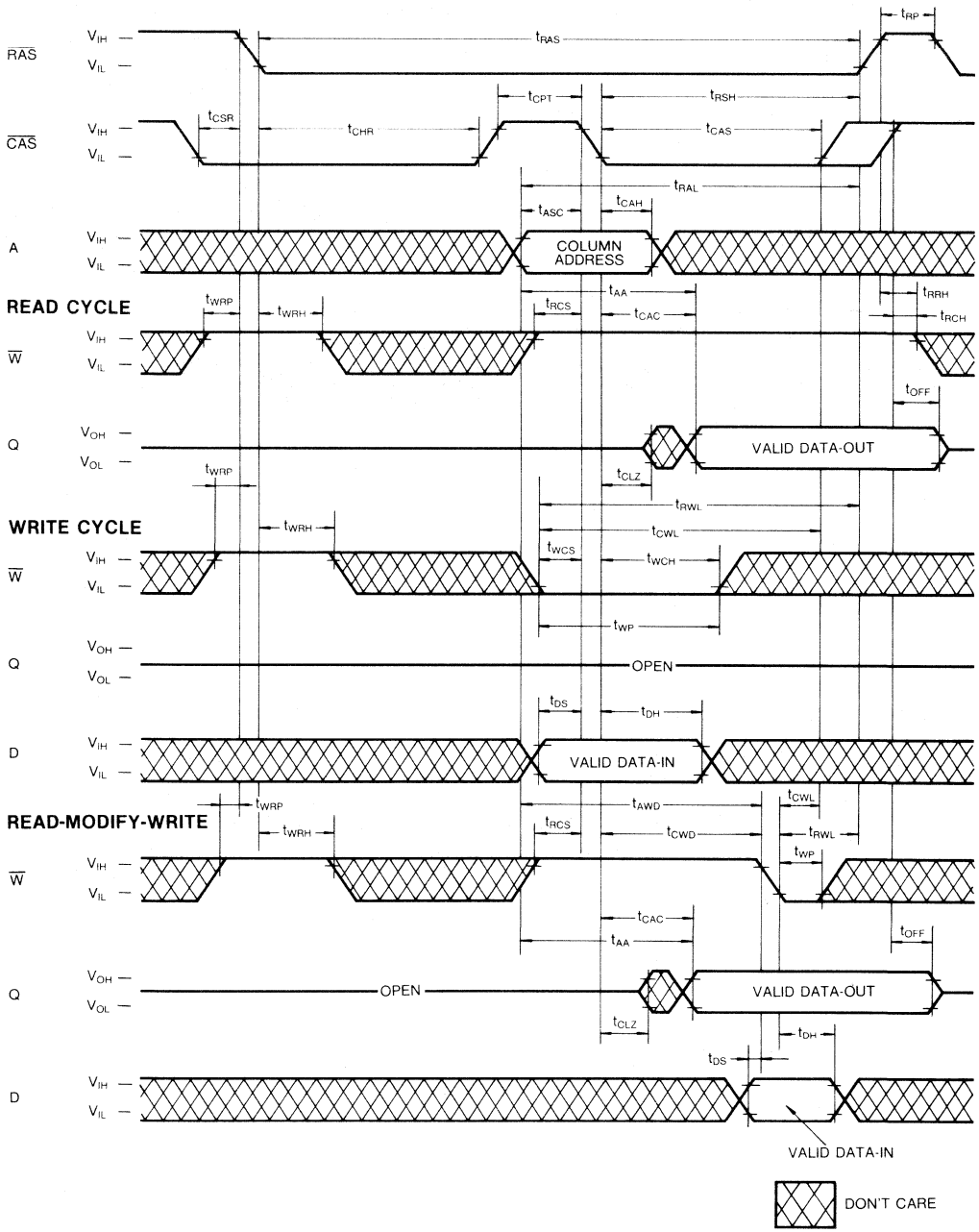


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

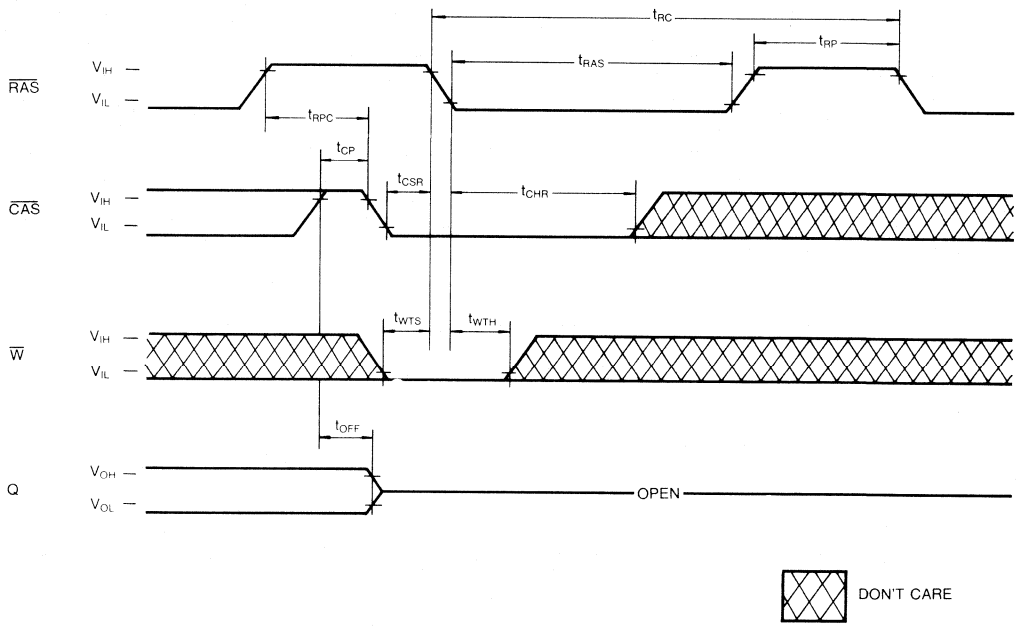
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: D, Address: Don't Care



TEST MODE DESCRIPTION

The KM41C16000L is the RAM organized 16,777,216 words by 1 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0, A_1, A_{10} and A_{11} are not used. If, upon reading, 16 bits are equal (all "1"s or "0"s) the Q pin indicates a "1".

If they were not equal, the Q pin would indicate a "0"

In "Test Mode", the 16M DRAM can be tested as if it were a 1M×1 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE "or" "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/16 in cases of N test pattern).

DEVICE OPERATIONS

The KM41C16000L contains 16,777,216 memory locations. Twenty-four address bits are required to address a particular memory location. Since the KM41C16000L has only 12 address input pins, time multiplexed addressing is used to input 12 row and 12 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM41C16000L begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 12 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C16000L cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing RAS low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C16000L begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

The KM41C16000L can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$, $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. The cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing W low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C16000L has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}), the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C16000L operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

DEVICE OPERATION (Continued)

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C16000L is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 256 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C16000L has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C16000L hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C16000L by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM41C16000L has Fast page mode capability. Fast page mode memory cycles provides faster access and lower power dissipation than normal memory cycles. In Fast page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page. Up to 4096 memory cells can be accessed with the same row address.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 12 row address bits and 12 column address bits defined as follows:

Row Address — Bits A_0 through A_{11} are supplied by tthe on-chip refresh counter.

Column Address — Bits A_0 through A_{11} are strobed-in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 4096 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 4096 times so that highs are written into the 4096 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

DEVICE OPERATION (Continued)

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM41C16000L could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. Eight initialization cycles are also required after any 256 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41C16000L inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C16000L input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

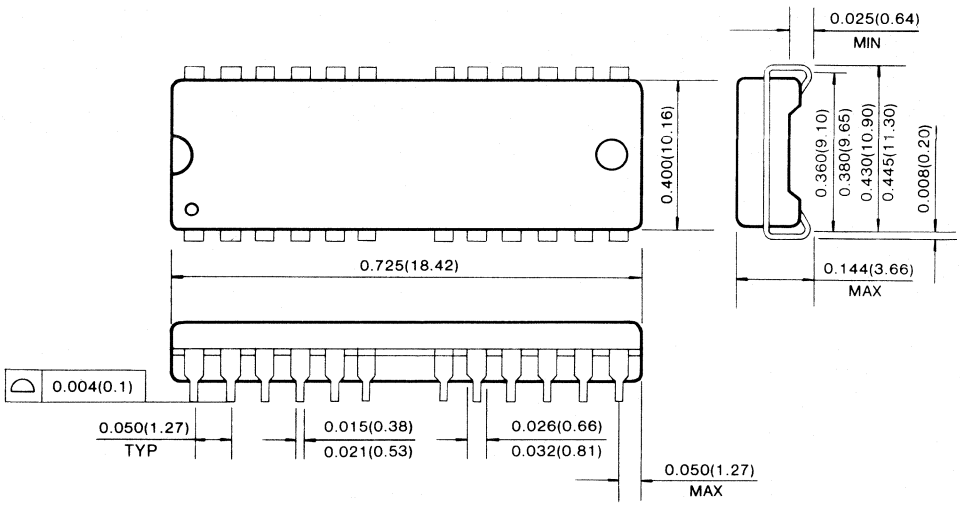
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM41C16000L using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C16000L and they supply much of the current used by the KM41C16000L during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

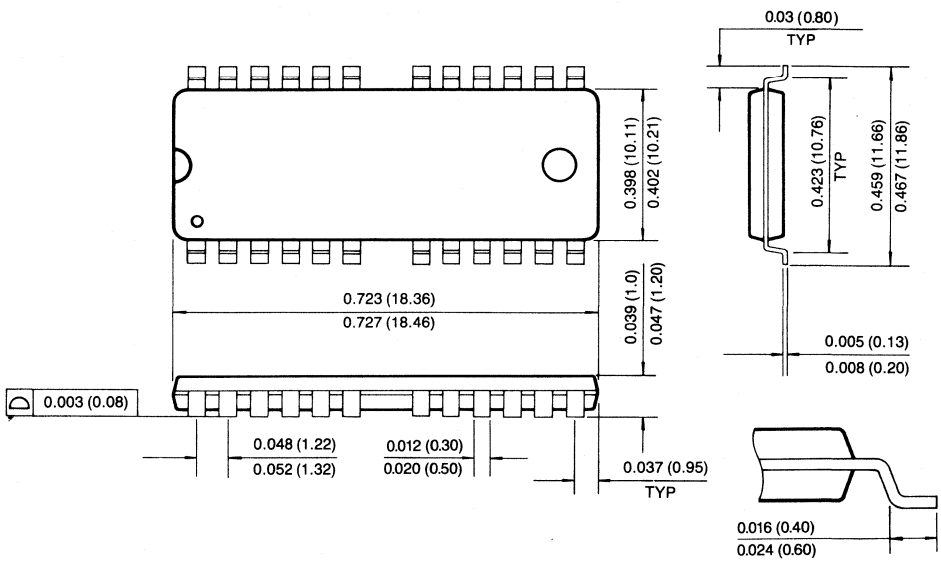
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (Forward and Reverse Type)



16M×1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C16100-6	60ns	15ns	110ns
KM41C16100-7	70ns	20ns	130ns
KM41C16100-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Write**
- **Double +5V±10% power supply**
- **2048 cycles/32ms refresh**
- **JEDEC standard pinout**
- **Available in plastic SOJ, TSOP (II) packages**

GENERAL DESCRIPTION

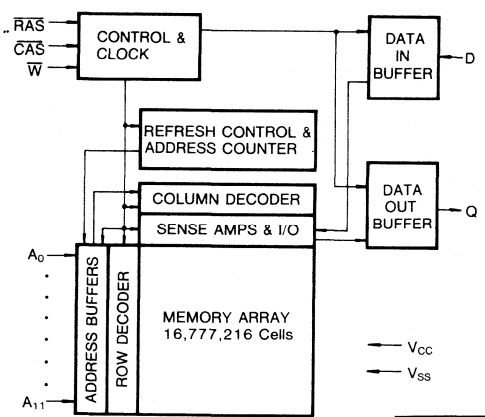
The Samsung KM41C16100 is a high speed CMOS 16,777,216×1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C16100 features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and output are fully TTL compatible.

The KM41C16100 is fabricated using Samsung's advanced CMOS process.

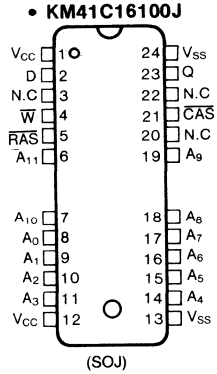
2

FUNCTIONAL BLOCK DIAGRAM



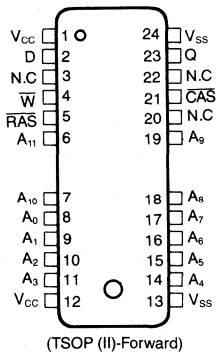
PIN CONFIGURATION (Top Views)

• KM41C16100J



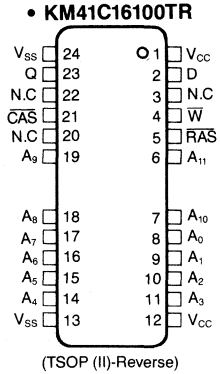
(SOJ)

• KM41C16100T



(TSOP (II)-Forward)

• KM41C16100TR



(TSOP (II)-Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM41C16100-6	I_{CC1}	—	110	mA
	KM41C16100-7		—	100	mA
	KM41C16100-8		—	90	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @ t_{RC}=min.)	KM41C16100-6	I_{CC3}	—	110	mA
	KM41C16100-7		—	100	mA
	KM41C16100-8		—	90	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @ t_{PC}=min.)	KM41C16100-6	I_{CC4}	—	90	mA
	KM41C16100-7		—	80	mA
	KM41C16100-8		—	70	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM41C16100-6	I_{CC6}	—	110	mA
	KM41C16100-7		—	100	mA
	KM41C16100-8		—	90	mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL}, D_{OUT} Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} address transition should be changed only once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address transition should be changed only once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	—	5	pF
Input Capacitance (A_0-A_{11})	C_{IN2}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN3}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	KM41C16100-6		KM41C16100-7		KM41C16100-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	130		155		175		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

Parameter	Symbol	KM41C16100-6		KM41C16100-7		KM41C16100-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (2.048 cycles)	t_{REF}		32		32		32	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	15		20		20		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	60		70		80		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	30		35		40		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	60		70		75		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
Write command set-up time (test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ cycle)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ cycle)	t_{WRH}	10		10		10		ns	

TEST MODE CYCLE

(Note. 12)

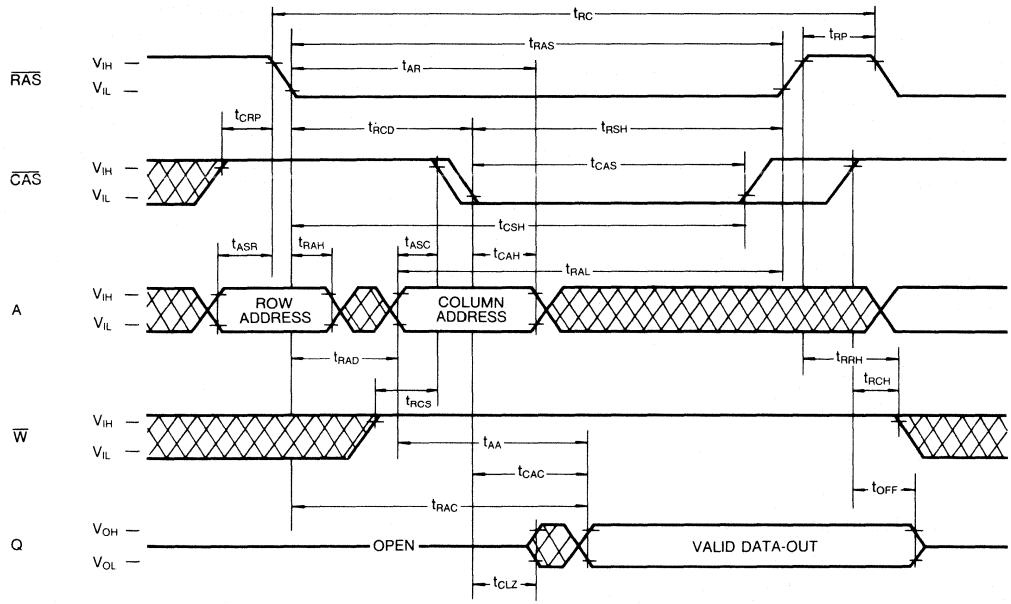
Parameter	Symbol	KM41C16100-6		KM41C16100-7		KM41C16100-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	135		160		180		ns	
Access time from $\overline{RAS}$	t_{RAC}		65		75		85	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,10
$\overline{RAS}$ pulse width	t_{RAS}	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		45		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	20		25		25		ns	7
$\overline{RAS}$ to write enable delay	t_{RWD}	65		75		85		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		45		ns	7
Fast mode cycle time	t_{PC}	45		50		55		ns	
Fast page mode read-modefy-write	t_{PRWC}	65		75		80		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3

NOTES

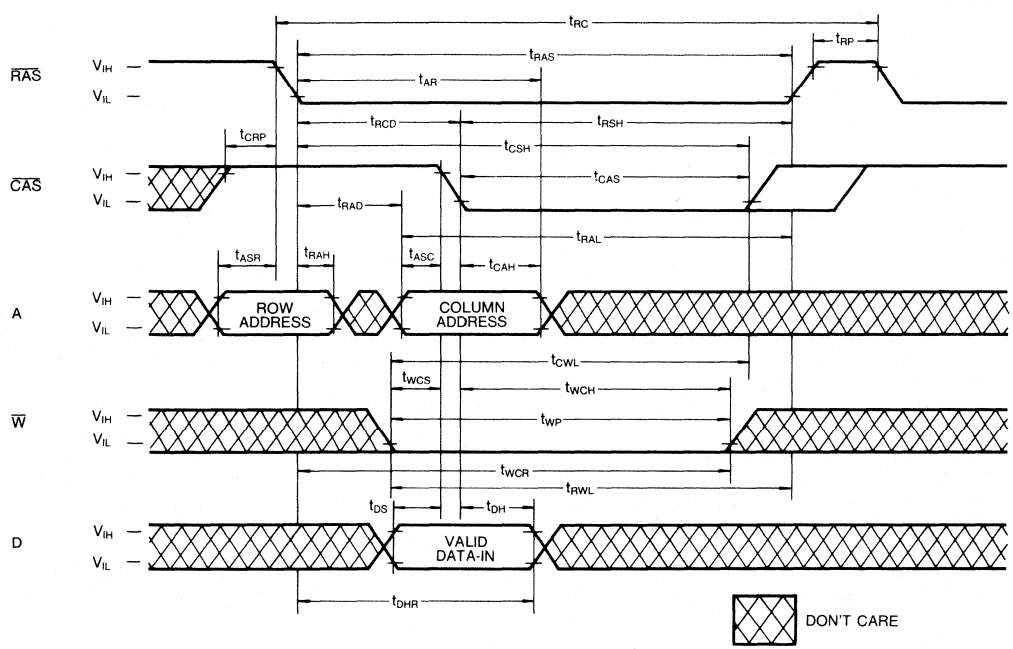
1. An initial pause of 200μs is required after power up followed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only Refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF(max)}$ and $t_{OEZ(max)}$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

TIMING DIAGRAMS

READ CYCLE

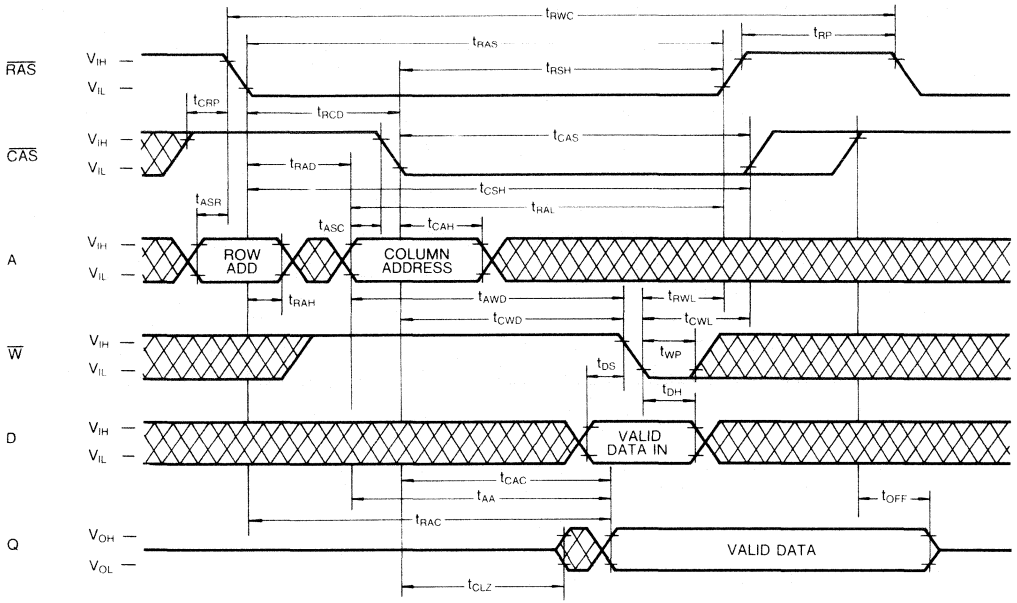


WRITE CYCLE (EARLY WRITE)

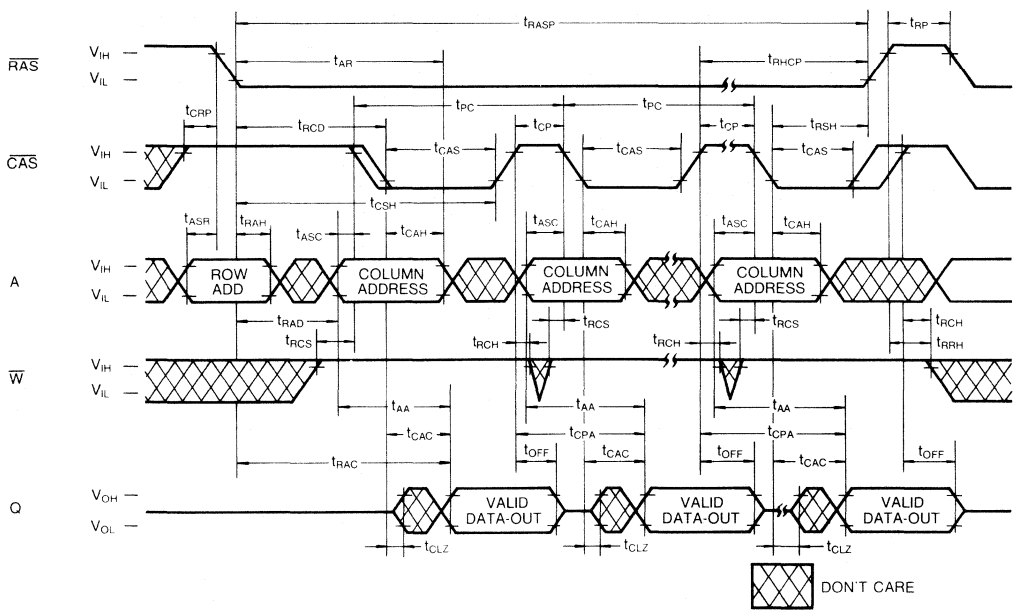


TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

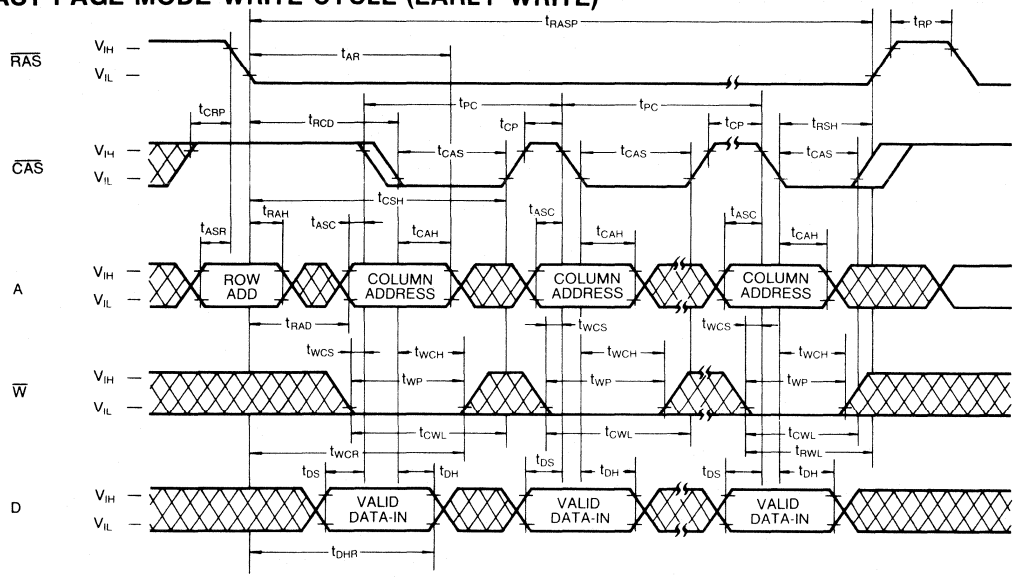


FAST PAGE MODE READ CYCLE

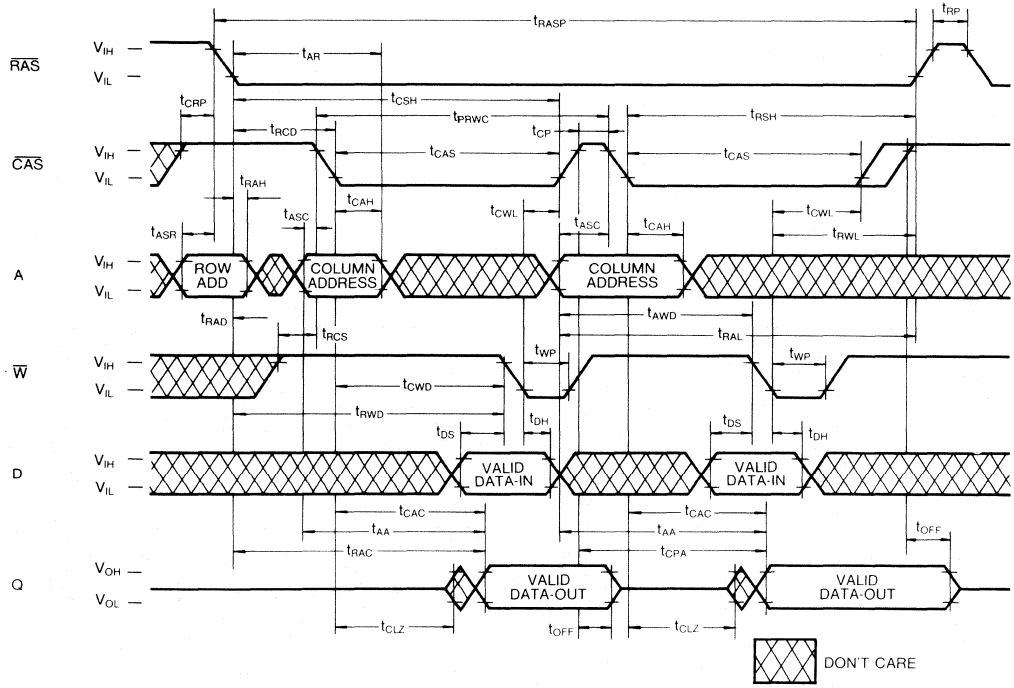


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



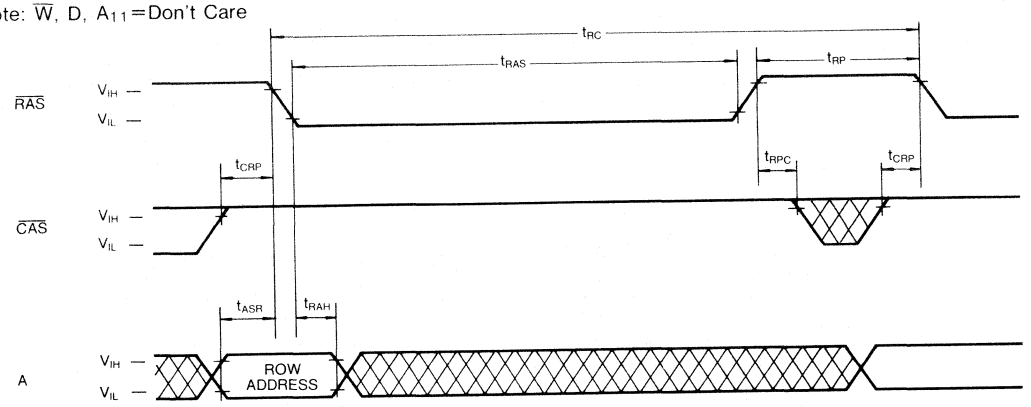
FAST PAGE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

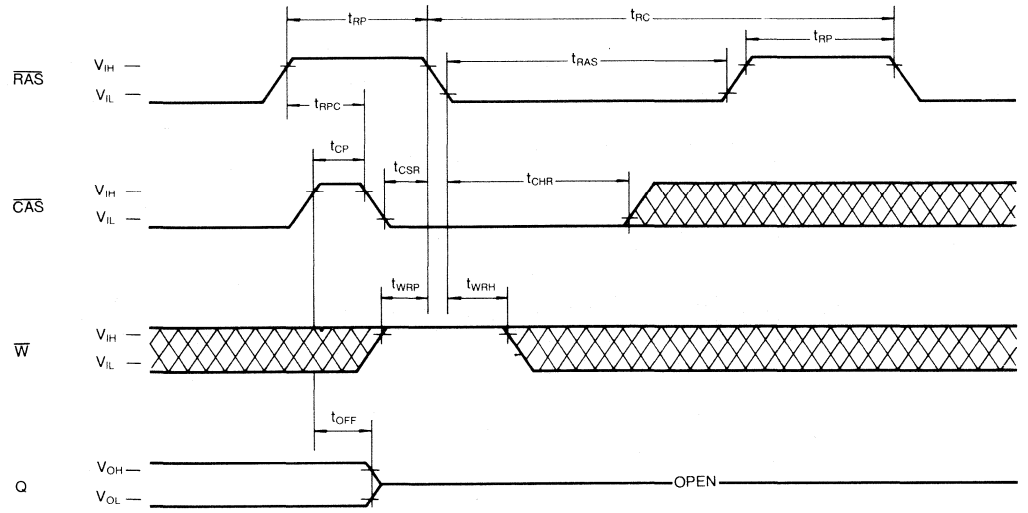
$\overline{RAS}$ ONLY REFRESH CYCLE

Note: $\overline{W}$, D, A_{11} = Don't Care



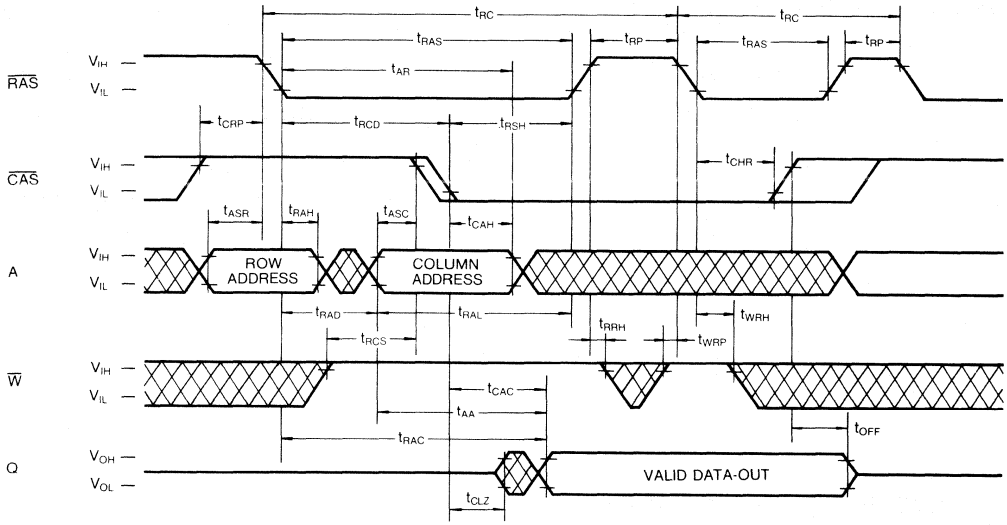
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: Address = Don't Care

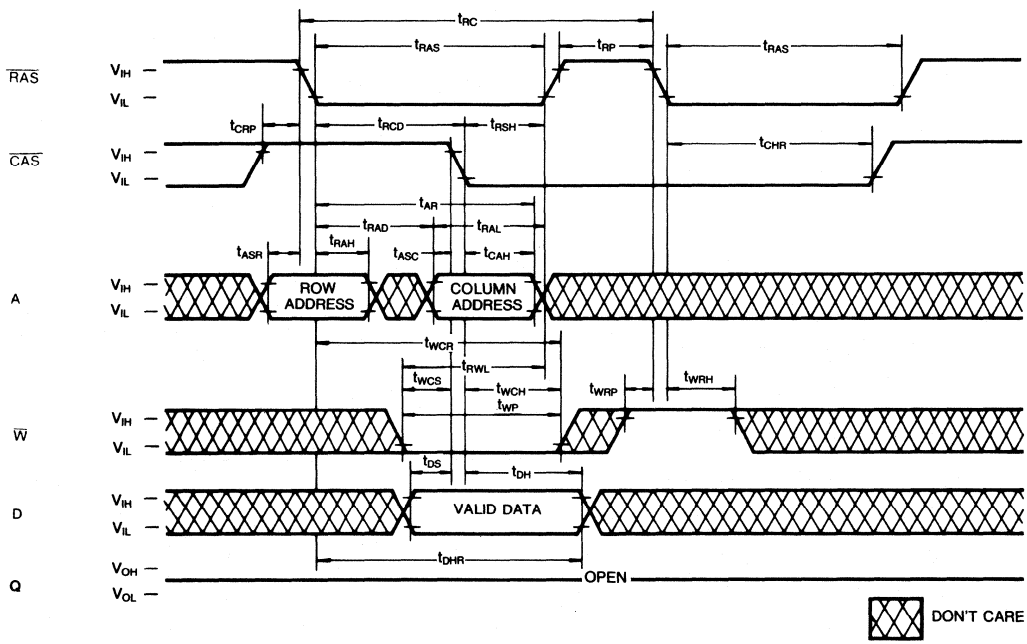


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

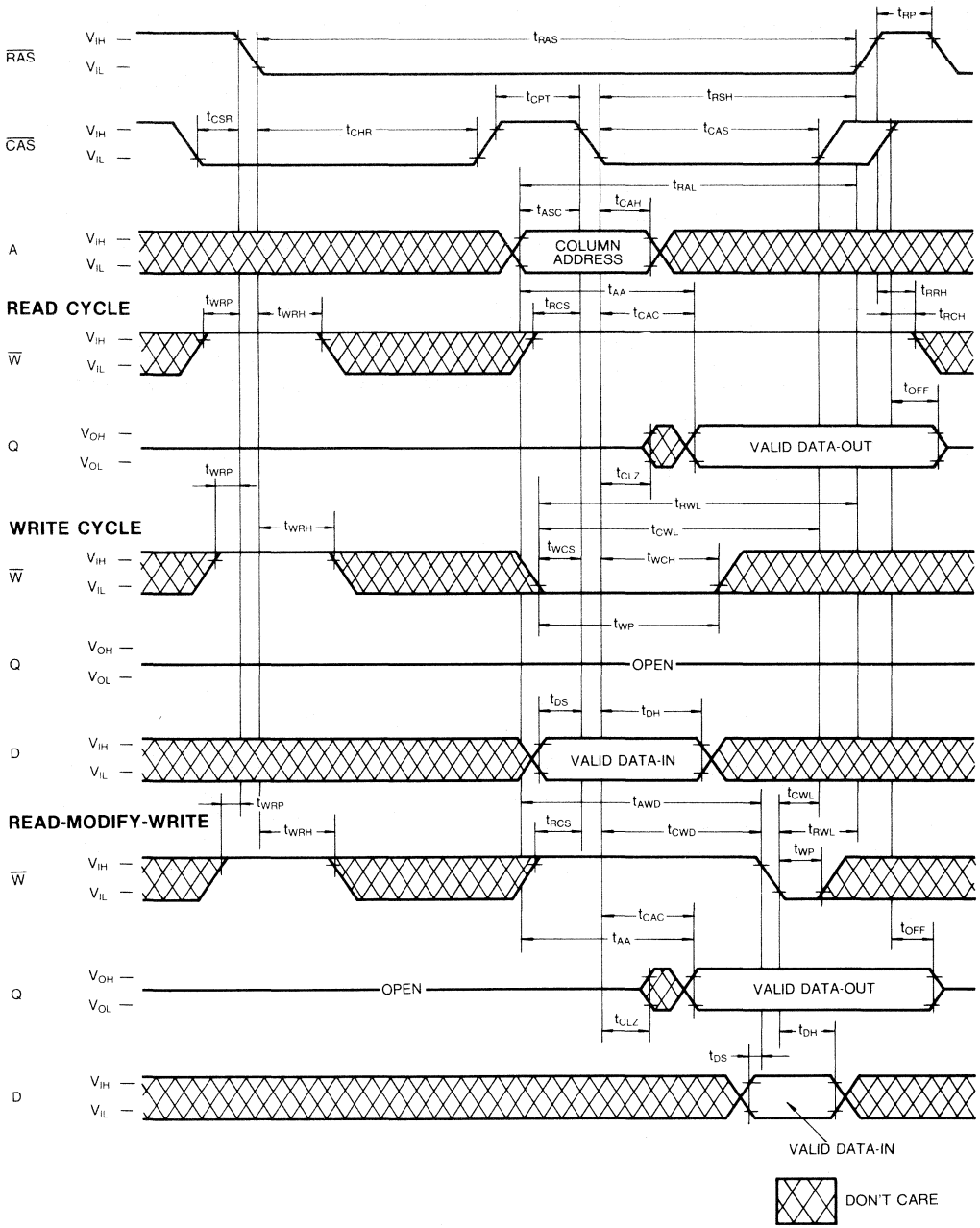


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

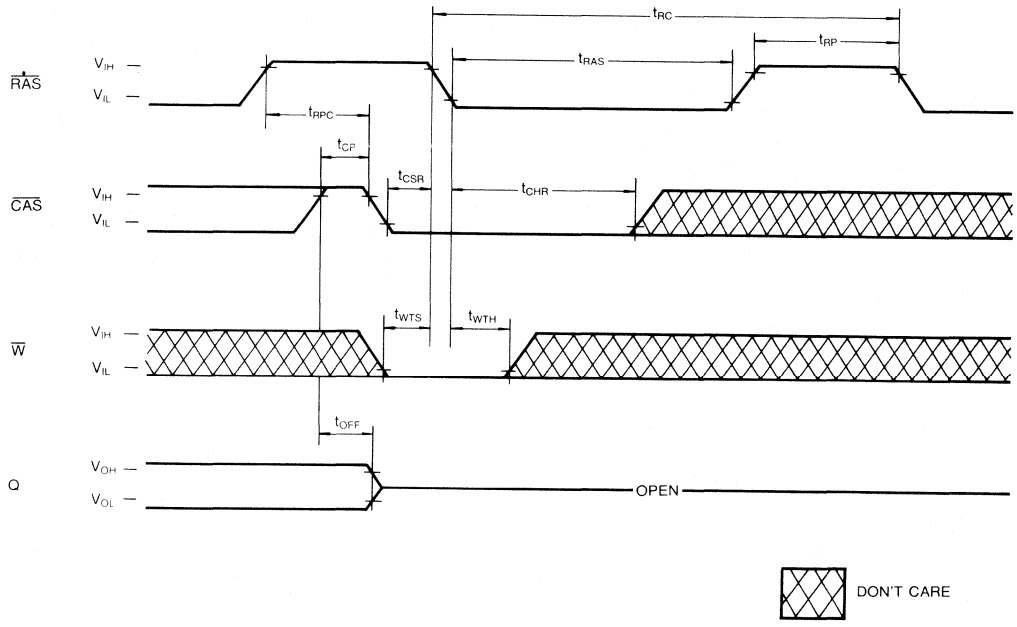
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: D, Address: Don't Care



TEST MODE DESCRIPTION

The KM41C16100 is the RAM organized 16,777,216 words by 1 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0, A_1, A_{11}, also Row address bit A_{11} are not used. If, upon reading, 16 bits are equal (all "1" or "0"s) the Q pin indicates a "1".
If they were not equal, the Q pin would indicate a "0".

In "Test Mode", the 16M DRAM can be tested as if it were a 1M×1 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE "or" "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/16 in cases of N test pattern).

DEVICE OPERATIONS

The KM41C16100 contains 16,777,216 memory locations. Twenty four address bits are required to address a particular memory location. Since the KM41C16100 has only 12 address input pins, time multiplexed addressing is used to input 12 row and 12 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM41C16100 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 12 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C16100 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C16100 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41C16100 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C16100 has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C16100 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C16100 is stored on a tiny capacitor within each memory cell. Due to leakage the

DEVICE OPERATION (Continued)

data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 32 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C16100 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuity is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C16100 hidden refresh cycle is actually a $\overline{CAS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C16100 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM41C16100 has Fast Page mode capability. Fast Page mode capability. Fast Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In Fast Page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A fast Page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page. Up to 2048 memory cells can be accessed with the same row address.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 12 row address bits and 12 column address bits defined as follows:

Row Address—Bits A_0 through A_{11} are supplied by the on-chip refresh counter.

Column Address—Bits A_0 through A_{11} are strobedin by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 2048 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 2048 times so that highs are written into the 2048 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

If $\overline{RAS}$-V_{SS} during power-up, the KM41C16100 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 32msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41C16100

DEVICE OPERATION (Continued)

inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C16100 input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

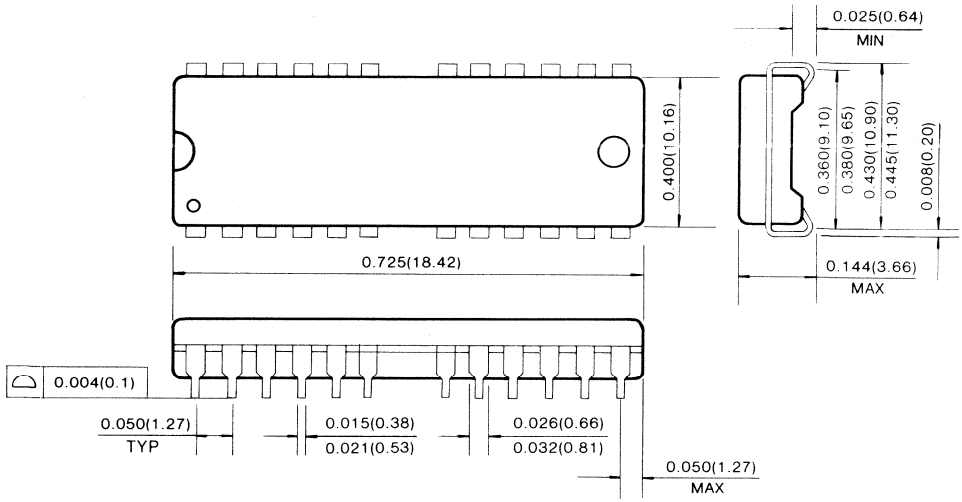
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM41C16100 u;sing the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C16100 and they supply much of the current used by the KM41C16100 during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantlum capacitor around the memory array.

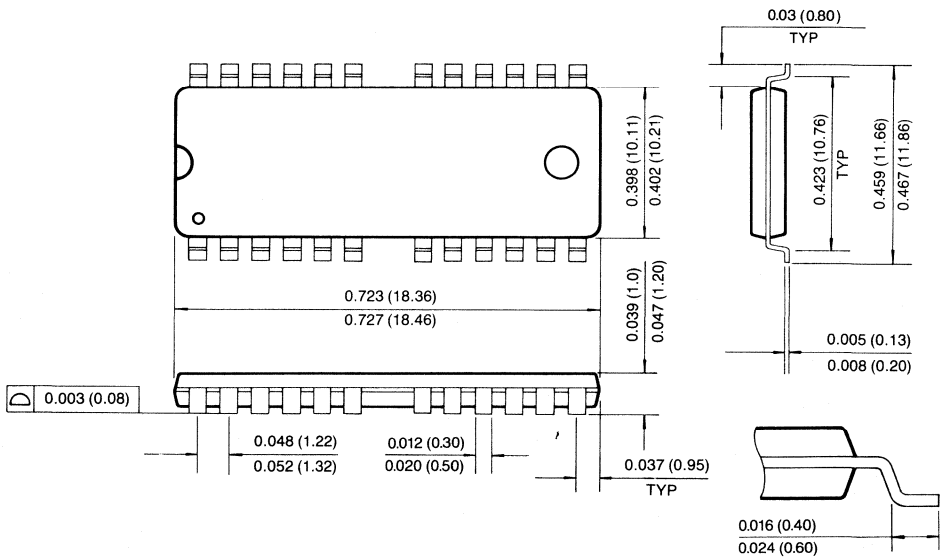
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (Forward and Reverse Type)



16M×1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C16100L-6	60ns	15ns	110ns
KM41C16100L-7	70ns	20ns	130ns
KM41C16100L-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and output**
- **Common I/O using Early Write**
- **Double +5V±10% power supply**
- **2048 cycles/256ms refresh**
- **JEDEC standard pinout**
- **Available in plastic SOJ, TSOP (II) packages**

GENERAL DESCRIPTION

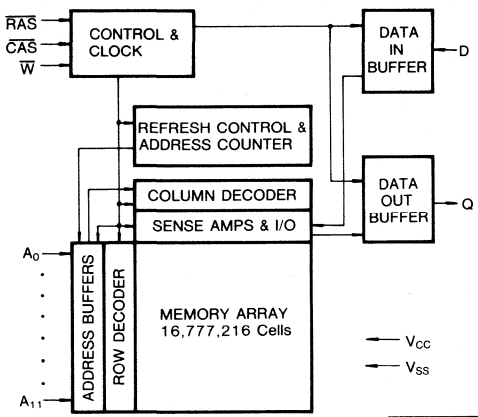
The Samsung KM41C16100L is a CMOS high speed 16,777,216 × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C16100L features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM41C16100L is fabricated using Samsung's advanced CMOS process.

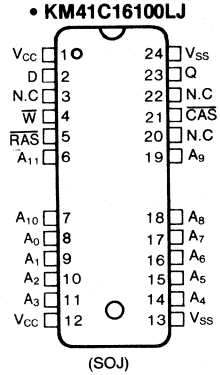
2

FUNCTIONAL BLOCK DIAGRAM



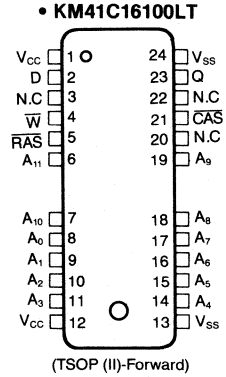
PIN CONFIGURATION (Top Views)

- **KM41C16100LJ**



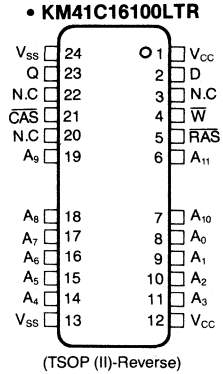
(SOJ)

- **KM41C16100LT**



(TSOP (II)-Forward)

- **KM41C16100LTR**



(TSOP (II)-Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC} = min.)	KM41C16100L-6	I_{CC1}	—	110	mA
	KM41C16100L-7		—	100	mA
	KM41C16100L-8		—	90	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM41C16100L-6	I_{CC3}	—	110	mA
	KM41C16100L-7		—	100	mA
	KM41C16100L-8		—	90	mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC} = min.)	KM41C16100L-6	I_{CC4}	—	90	mA
	KM41C16100L-7		—	80	mA
	KM41C16100L-8		—	70	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		I_{CC5}	—	300	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min.)	KM41C16100L-6	I_{CC6}	—	110	mA
	KM41C16100L-7		—	100	mA
	KM41C16100L-8		—	90	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH}) = V_{CC}-0.2V Input Low Voltage (V_{IL}) = 0.2V $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V DQ_{1-4} = Don't Care T_{RC} = 125 μs, T_{RAS} = t_{RAS} min. ~ 1μs		I_{CC7}	—	500	μA
Standby Current ($\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{OUT} Enable)		I_{CC8}	—	5	mA
Input Leakage Current (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$ = V_{IL}. In I_{CC4}, Address can be changed maximum once while $\overline{CAS}$ = V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	—	5	pF
Input Capacitance (A_0-A_{11})	C_{IN2}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN3}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	KM41C16100L-6		KM41C16100L-7		KM41C16100L-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	130		155		175		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

Parameter	Symbol	KM41C16100L-6		KM41C16100L-7		KM41C16100L-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (2.048 cycles)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	15		20		20		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	60		70		80		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	30		35		40		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	60		70		75		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
Write command set-up time (test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ cycle)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ cycle)	t_{WRH}	10		10		10		ns	

TEST MODE CYCLE

(Note. 12)

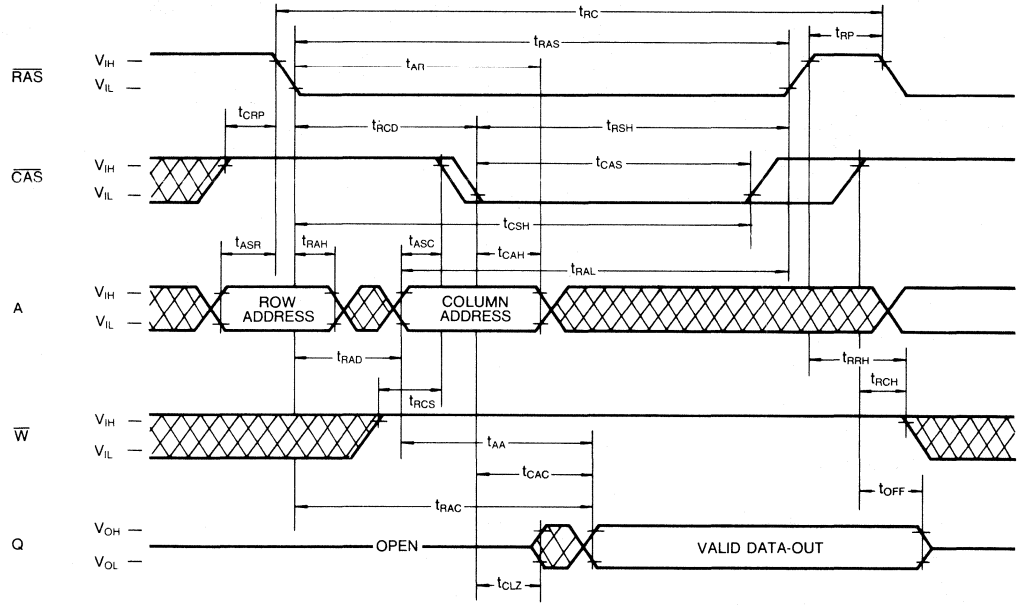
Parameter	Symbol	KM41C16100L-6		KM41C16100L-7		KM41C16100L-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	135		160		180		ns	
Access time from $\overline{RAS}$	t_{RAC}		65		75		85	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,10
$\overline{RAS}$ pulse width	t_{RAS}	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		45		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	20		25		25		ns	7
$\overline{RAS}$ to write enable delay	t_{RWD}	65		75		85		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	35		40		45		ns	7
Fast mode cycle time	t_{PC}	45		50		55		ns	
Fast page mode read-modefy-write	t_{PRWC}	65		75		80		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3

NOTES

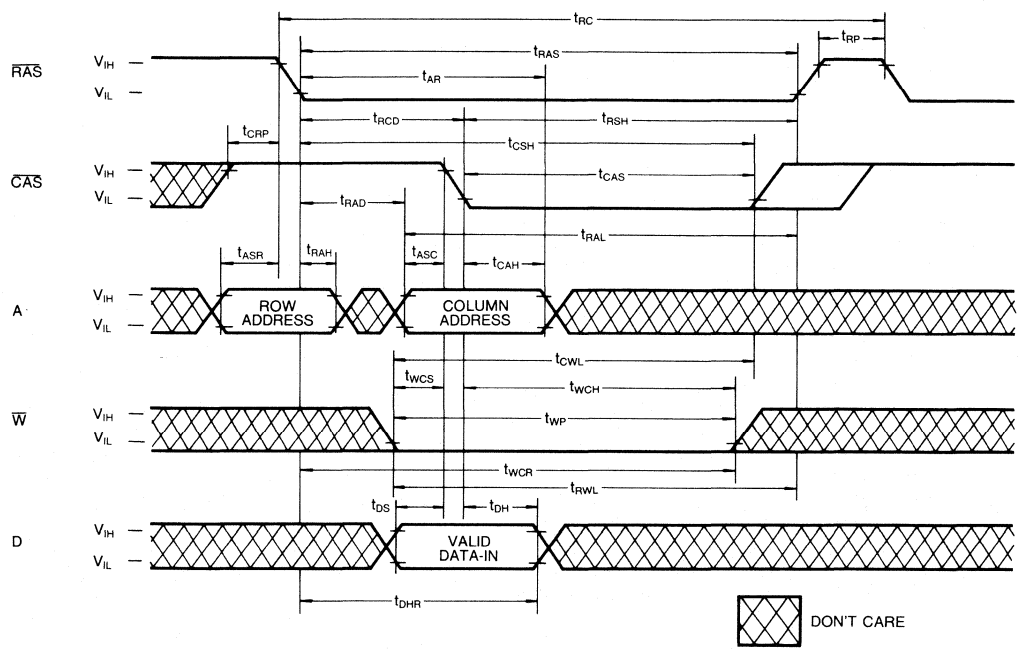
1. An initial pause of 200μs is required after power up followed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only Refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF(max)}$ and $t_{OEZ(max)}$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

TIMING DIAGRAMS

READ CYCLE

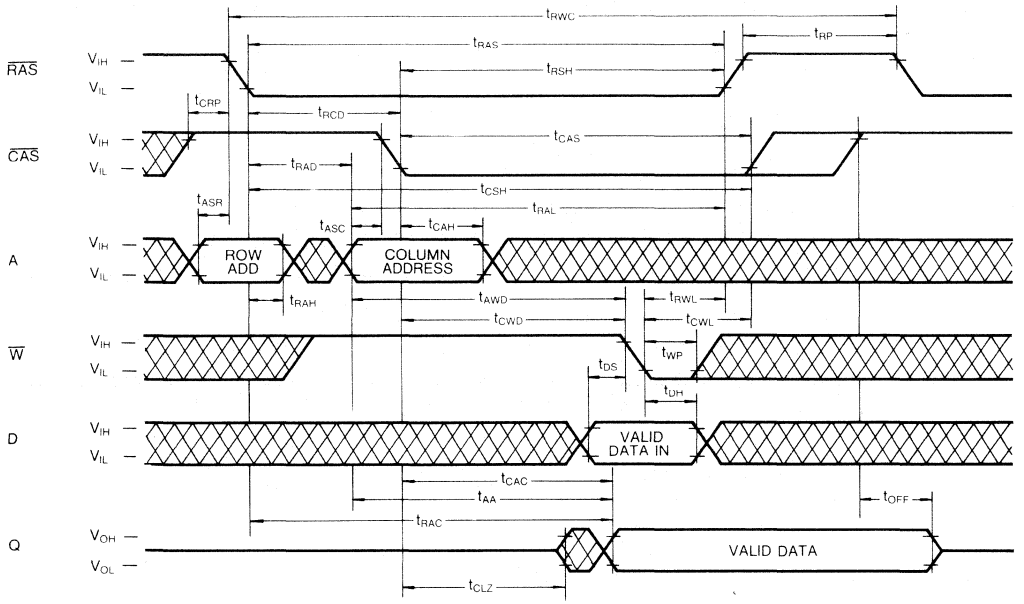


WRITE CYCLE (EARLY WRITE)

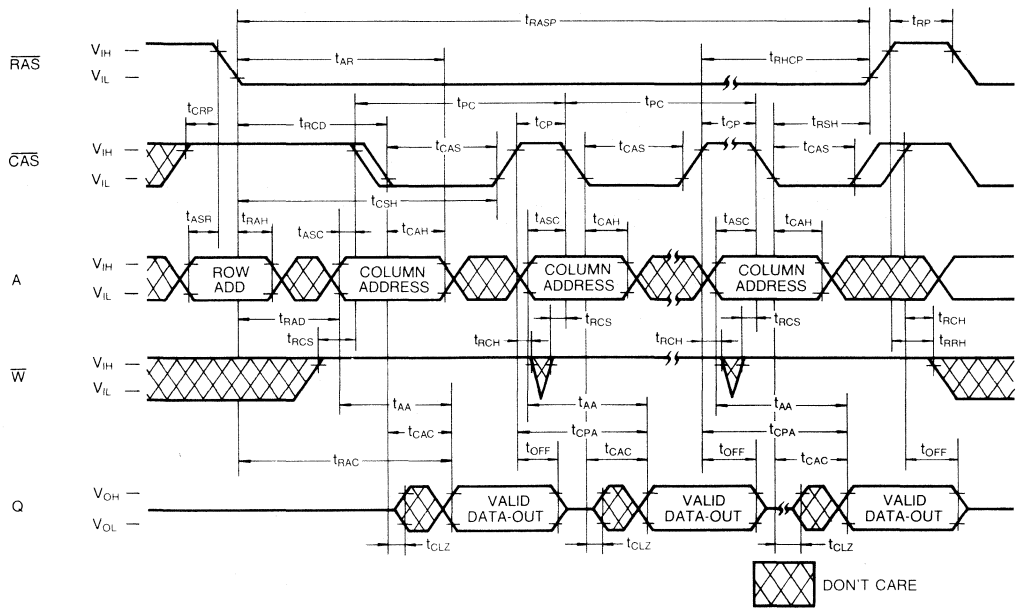


TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

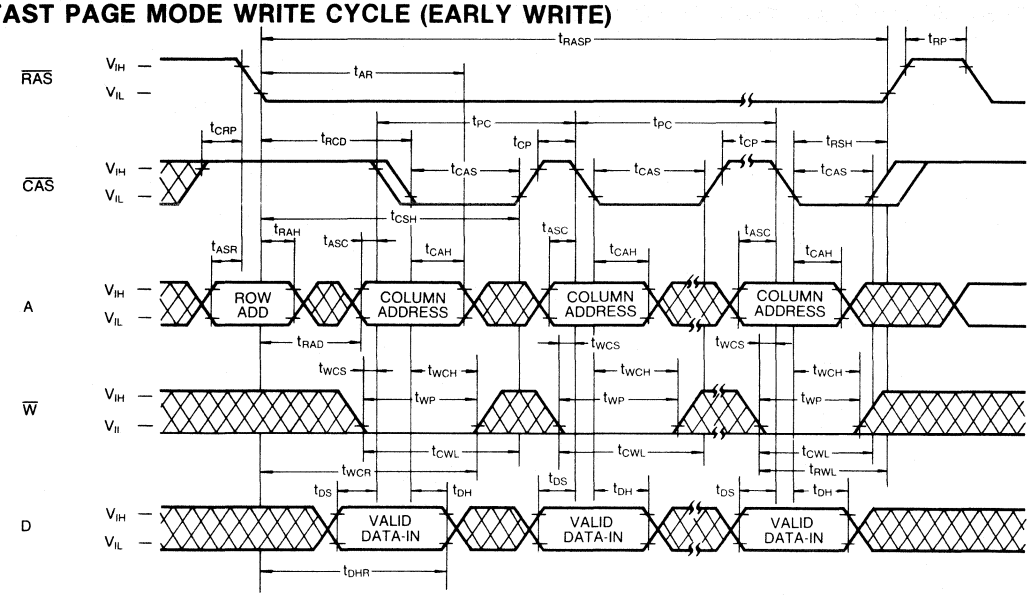


FAST PAGE MODE READ CYCLE

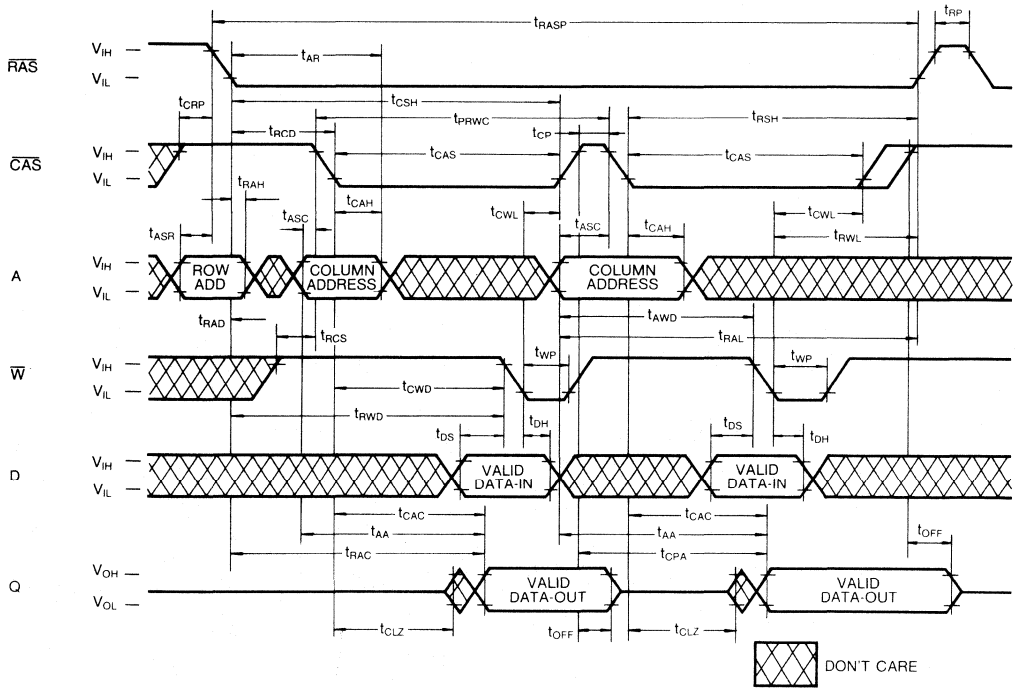


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



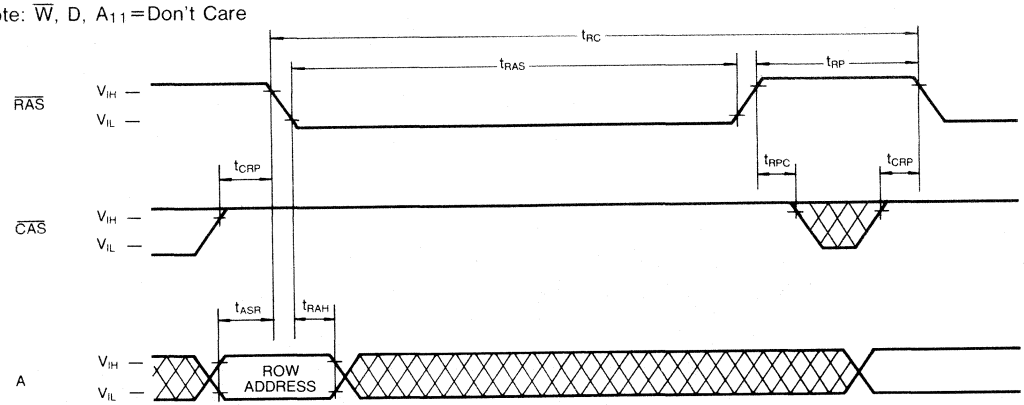
FAST PAGE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

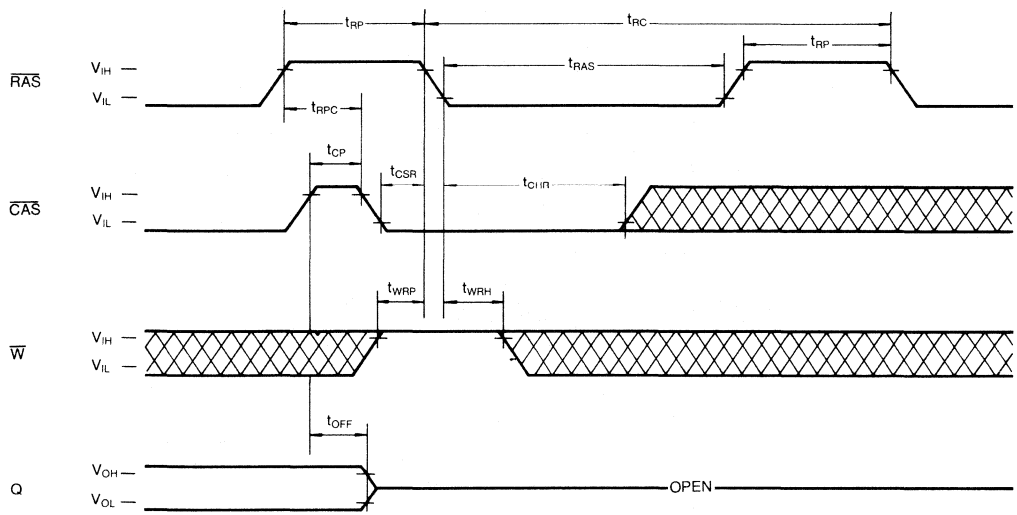
$\overline{RAS}$ ONLY REFRESH CYCLE

Note: $\overline{W}$, D, A_{11}=Don't Care



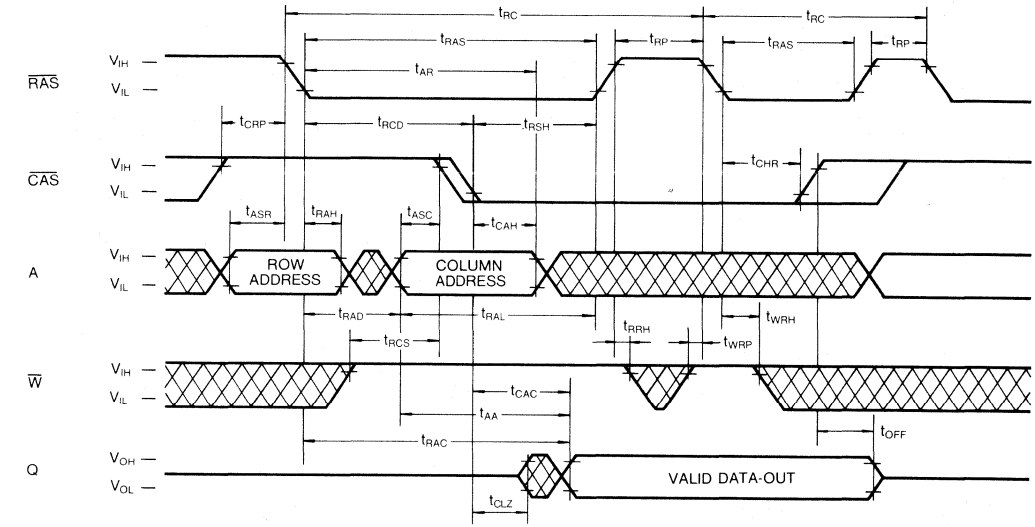
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: Address=Don't Care

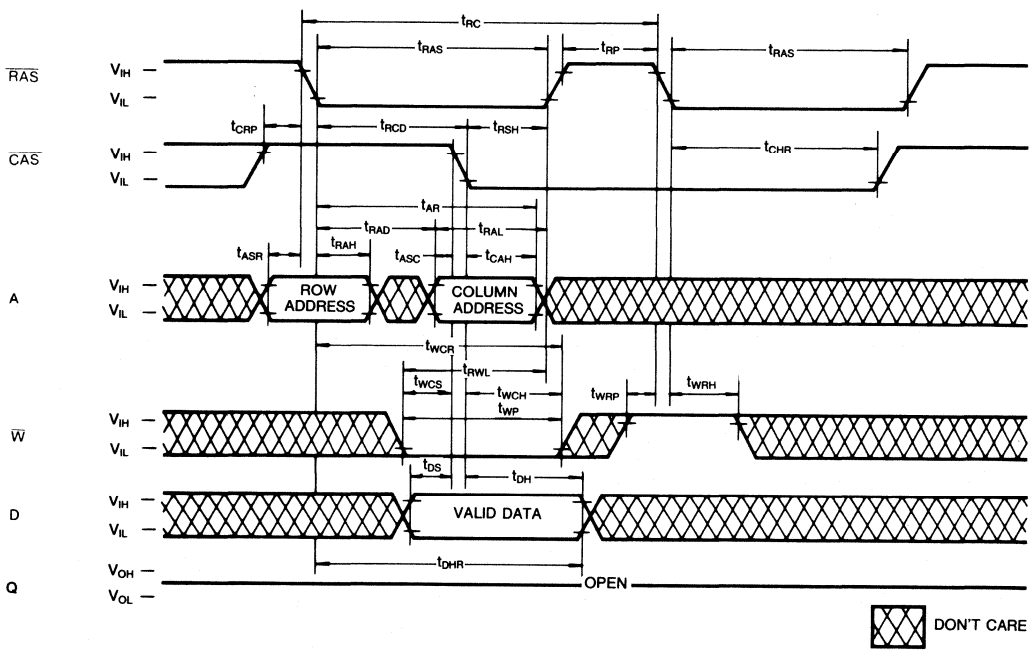


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

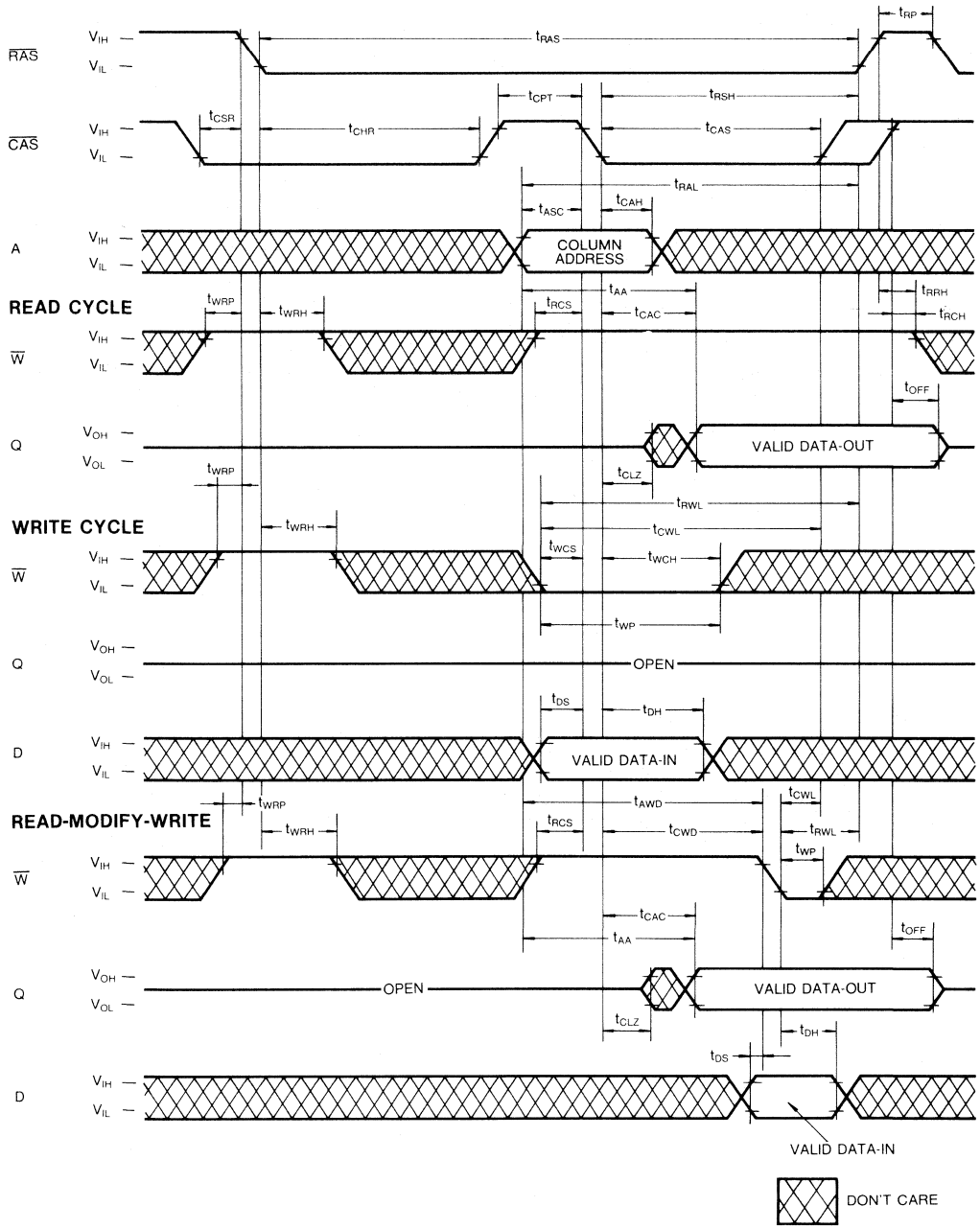


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

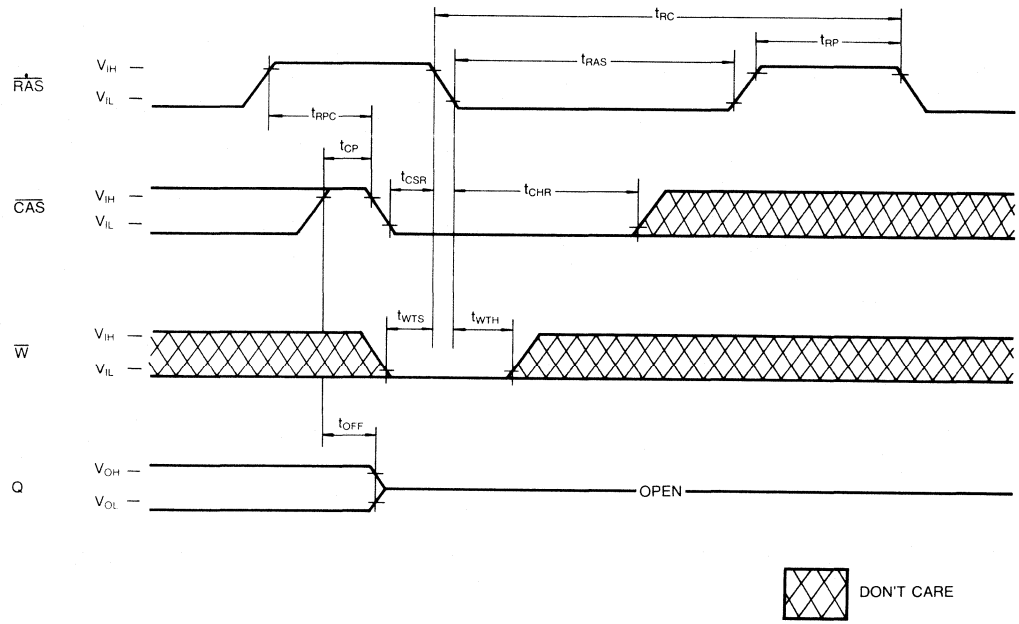
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: D, Address: Don't Care



TEST MODE DESCRIPTION

The KM41C16100L is the RAM organized 16,777,216 words by 1 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0, A_1, A_{11}, also Row address bit A_{11} are not used. If, upon reading, 16 bits are equal (all "1" or "0"s) the Q pin indicates a "1".
If they were not equal, the Q pin would indicate a "0".

In "Test Mode", the 16M DRAM can be tested as if it were a 1M×1 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE "or" "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/16 in cases of N test pattern).

DEVICE OPERATIONS

The KM41C16100L contains 16,777,216 memory locations. Twenty-four address bits are required to address a particular memory location. Since the KM41C16100L has only 12 address input pins, time multiplexed addressing is used to input 12 row and 12 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM41C16100L begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 12 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41C16100L cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C16100L begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

The KM41C16100L can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$, $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. The cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C16100L has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is high (V_{IH}), the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41C16100L operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

DEVICE OPERATION (Continued)

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C16100L is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 256 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41C16100L has $\overline{CAS}$-before-RAS on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM41C16100L hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C16100L by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general RAS-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM41C16100L has Fast page mode capability. Fast page mode memory cycles provides faster access and lower power dissipation than normal memory cycles. In Fast page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page. Up to 2048 memory cells can be accessed with the same row address.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 12 row address bits and 12 column address bits defined as follows:

Row Address — Bits A_0 through A_{11} are supplied by tthe on-chip refresh counter.

Column Address — Bits A_0 through A_{11} are strobed-in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 2048 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 2048 times so that highs are written into the 2048 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

DEVICE OPERATION (Continued)

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM41C16100L could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. Eight initialization cycles are also required after any 256 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41C16100L inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C16100L input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

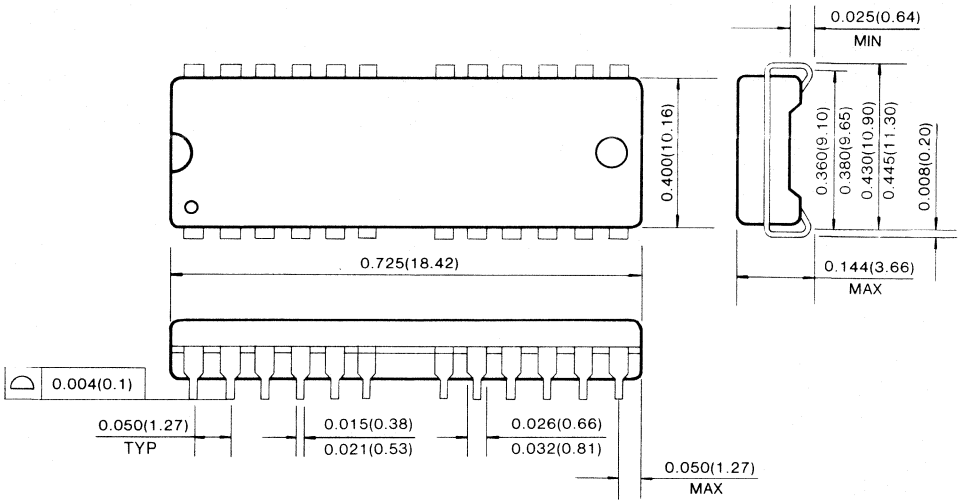
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM41C16100L using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C16100L and they supply much of the current used by the KM41C16100L during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

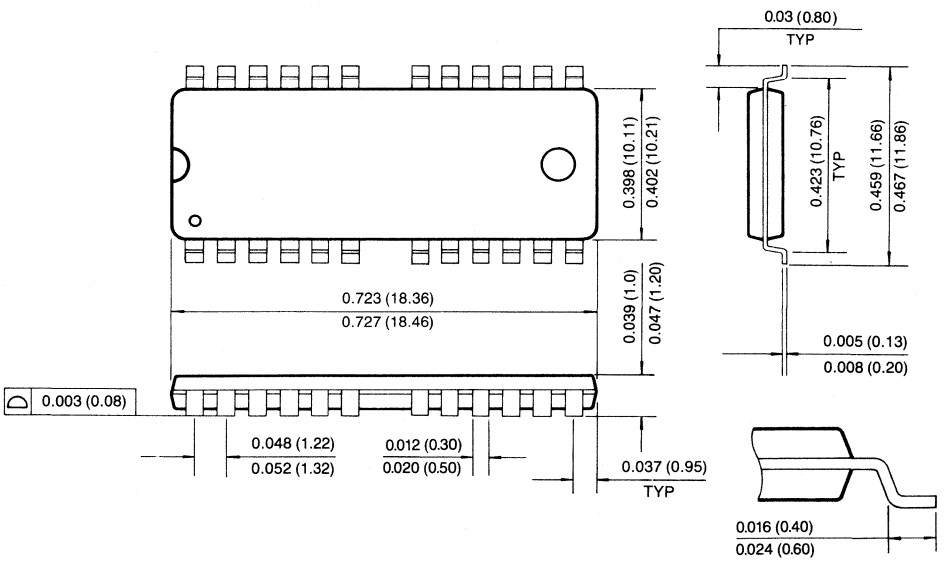
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (Forward and Reverse Type)



4M×4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C4000-6	60ns	15ns	110ns
KM44C4000-7	70ns	20ns	130ns
KM44C4000-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Double +5V±10% power supply**
- **4096 cycles/64ms refresh**
- **JEDEC standard pinout**
- **Available in plastic SOJ, TSOP (II) packages**

GENERAL DESCRIPTION

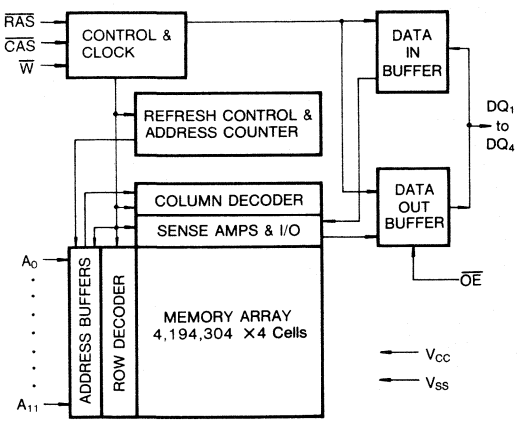
The Samsung KM44C4000 is a high speed CMOS 4,194,304×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C4000 features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and outputs are fully TTL compatible.

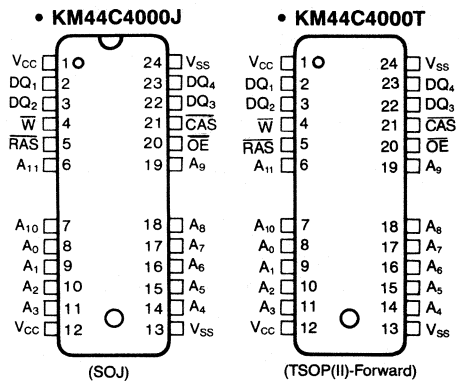
The KM44C4000 is fabricated using Samsung's advanced CMOS process.

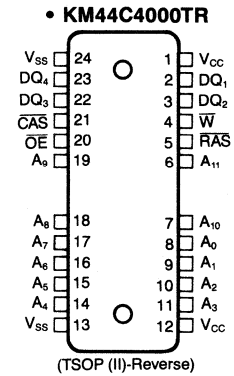
2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)





Pin Name	Pin Function
A_0-A_{11}	Address Inputs
DQ_1-DQ_4	Data In/Data Out
$\overline{OE}$	Data out Enable
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM44C4000-6	I_{CC1}	—	90	mA
	KM44C4000-7		—	80	mA
	KM44C4000-8		—	70	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @ t_{RC}=min.)	KM44C4000-6	I_{CC3}	—	90	mA
	KM44C4000-7		—	80	mA
	KM44C4000-8		—	70	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @ t_{PC}=min.)	KM44C4000-6	I_{CC4}	—	80	mA
	KM44C4000-7		—	70	mA
	KM44C4000-8		—	60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM44C4000-6	I_{CC6}	—	90	mA
	KM44C4000-7		—	80	mA
	KM44C4000-8		—	70	mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL}, D_{OUT} Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} address transition should be changed only once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address transition should be changed only once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{11})	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	KM44C4000-6		KM44C4000-7		KM44C4000-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

Parameter	Symbol	KM44C4000-6		KM44C4000-7		KM44C4000-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (4,096 cycles)	t_{REF}		64		64		64	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	85		100		105		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	15		20		20		ns	
Write command set-up time (test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ cycle)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ cycle)	t_{WRH}	10		10		10		ns	

TEST MODE CYCLE

(Note. 12)

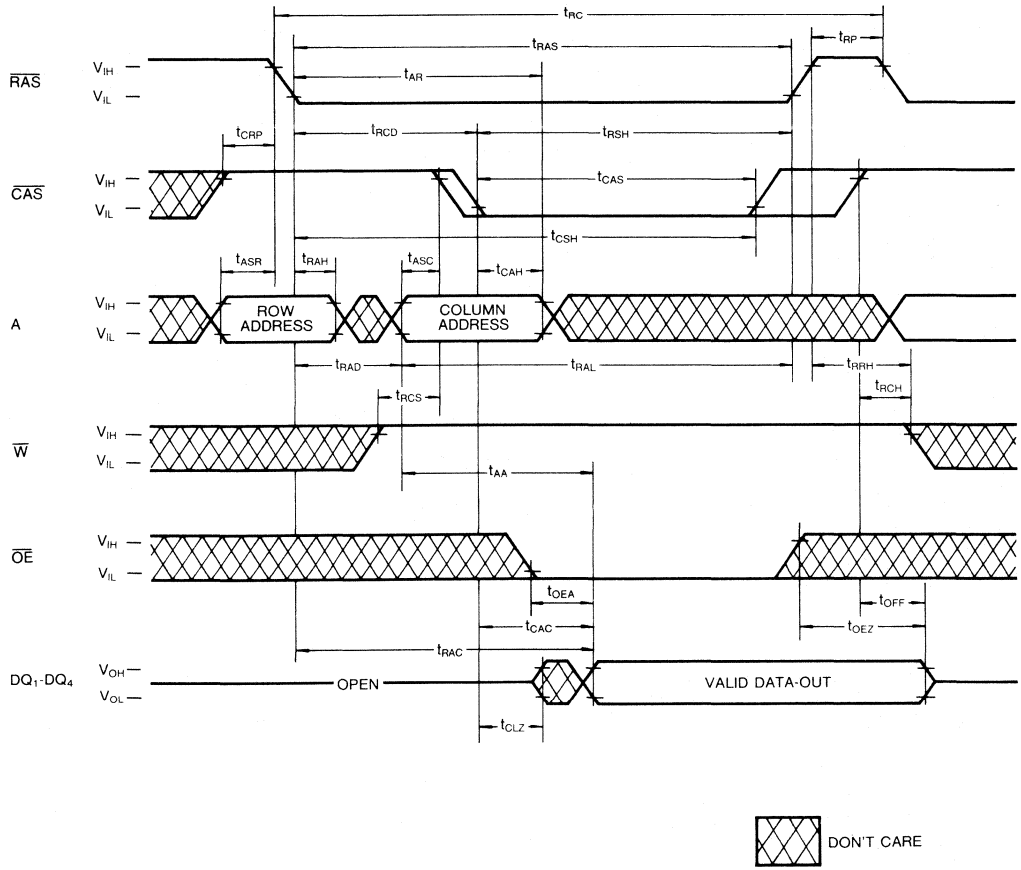
Parameter	Symbol	KM44C4000-6		KM44C4000-7		KM44C4000-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	160		190		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		45		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	45		55		55		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	90		105		115		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	60		70		75		ns	8
Fast mode cycle time	t_{PC}	45		50		55		ns	
Fast page mode read-modefy-write	t_{PRWC}	90		105		110		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3
$\overline{OE}$ access time	t_{OEA}		20		25		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		25		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only Refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF(max)}$ and $t_{OEZ(max)}$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

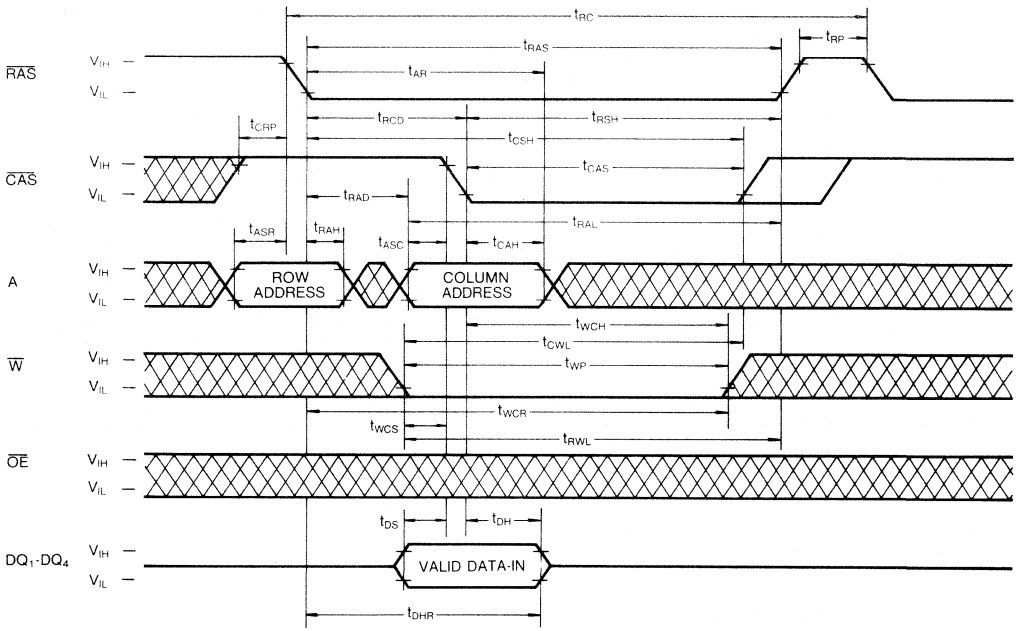
TIMING DIAGRAMS

READ CYCLE

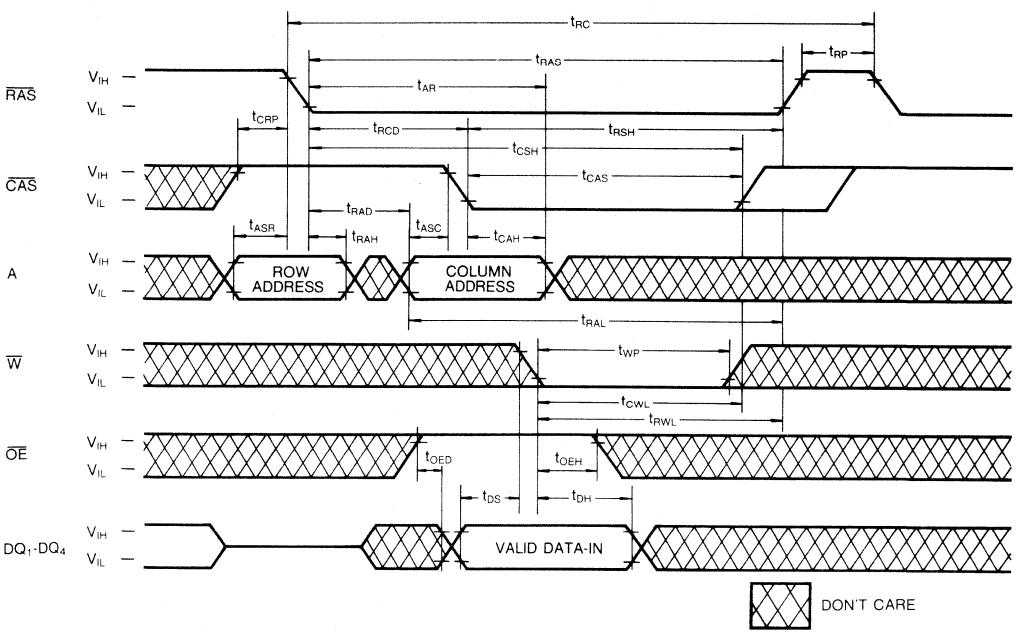


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)

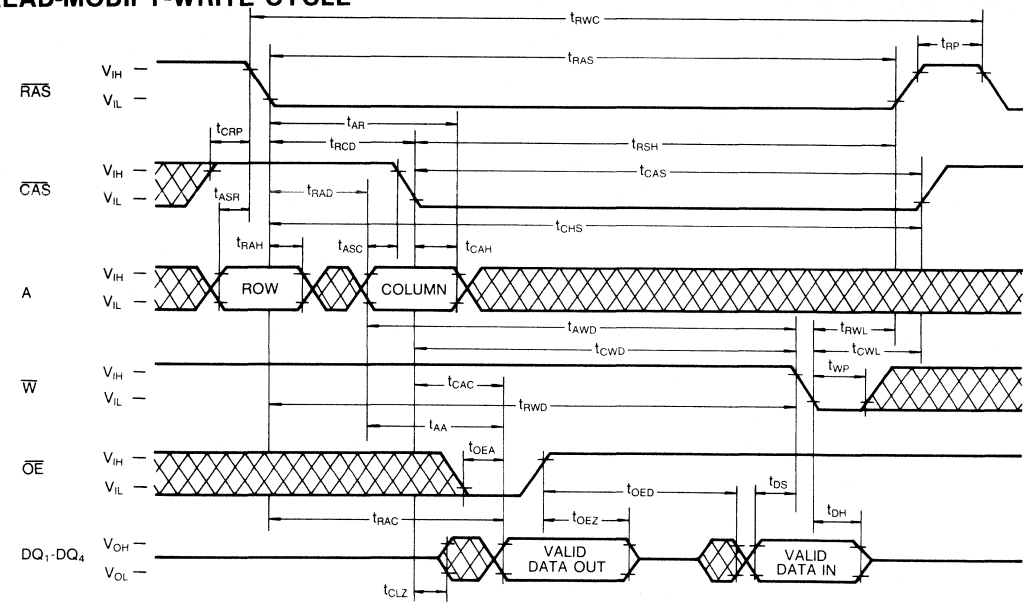


WRITE CYCLE (OE CONTROLLED WRITE)

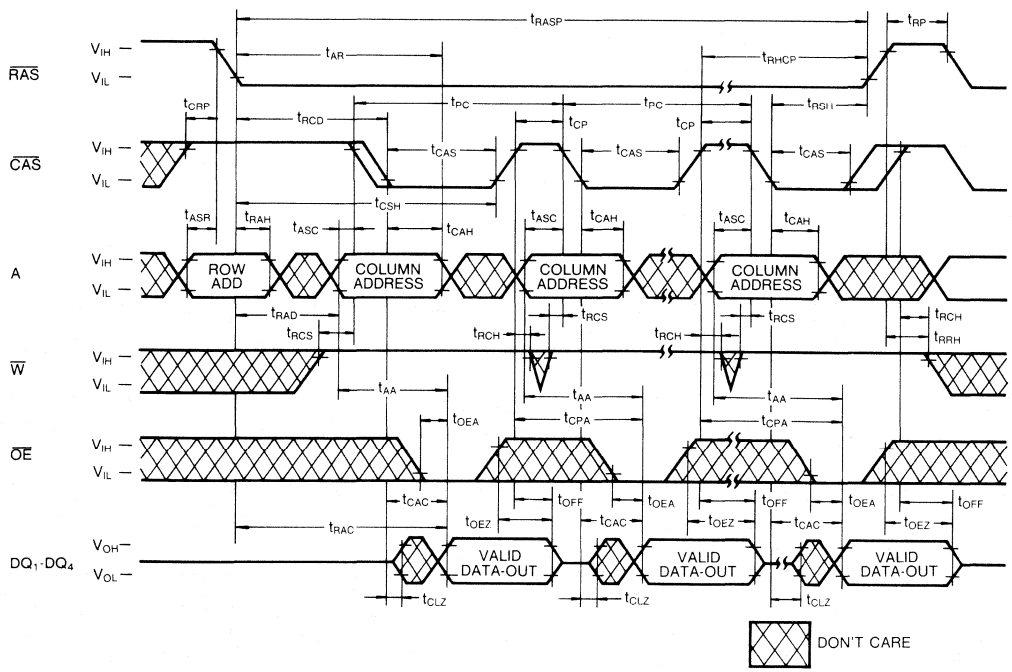


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE

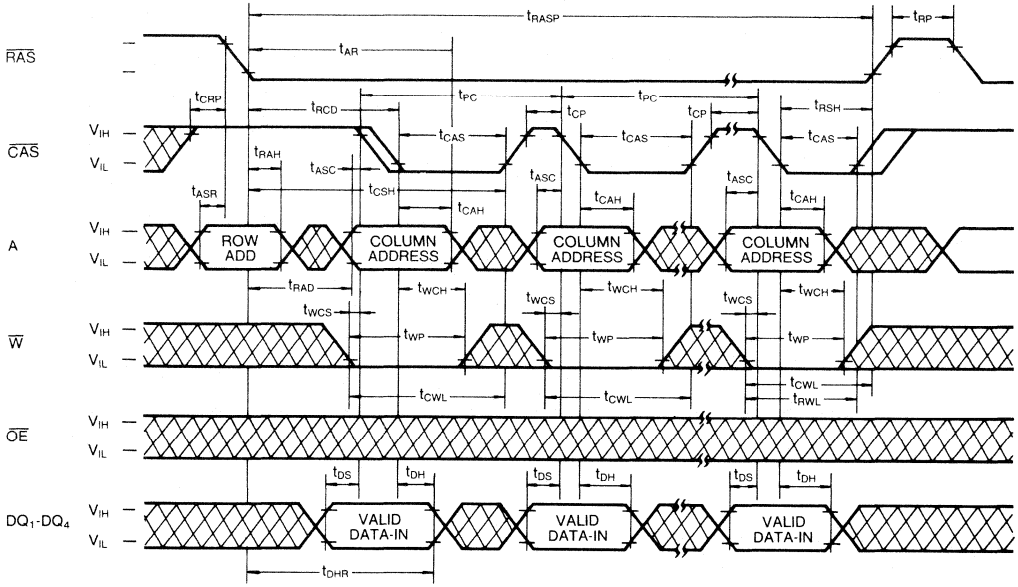


FAST PAGE MODE READ CYCLE

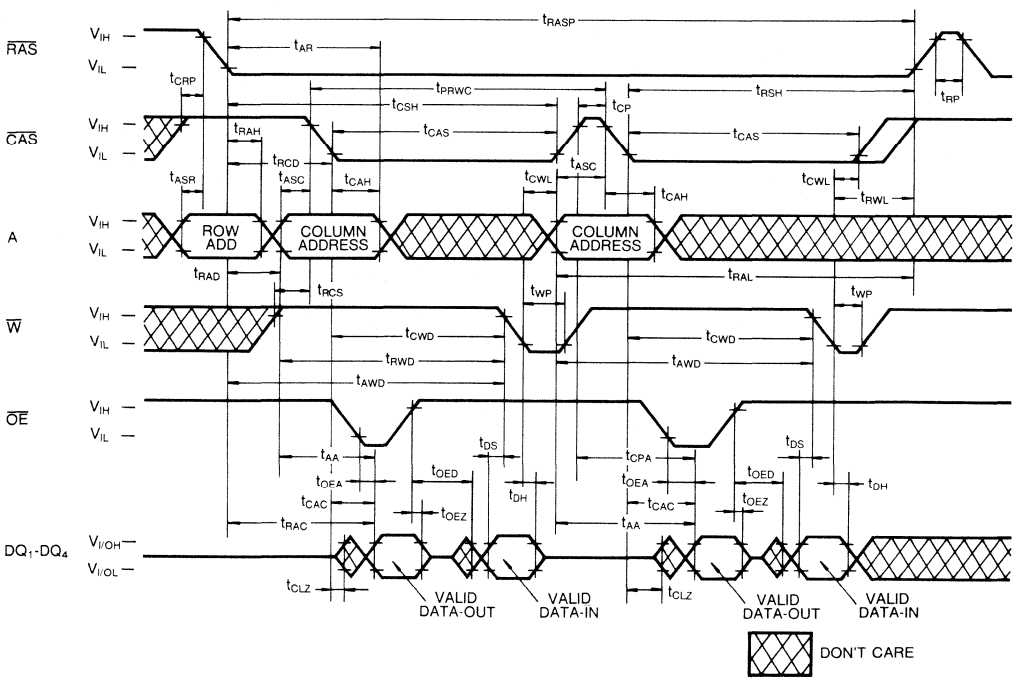


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



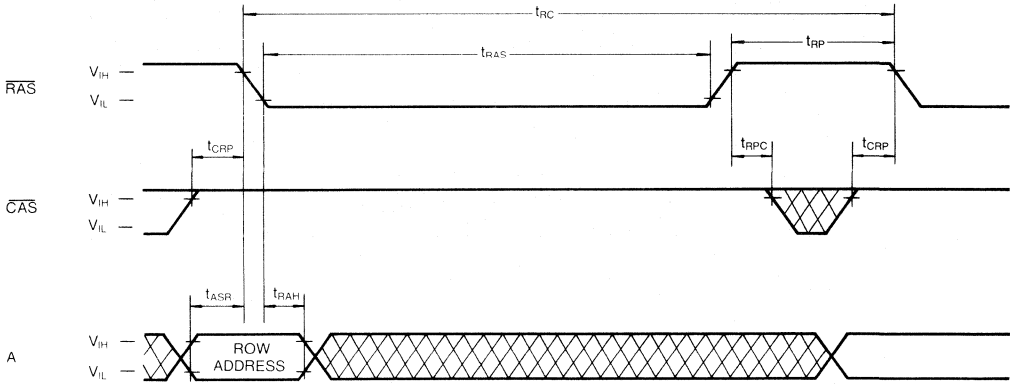
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

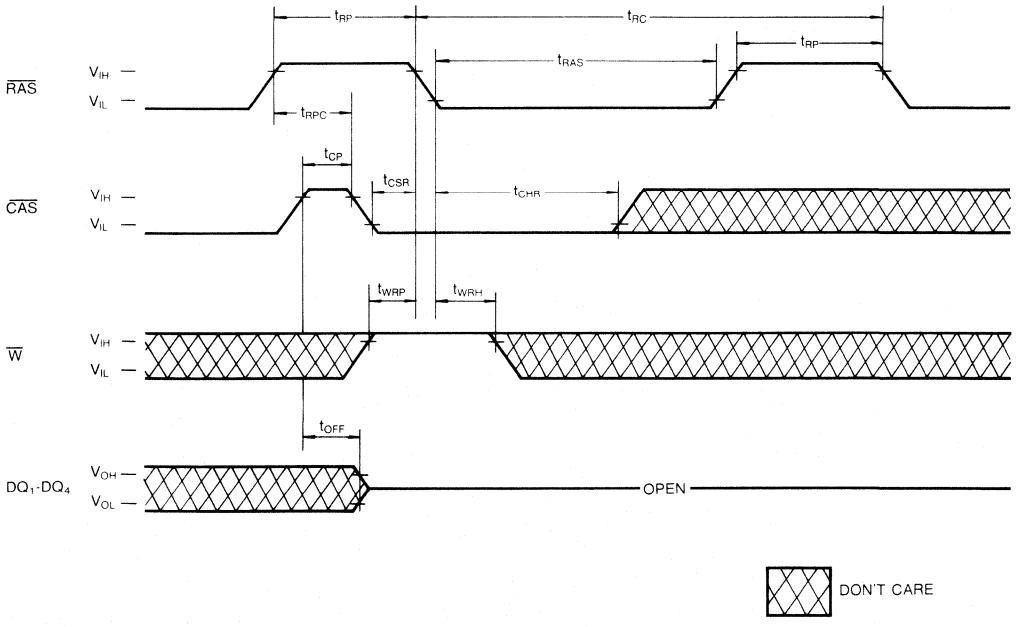
$\overline{RAS}$ ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



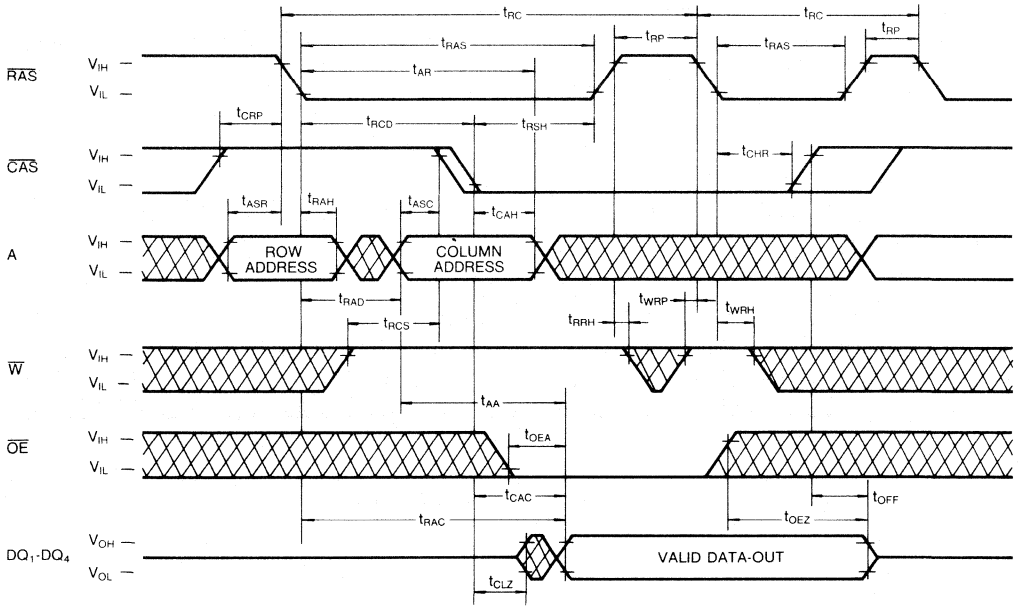
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: $\overline{OE}$, Address=Don't Care

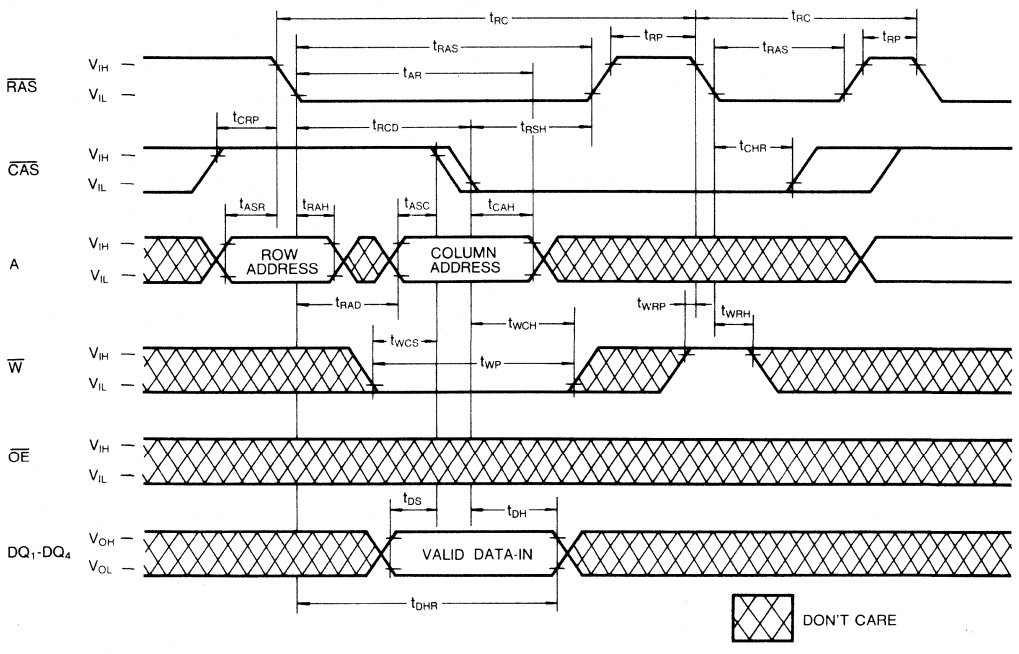


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

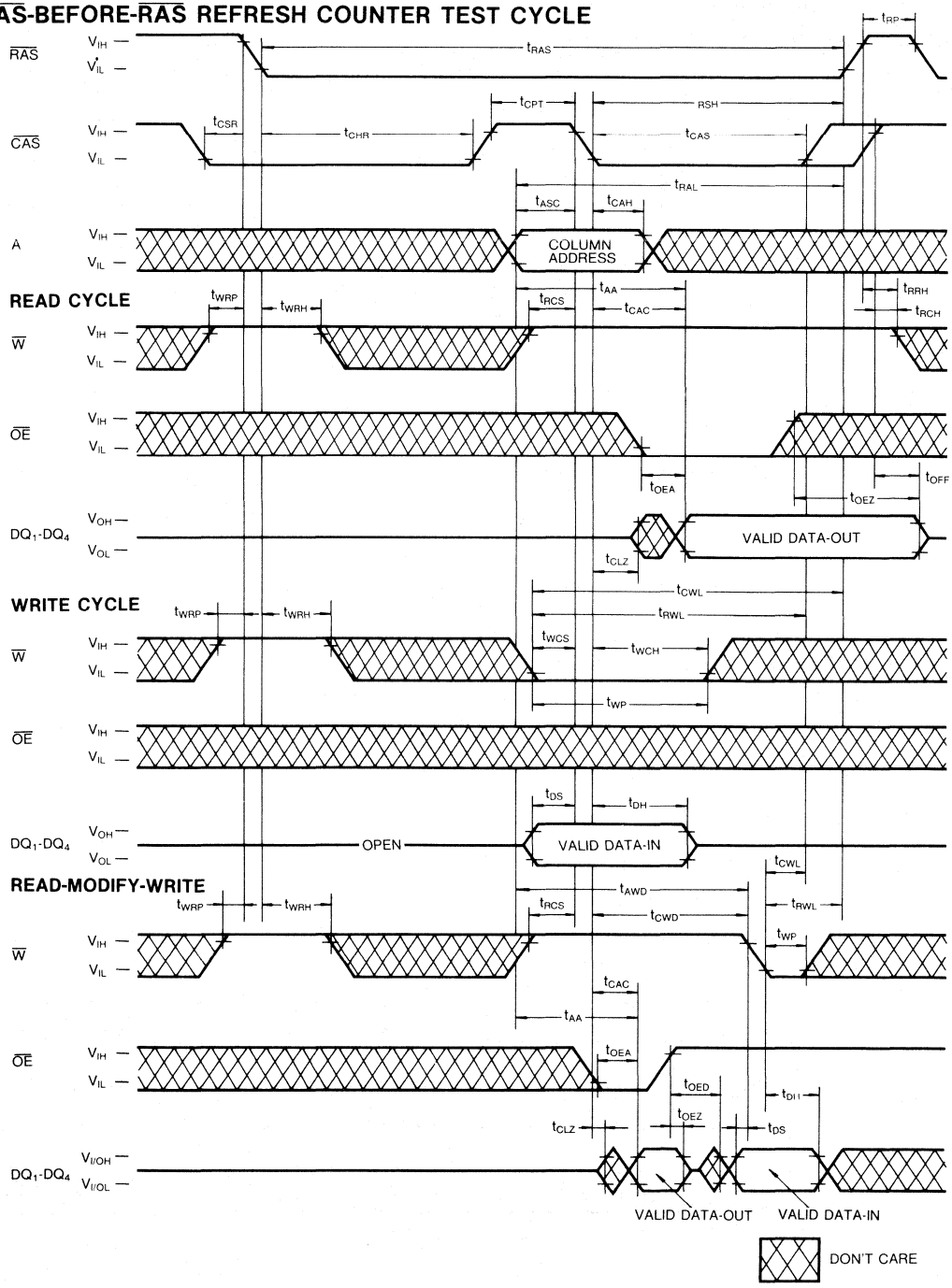


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

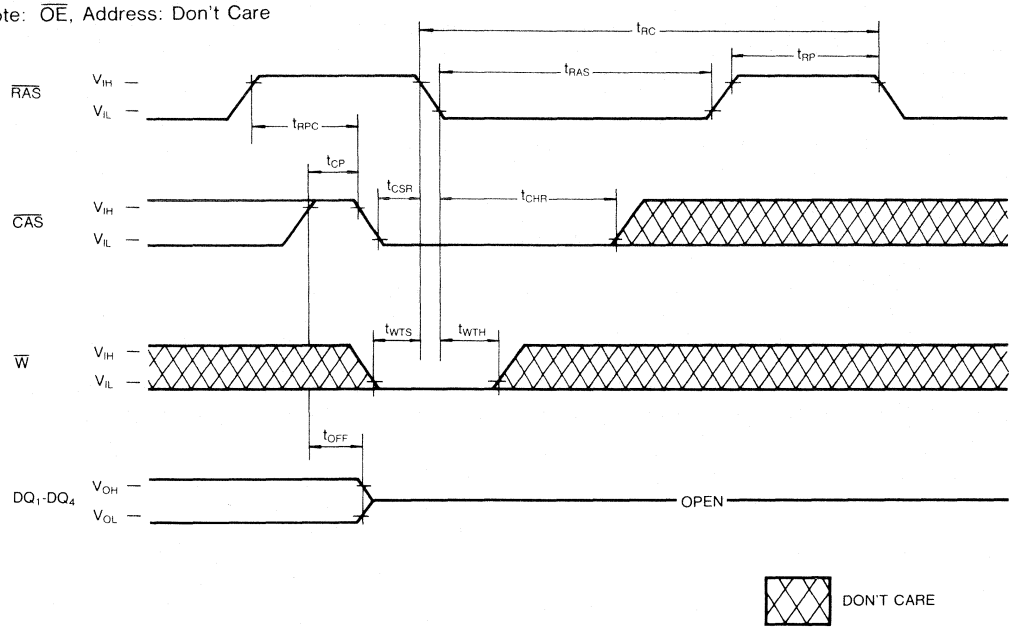
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



TEST MODE DESCRIPTION

The KM44C4000 is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0 and $A_1$are not used. If, upon reading, four bits on one D/Q pin are equal (all "1"s or "0"s) the D/Q pin indicates a "1". If they were not equal, the D/Q pin would indicate a "0". In "Test Mode", the 4M×4 DRAM can be tested as if it were a 1M×4 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE "or" "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

DEVICE OPERATIONS

The KM44C4000 contains 4,194,304×4 memory locations. Twenty two address bit are required to address a particular 4-bit word in the memory array. Since the KM44C4000 has only 12 address input pins, time multiplexed addressing is used to input 12 row (A_0-A_{11}) and 10 column (A_0-A_9) addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM44C4000 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins(A_0-A_9) is changed from a row address to a column address and is strobed in by $\overline{CAS}$. At that time, the status of the input pins (A_{10}, A_{11}) is don't care. This is the beginning of any KM44C4000 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C4000 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAC}(max), then the access time to valid data is specified by r_{RAC}(min). However, If $\overline{CAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max). The KM44C4000 has common data I/O pins.

The this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44C4000 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CAS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the three state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44C4000 has a three-state output buffer which is controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever $\overline{CAS}$ and $\overline{OE}$ are high (V_{IH}), the outputs are in the high impedance state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C4000 operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z output state: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} are not met)

Refresh

The data in the KM44C4000 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 64 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 4096 row address (A_0-A_{11}).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C4000 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuity is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C4000 hidden refresh cycle is actually a $\overline{CAS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C4000 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 12 row address bits and 10 column address bits defined as follows:

Row Address—Bits A_0 through A_{11} are supplied by the on-chip refresh counter.

Column Address—Bits A_0 through A_9 are strobedin by the falling edge of $\overline{CAS}$ as in a normal memory cycle. The status of A_{10}, A_{11} is don't care.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 4096 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 4096 times so that highs are written into the 4096 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

If $\overline{RAS}$-V_{SS} during power-up, the KM44C4000 could possibly begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid

DEVICE OPERATION (Continued)

VIH in order to minimize the power-up current.

An initial pause of 200 usec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 64 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C4000 inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C4000 input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

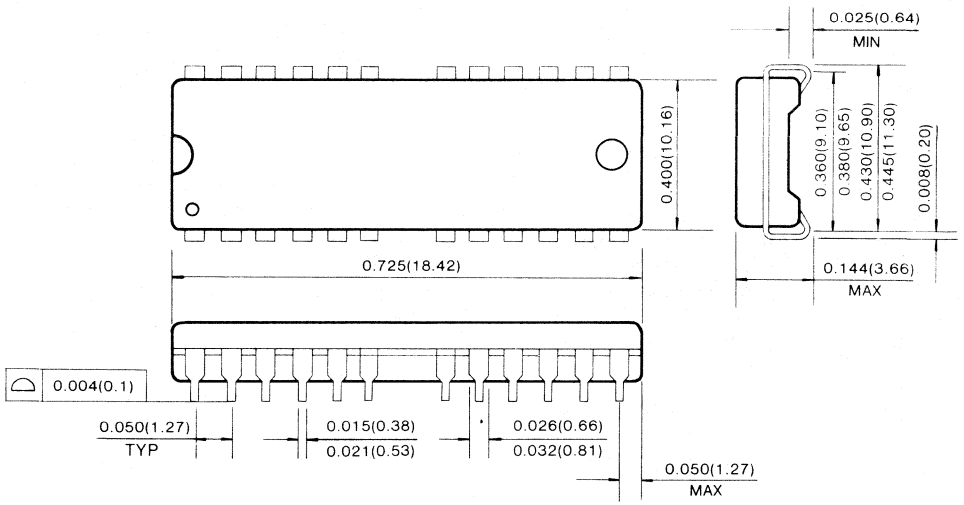
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM44C4000 using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C4000 and they supply much of the current used by the KM44C4000 during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1uF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

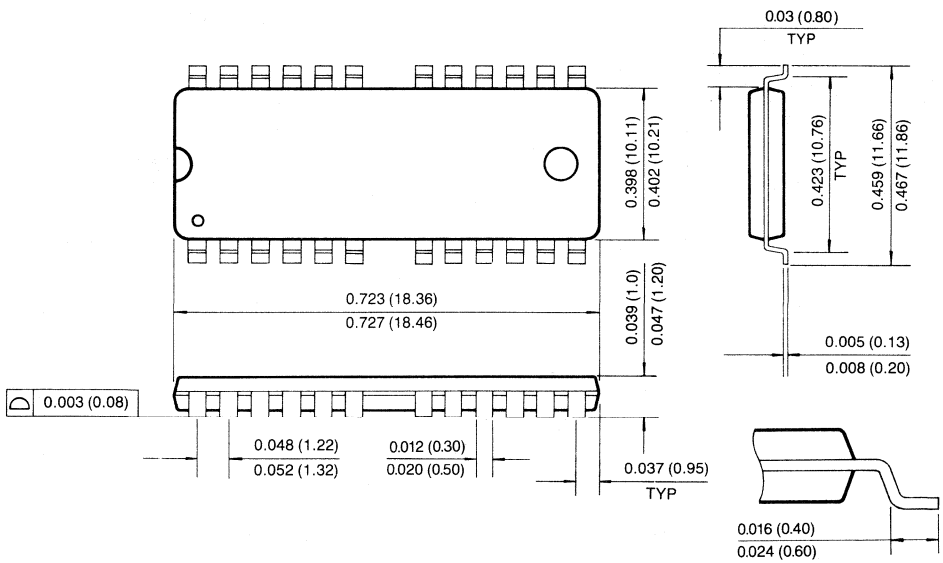
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (Forward and Reverse Type)



4M×4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C4000L-6	60ns	15ns	110ns
KM44C4000L-7	70ns	20ns	130ns
KM44C4000L-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Double +5V±10% power supply**
- **4096 cycles/256ms refresh**
- **JEDEC standard pinout**
- **Available in plastic SOJ, TSOP (II) packages**

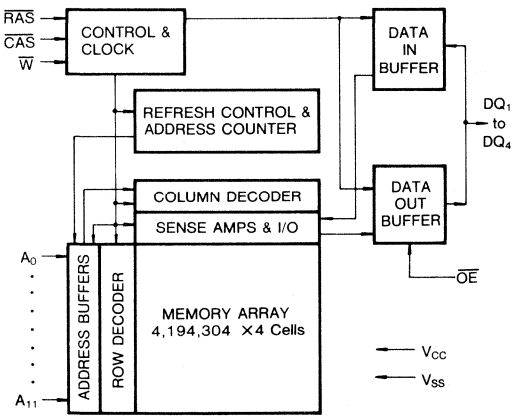
GENERAL DESCRIPTION

The Samsung KM44C4000L is a CMOS high speed 4,194,304 x 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

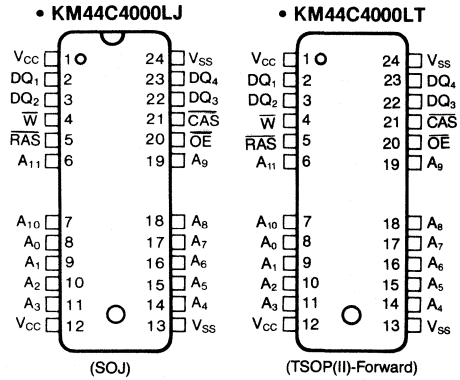
The KM44C4000L features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

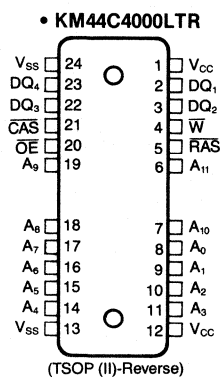
The KM44C4000L is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)





Pin Name	Pin Function
A_0-A_{11}	Address Inputs
DQ_1-DQ_4	Data In/Data Out
$\overline{OE}$	Data out Enable
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC} = min.)	KM44C4000L-6	I_{CC1}	—	90	mA
	KM44C4000L-7		—	80	mA
	KM44C4000L-8		—	70	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM44C4000L-6	I_{CC3}	—	90	mA
	KM44C4000L-7		—	80	mA
	KM44C4000L-8		—	70	mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC} = min.)	KM44C4000L-6	I_{CC4}	—	80	mA
	KM44C4000L-7		—	70	mA
	KM44C4000L-8		—	60	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		I_{CC5}	—	300	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min.)	KM44C4000L-6	I_{CC6}	—	90	mA
	KM44C4000L-7		—	80	mA
	KM44C4000L-8		—	70	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH}) = V_{CC}-0.2V Input Low Voltage (V_{IL}) = 0.2V $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V DQ_{1-4} = Don't Care T_{RC} = 62.5μs, T_{RAS} = t_{RAS} min. ~ 1μs		I_{CC7}	—	500	μA
Standby Current ($\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{OUT} Enable)		I_{CC8}	—	5	mA
Input Leakage Current (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$ = V_{IL}. In I_{CC4}, Address can be changed maximum once while $\overline{CAS}$ = V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{11})	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	KM44C4000L-6		KM44C4000L-7		KM44C4000L-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

Parameter	Symbol	KM44C4000L-6		KM44C4000L-7		KM44C4000L-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (4,096 cycles)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	85		100		105		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	15		20		20		ns	
Write command set-up time (test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ cycle)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ cycle)	t_{WRH}	10		10		10		ns	

TEST MODE CYCLE

(Note. 12)

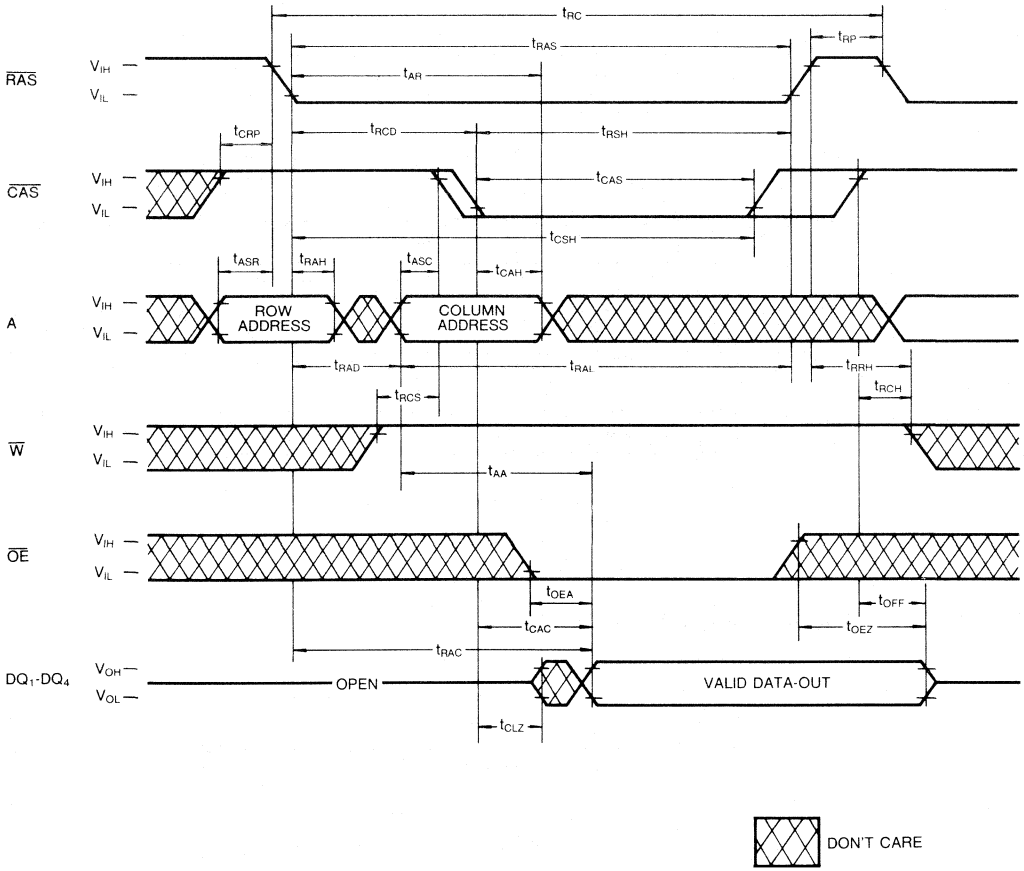
Parameter	Symbol	KM44C4000L-6		KM44C4000L-7		KM44C4000L-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	160		190		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		45		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	45		55		55		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	90		105		115		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	60		70		75		ns	8
Fast mode cycle time	t_{PC}	45		50		55		ns	
Fast page mode read-modefy-write	t_{PRWC}	90		105		110		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3
$\overline{OE}$ access time	t_{OEA}		20		25		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		25		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only Refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF(max)}$ and $t_{OEZ(max)}$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

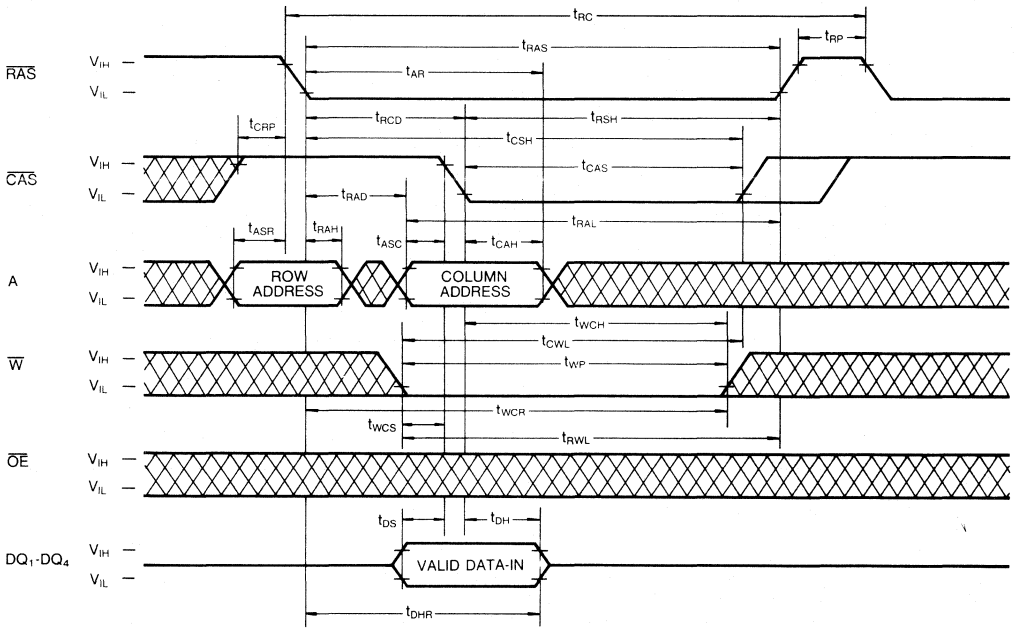
TIMING DIAGRAMS

READ CYCLE

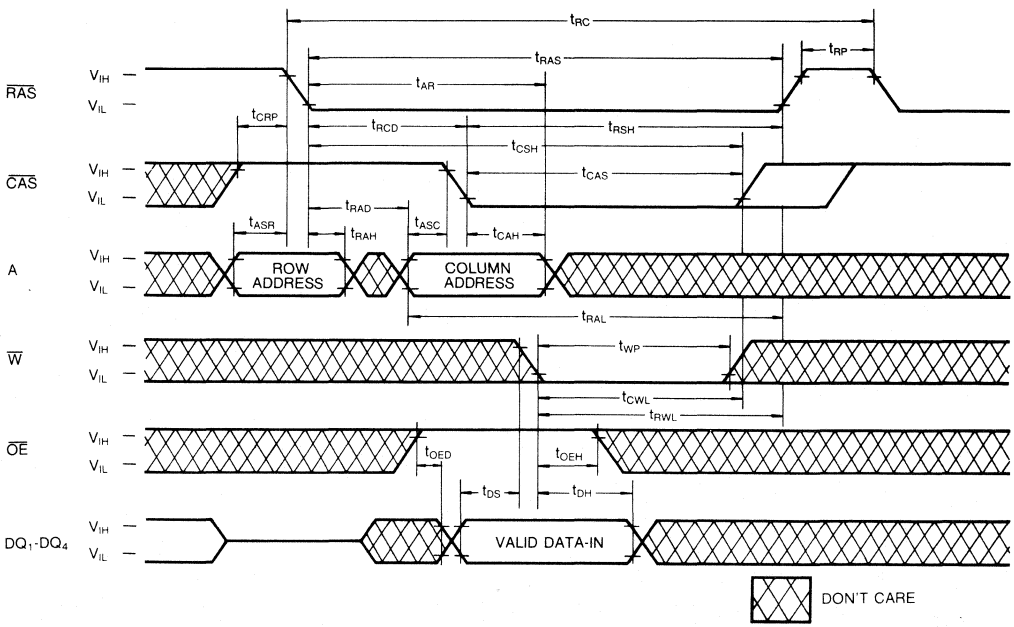


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)

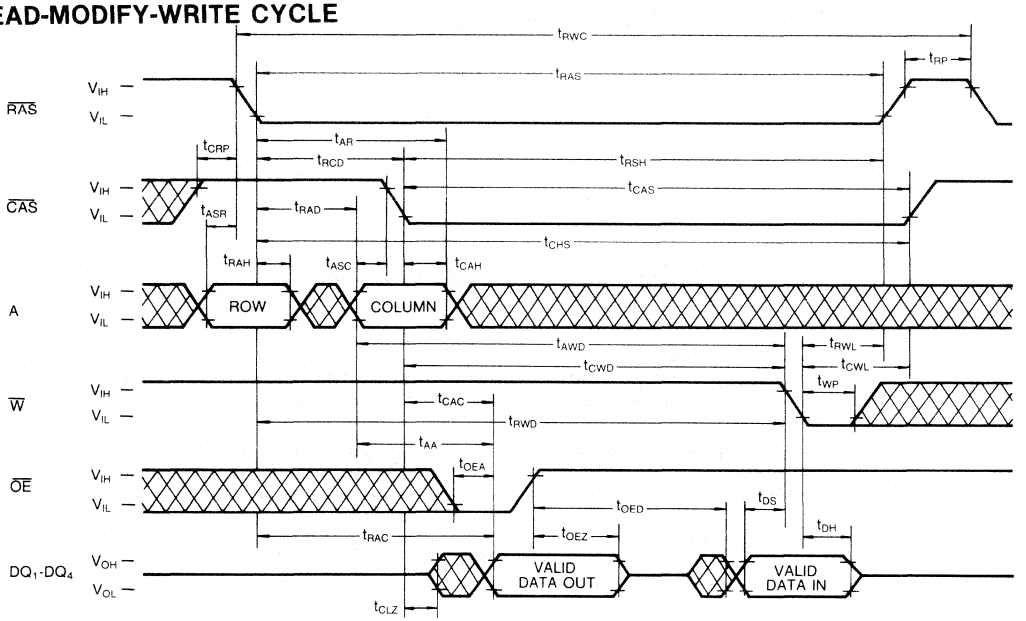


WRITE CYCLE (OE CONTROLLED WRITE)

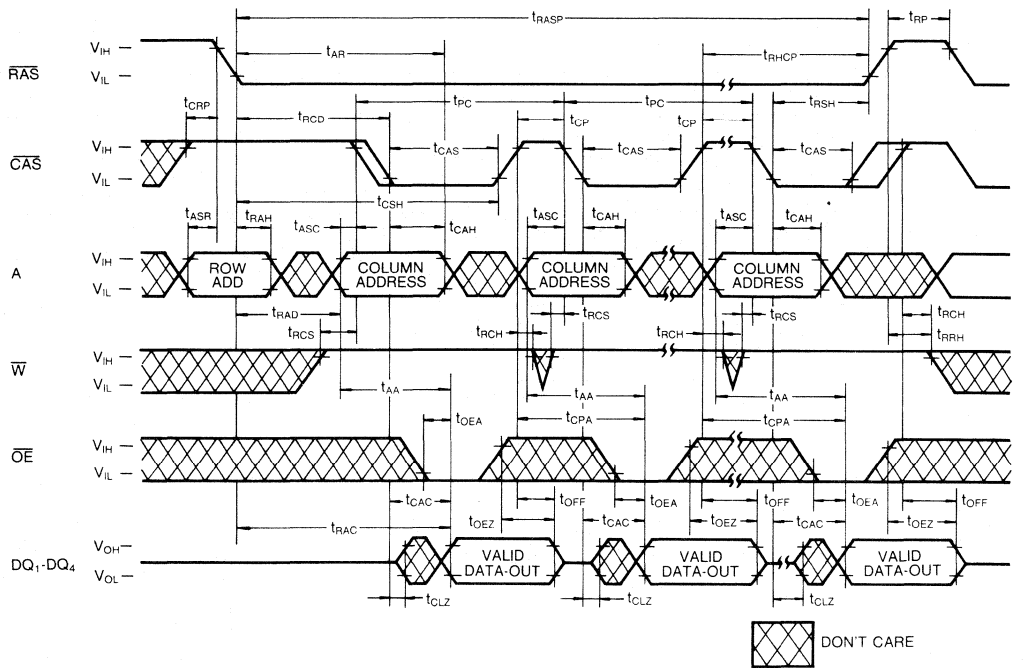


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE

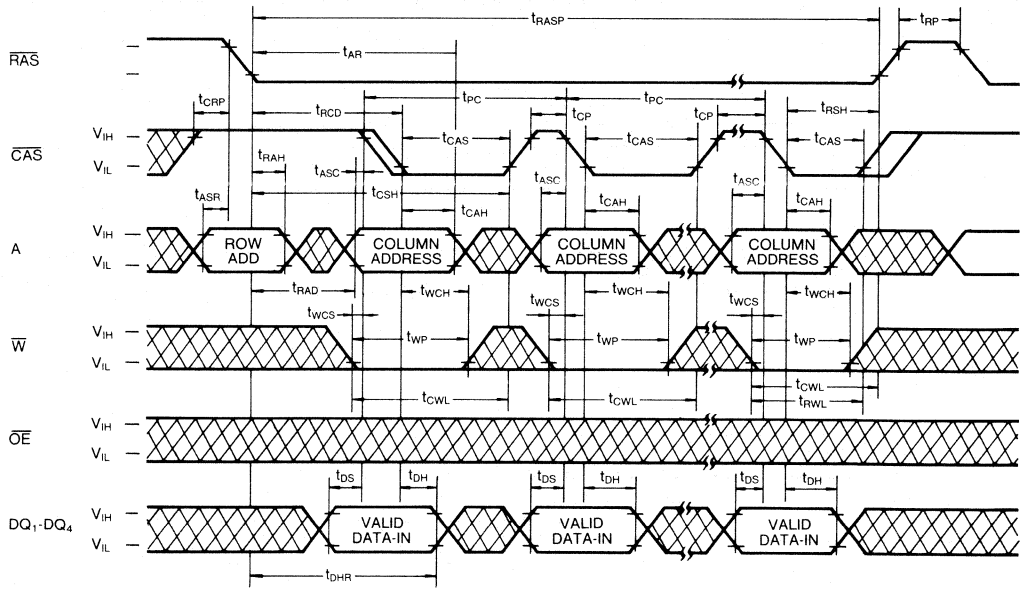


FAST PAGE MODE READ CYCLE

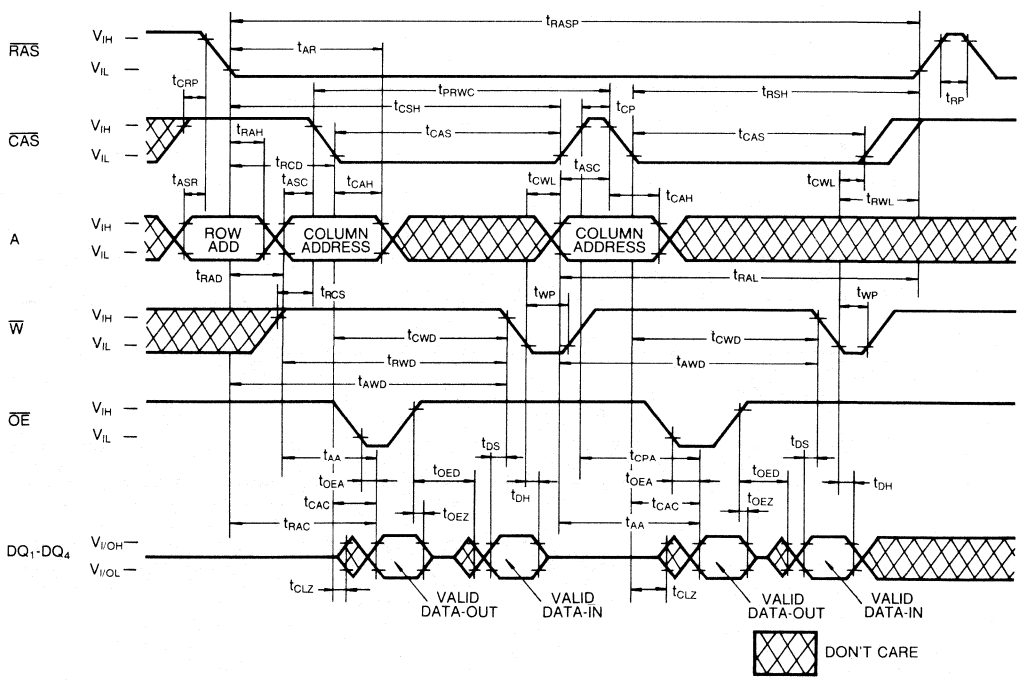


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



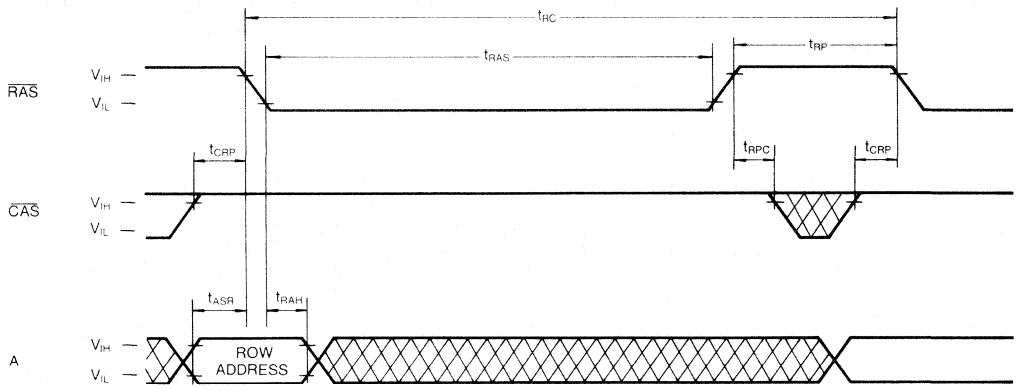
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

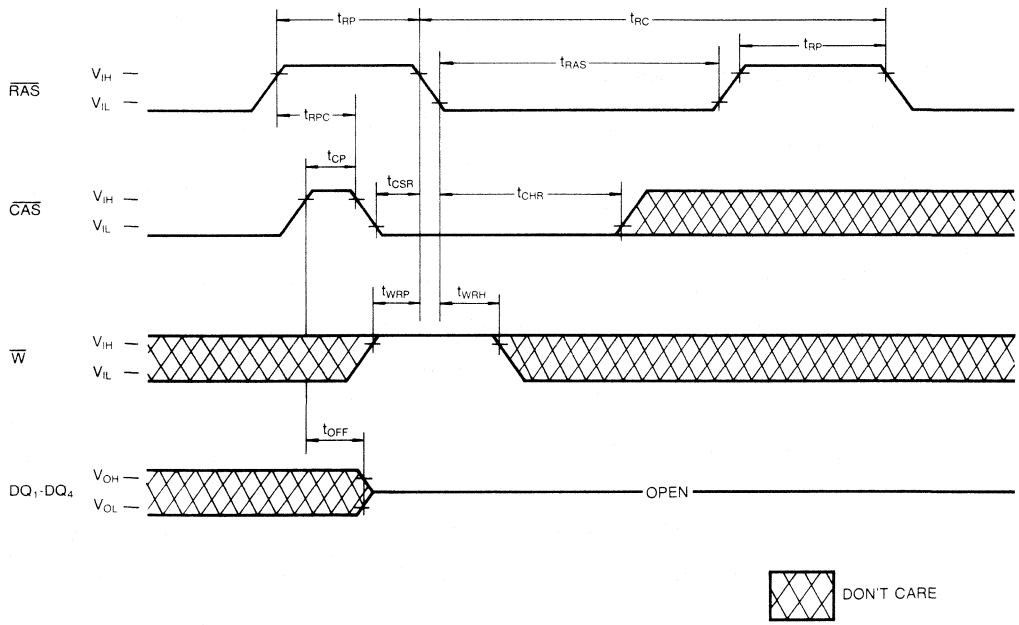
$\overline{RAS}$ ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



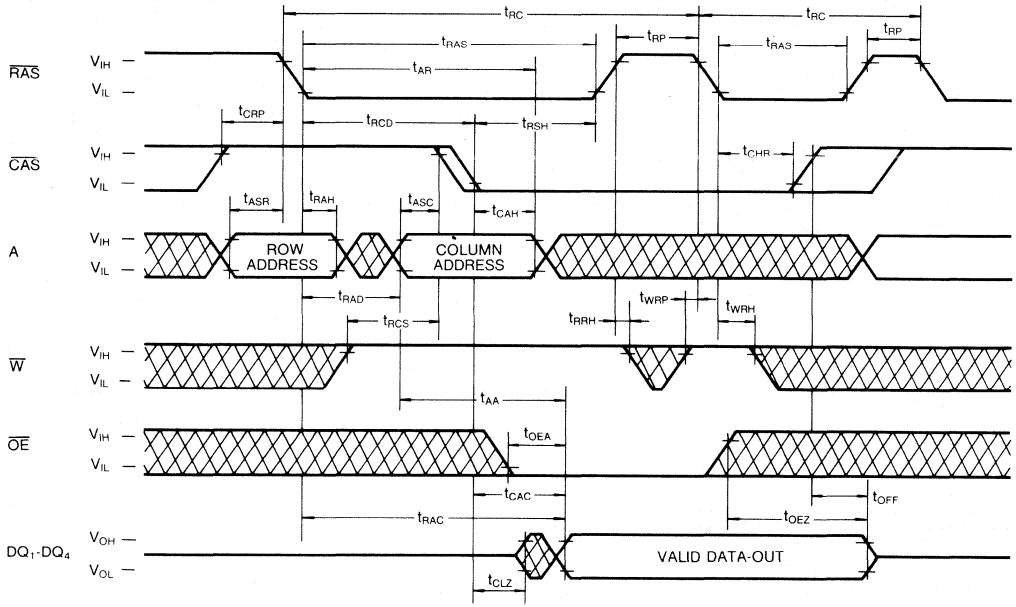
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: $\overline{OE}$, Address=Don't Care

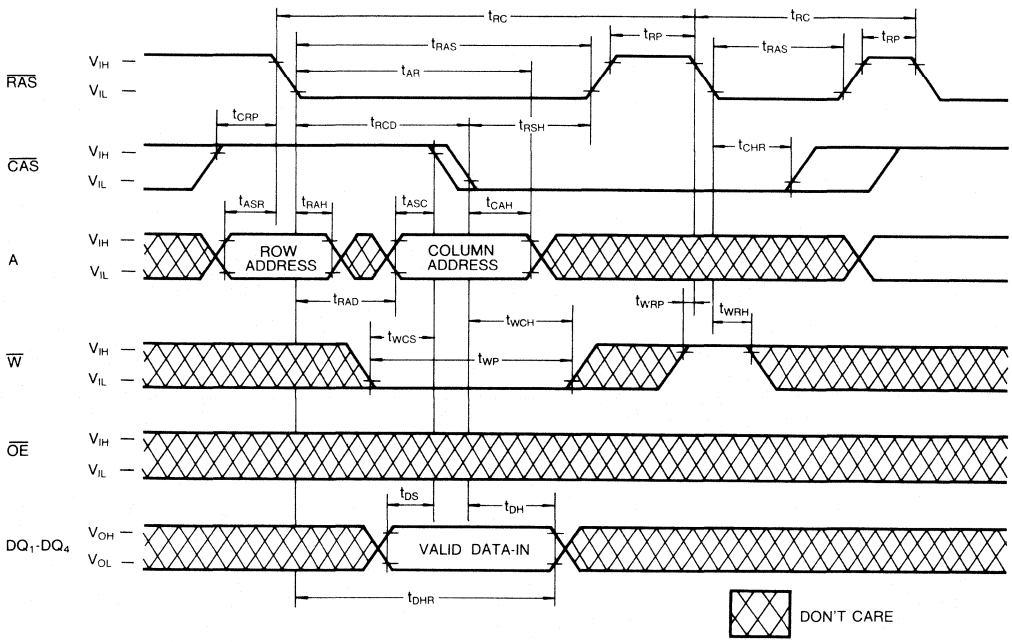


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

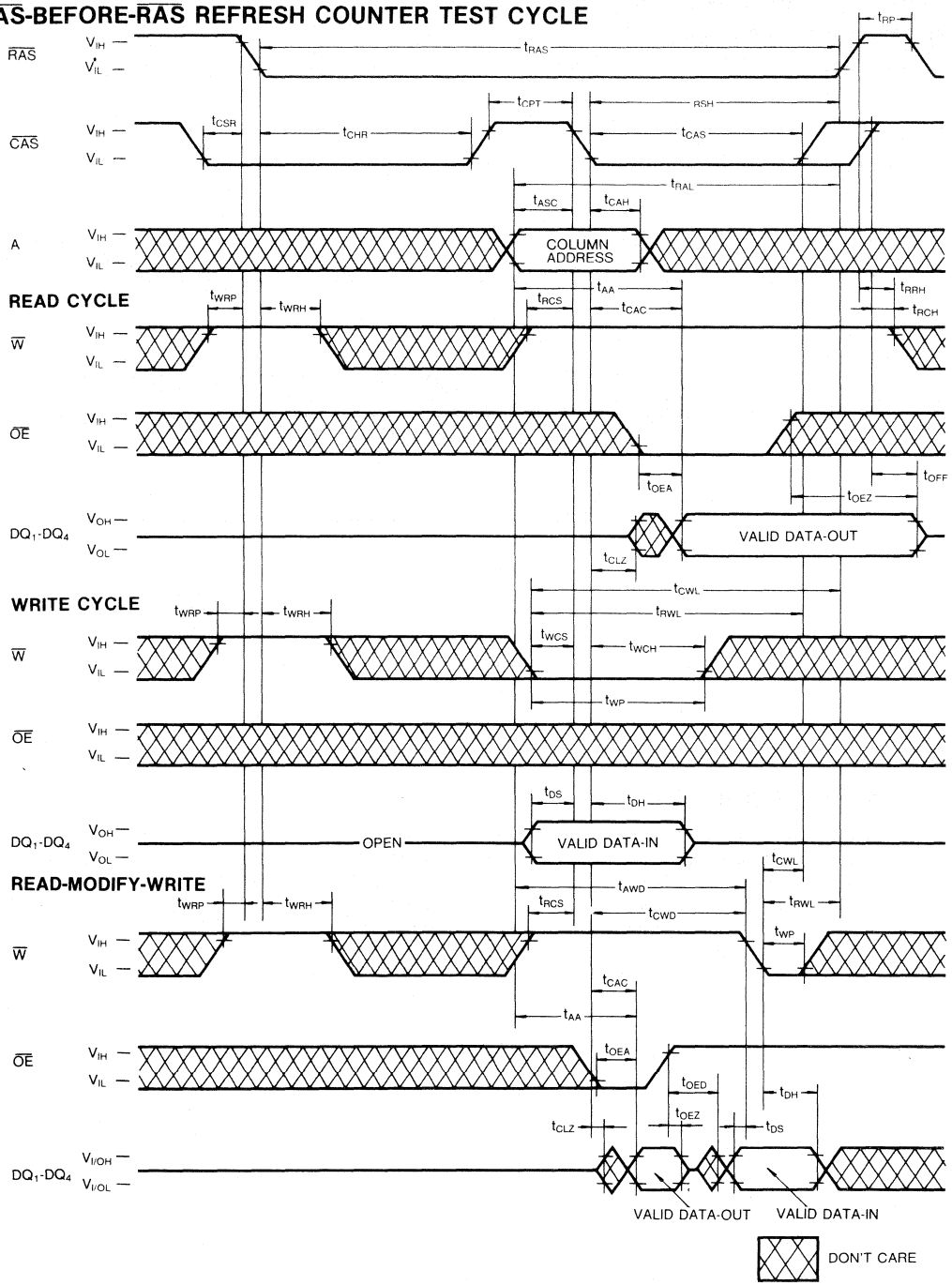


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

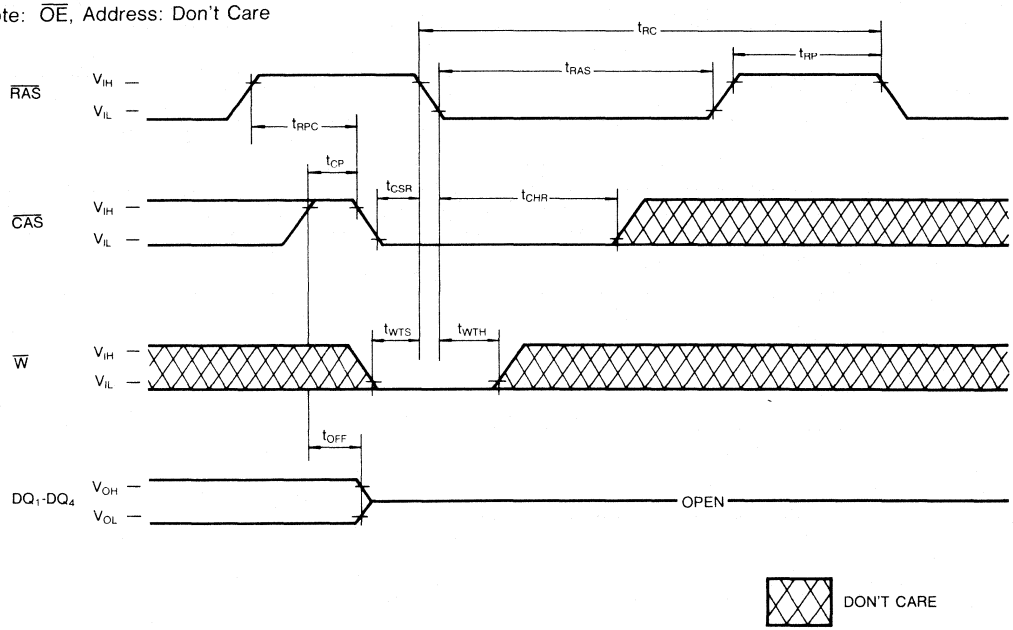
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



TEST MODE DESCRIPTION

The KM44C4000L is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0 and $A_1$are not used. If, upon reading, four bits on one D/Q pin are equal (all "1"s or "0"s) the D/Q pin indicates a "1". If they were not equal, the D/Q pin would indicate a "0". In "Test Mode", the 4M×4 DRAM can be tested as if it were a 1M×4 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE "or" "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

DEVICE OPERATIONS

Device Operation

The KM44C4000L contains 4,194,304 x 4 memory locations. Twenty-two address bits are required to address a particular 4-bit word in the memory array. Since the KM44C4000L has only 12 address input pins, time multiplexed addressing is used to input 12 row (A_0-A_{11}) and 10 column (A_0-A_9) addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM44C4000L begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins (A_0-A_9) is changed from a row address to a column address and is strobed in by $\overline{CAS}$. At that time, the status of the input pins (A_{10}-A_{11}) is don't care. This is the beginning of any KM44C4000L cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C4000L begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max). The KM44C4000L has common data I/O pins. The this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44C4000L can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing W low before $\overline{CAS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the three state regardless of the state of the OE input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing W low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44C4000L has a three-state output buffer which is controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever $\overline{CAS}$ and $\overline{OE}$ are high (V_{IH}), the outputs are in the high impedance state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C4000L operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, OE controlled write.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM44C4000L is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 256 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 4096 row address (A_0-A_{11}).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C4000L has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C4000L hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C4000L by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM44C4000L has Fast page mode capability. Fast page mode memory cycles provides faster access and lower power dissipation than normal memory cycles. In Fast page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while RAS is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 12 row address bits and 10 column address bits defined as follows:

Row Address — Bits A_0 through A_{11} are supplied by tthe on-chip refresh counter.

Column Address — Bits A_0 through A_{11} are strobed-in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 4096 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 4096 times so that highs are written into the 4096 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

DEVICE OPERATION (Continued)

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM44C4000L could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

An initial pause of 200 μsec is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. Eight initialization cycles are also required after any 256 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C4000L inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C4000L input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

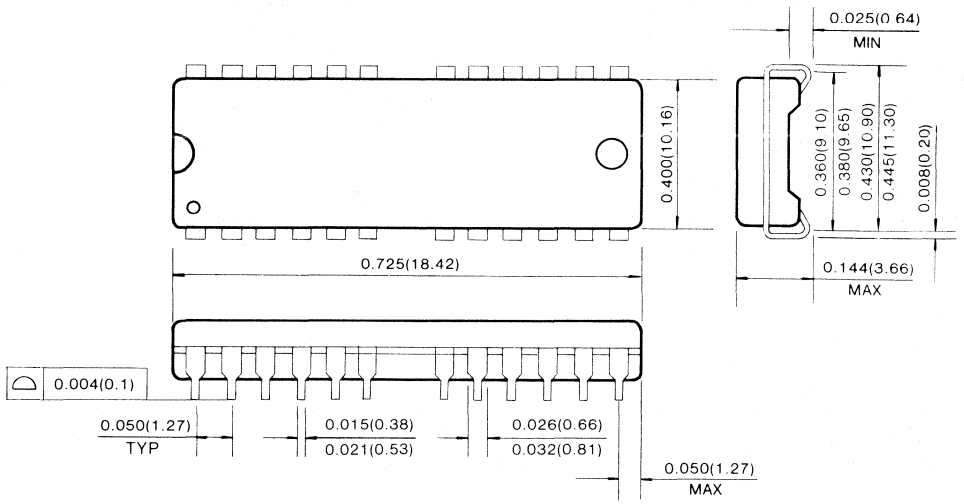
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM44C4000L using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C4000L and they supply much of the current used by the KM44C4000L during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

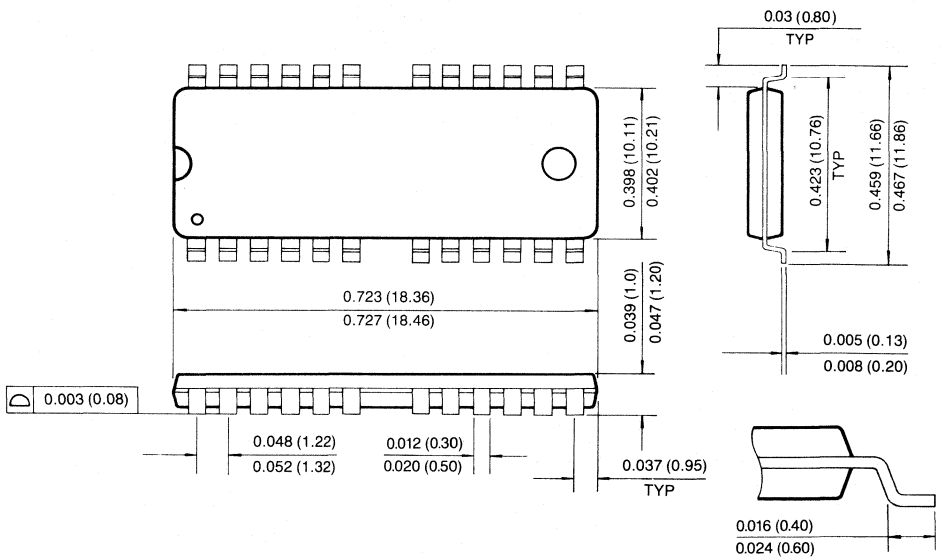
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (Forward and Reverse Type)



4M×4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C4100-6	60ns	15ns	110ns
KM44C4100-7	70ns	20ns	130ns
KM44C4100-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Double +5V±10% power supply**
- **2048 cycles/32ms refresh**
- **JEDEC standard pinout**
- **Available in plastic SOJ, TSOP (II) packages**

GENERAL DESCRIPTION

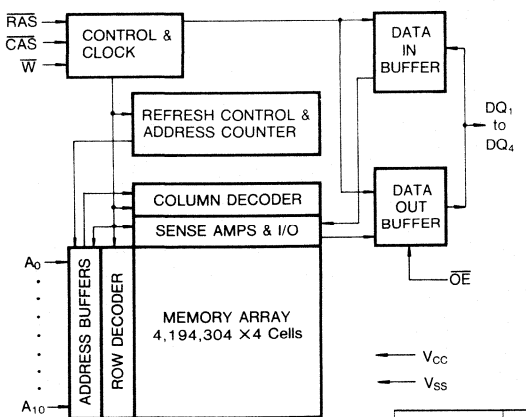
The Samsung KM44C4100 is a high speed CMOS 4,194,304×4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C4100 features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only Refresh. All inputs and outputs are fully TTL compatible.

The KM44C4100 is fabricated using Samsung's advanced CMOS process.

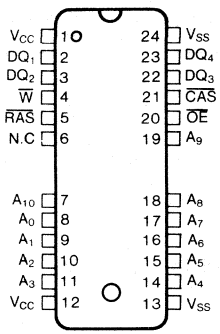
2

FUNCTIONAL BLOCK DIAGRAM



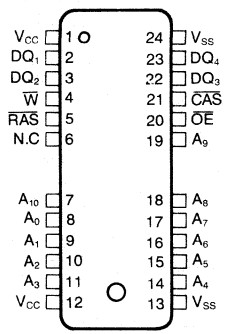
PIN CONFIGURATION (Top Views)

• KM44C4100J



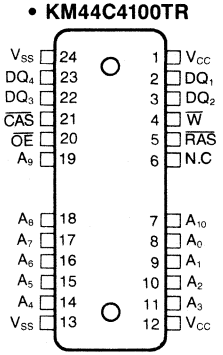
(SOJ)

• KM44C4100T



(TSOP(II)-Forward)

• KM44C4100TR



(TSOP (II)-Reverse)

Pin Name	Pin Function
A_0-A_{10}	Address Inputs
DQ_1-DQ_4	Data In/Data Out
$\overline{OE}$	Data out Enable
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min)	KM44C4100-6	I_{CC1}	—	110	mA
	KM44C4100-7		—	100	mA
	KM44C4100-8		—	90	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @ t_{RC}=min.)	KM44C4100-6	I_{CC3}	—	110	mA
	KM44C4100-7		—	100	mA
	KM44C4100-8		—	90	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @ t_{PC}=min.)	KM44C4100-6	I_{CC4}	—	90	mA
	KM44C4100-7		—	80	mA
	KM44C4100-8		—	70	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM44C4100-6	I_{CC6}	—	110	mA
	KM44C4100-7		—	100	mA
	KM44C4100-8		—	90	mA
Standby Current ($\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL}, D_{OUT} Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH}=−5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	—	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} address transition should be changed only once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address transition should be changed only once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{10})	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	KM44C4100-6		KM44C4100-7		KM44C4100-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

Parameter	Symbol	KM44C4100-6		KM44C4100-7		KM44C4100-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (2,048 cycles)	t_{REF}		32		32		32	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	85		100		105		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	15		20		20		ns	
Write command set-up time (test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ cycle)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ cycle)	t_{WRH}	10		10		10		ns	

TEST MODE CYCLE

(Note. 12)

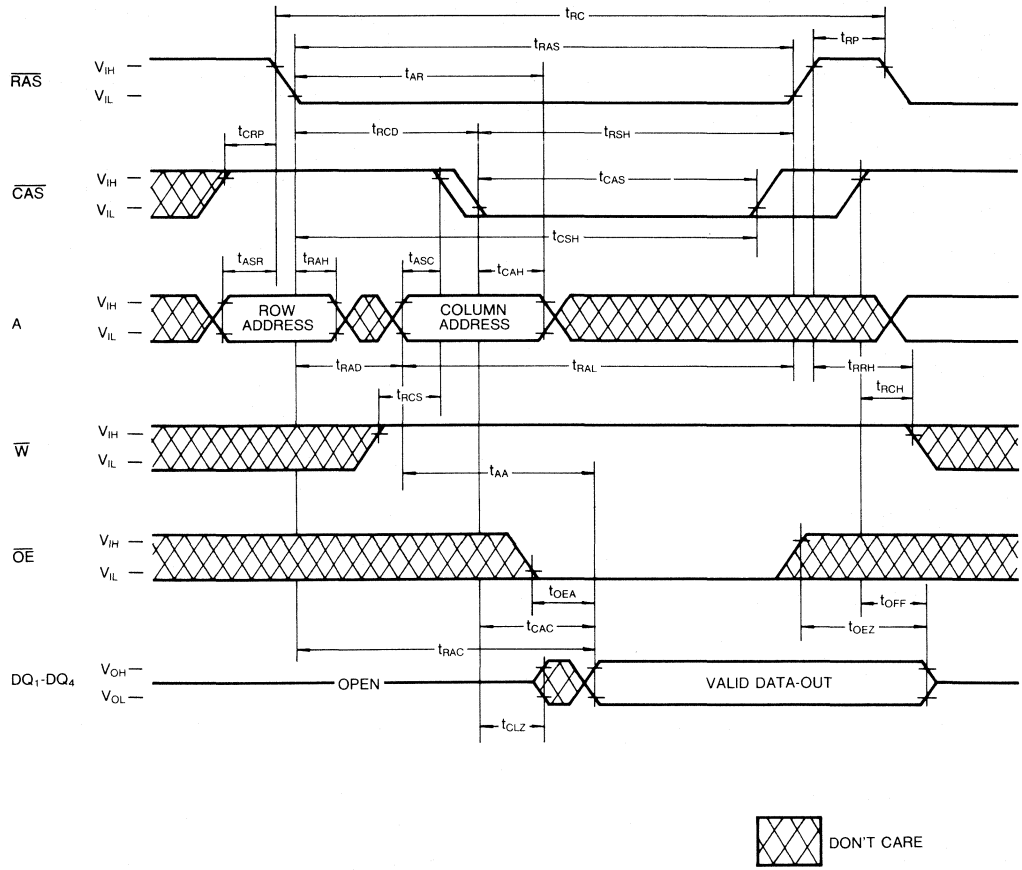
Parameter	Symbol	KM44C4100-6		KM44C4100-7		KM44C4100-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	160		190		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		45		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	45		55		55		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	90		105		115		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	60		70		75		ns	8
Fast mode cycle time	t_{PC}	45		50		55		ns	
Fast page mode read-modefy-write	t_{PRWC}	90		105		110		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3
$\overline{OE}$ access time	t_{OEA}		20		25		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		25		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only Refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF(max)}$ and $t_{OEZ(max)}$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

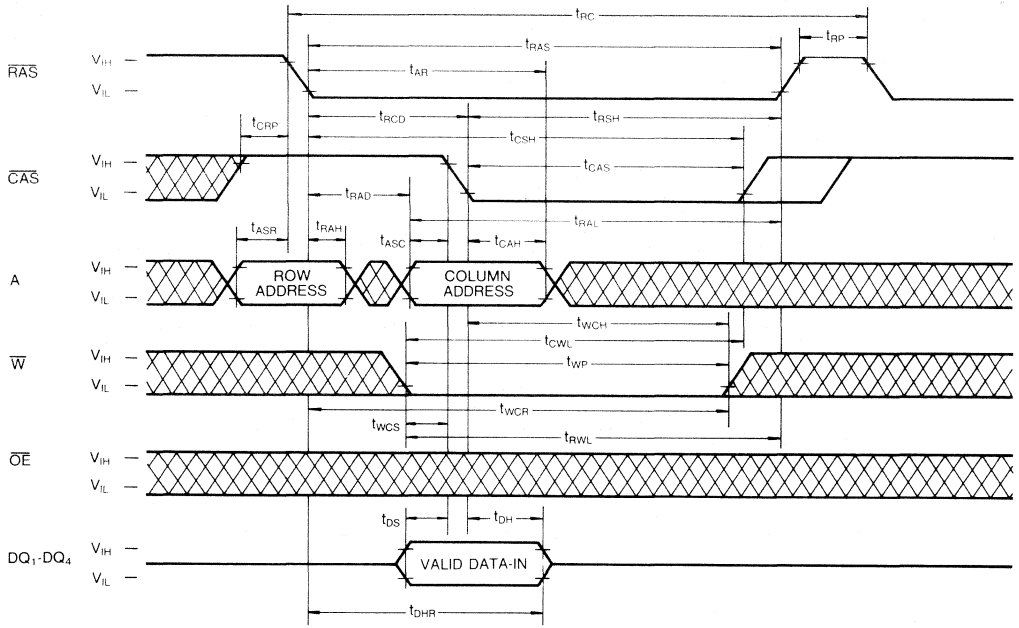
TIMING DIAGRAMS

READ CYCLE

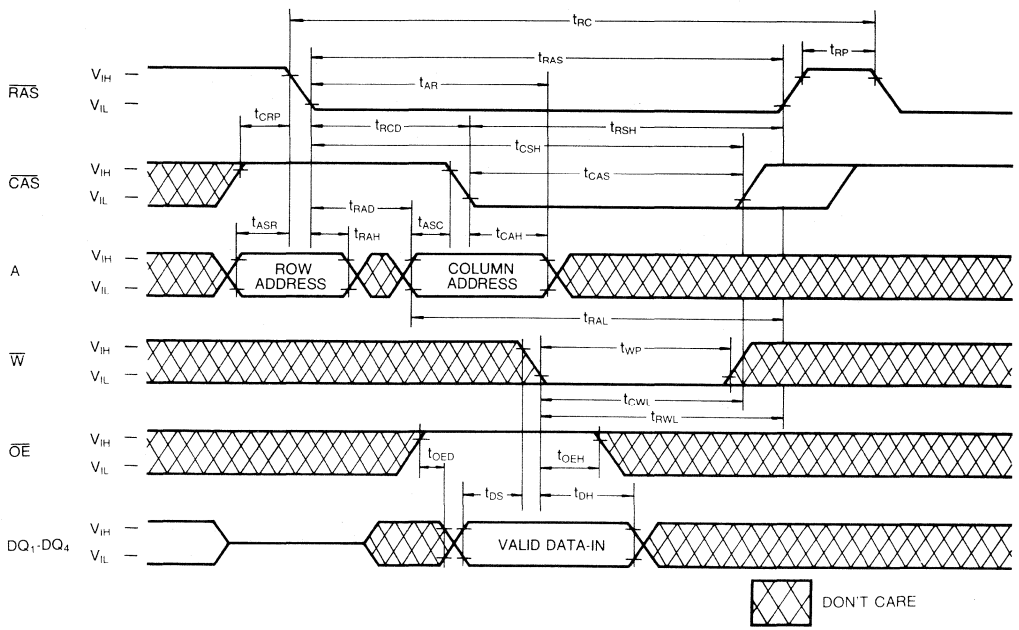


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)

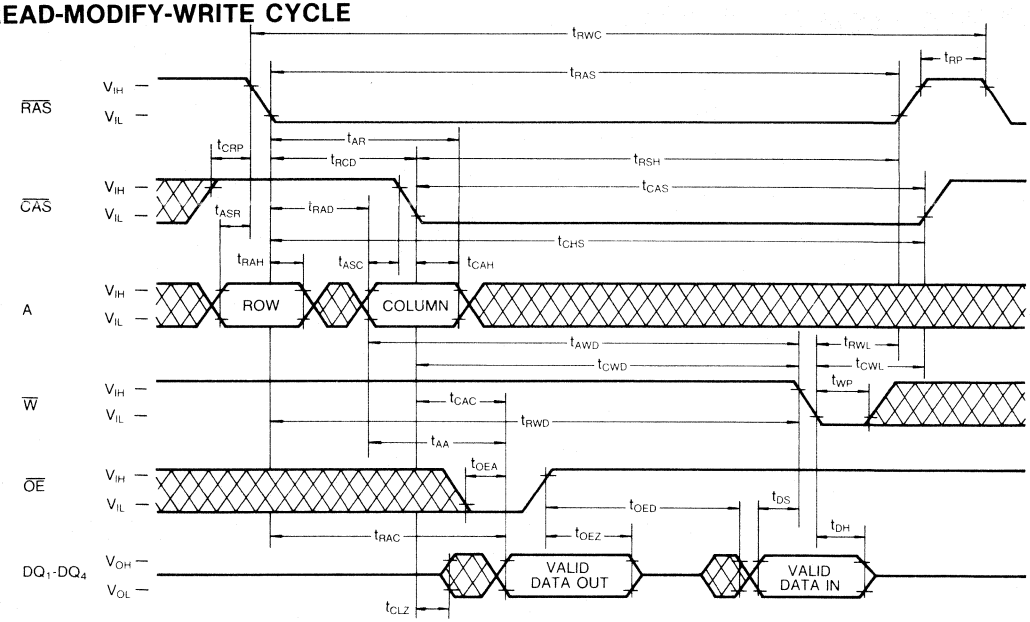


WRITE CYCLE (OE CONTROLLED WRITE)

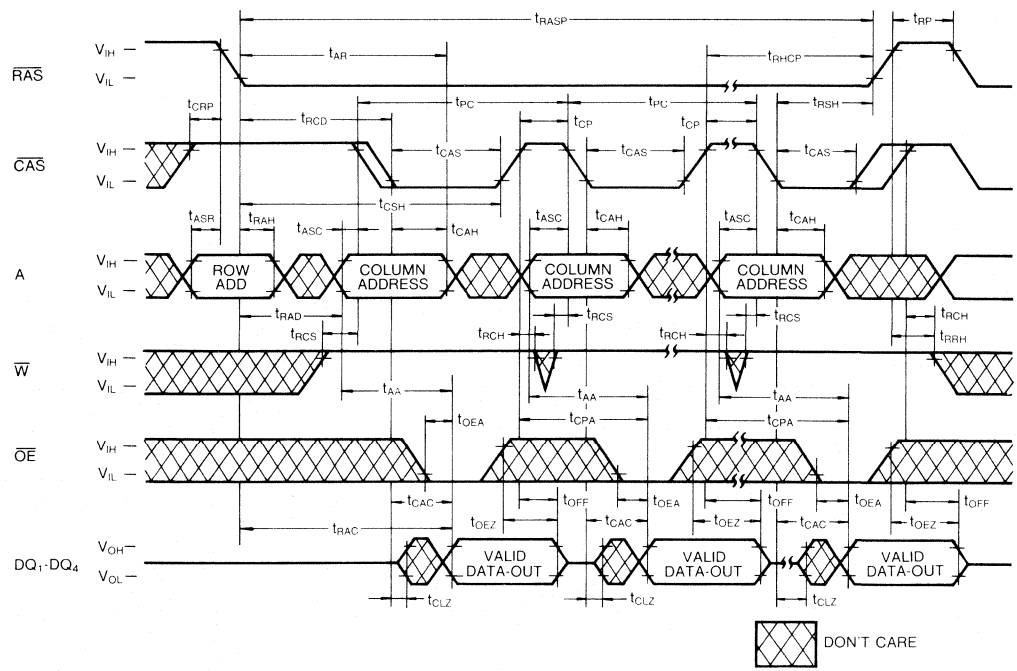


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE

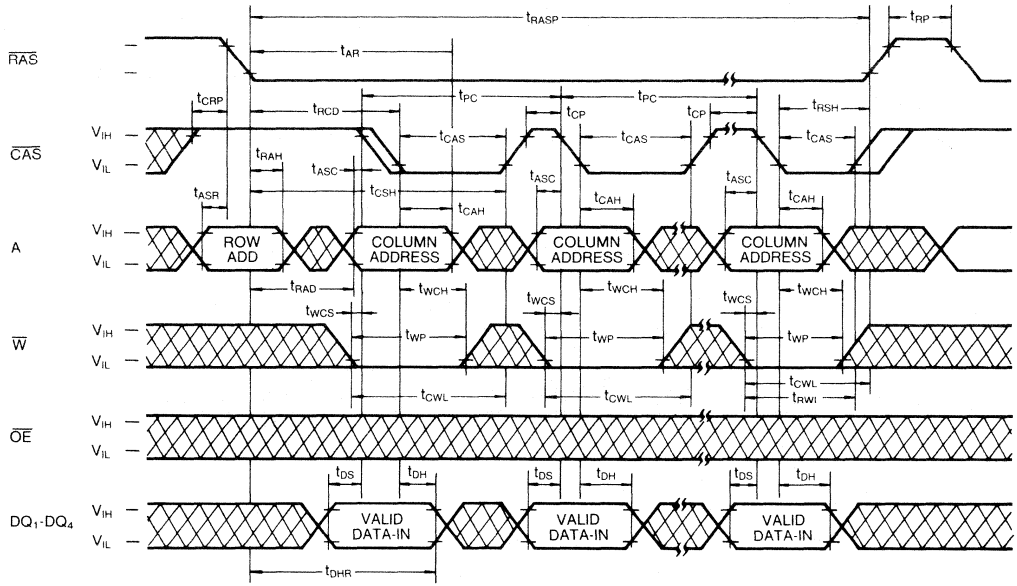


FAST PAGE MODE READ CYCLE

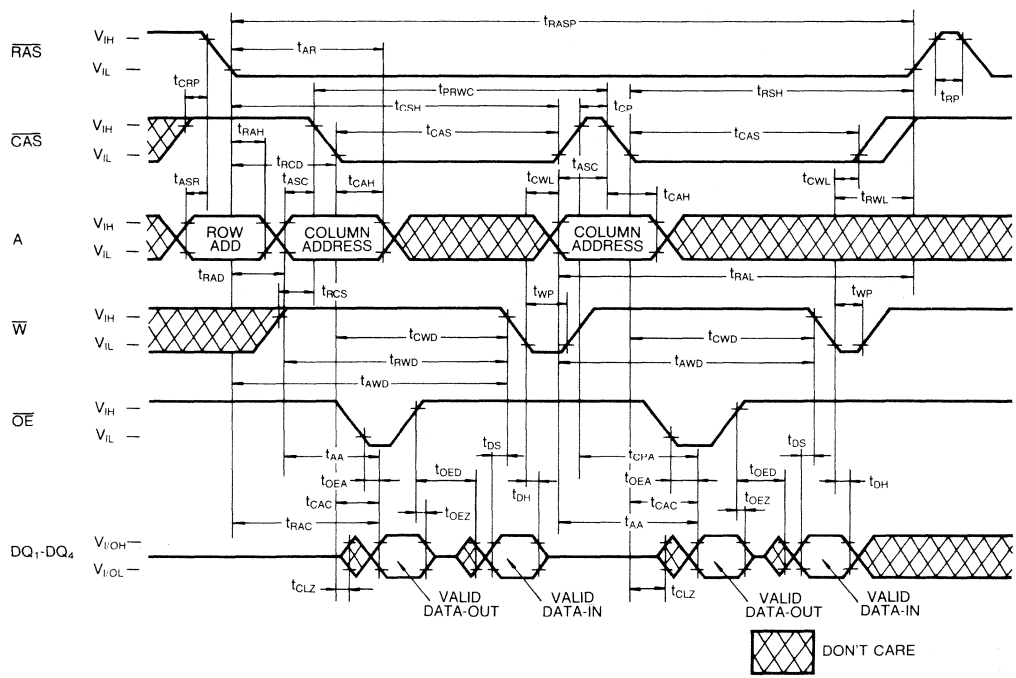


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



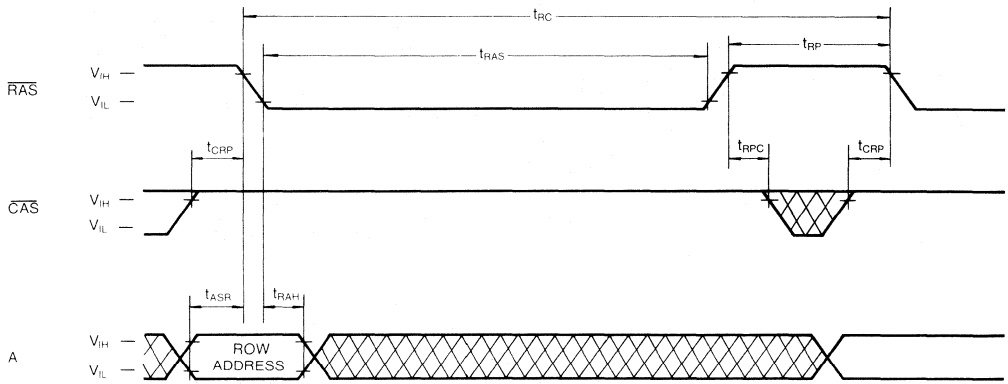
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

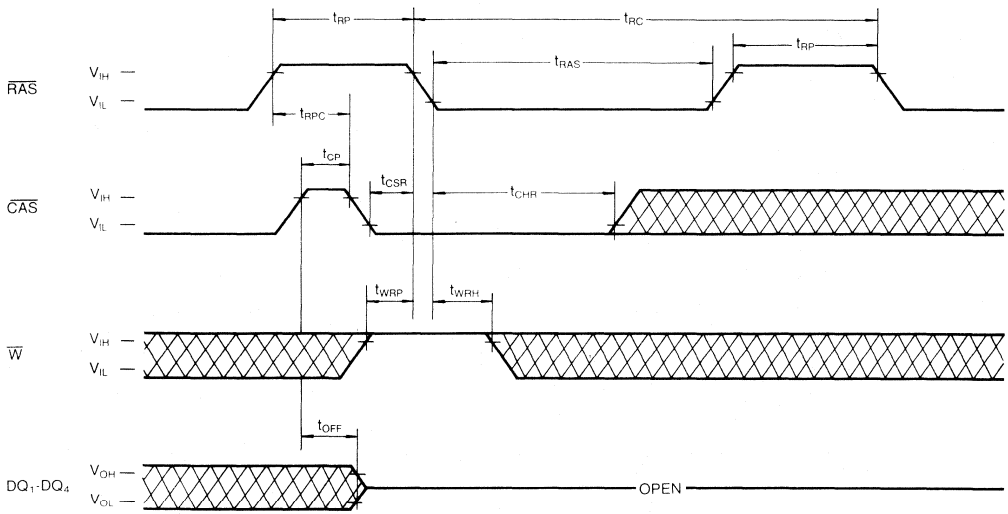
$\overline{RAS}$ ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



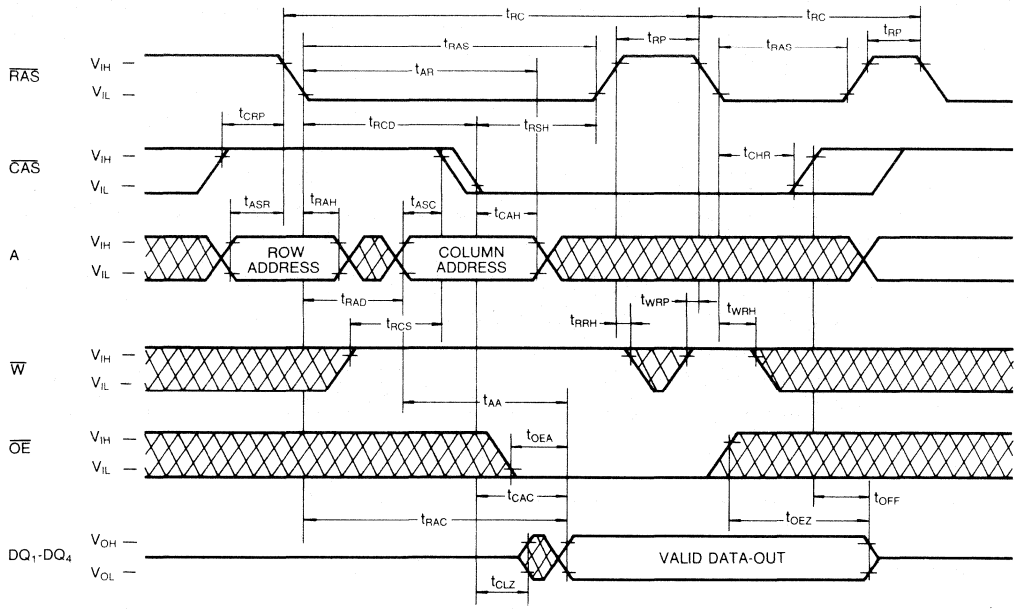
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: $\overline{OE}$, Address=Don't Care

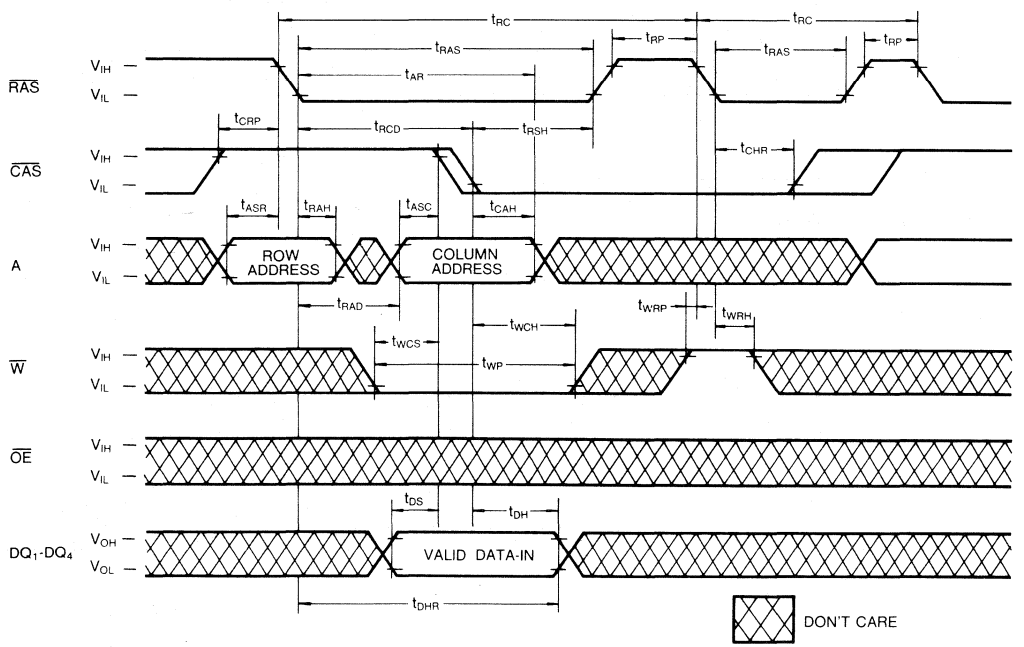


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

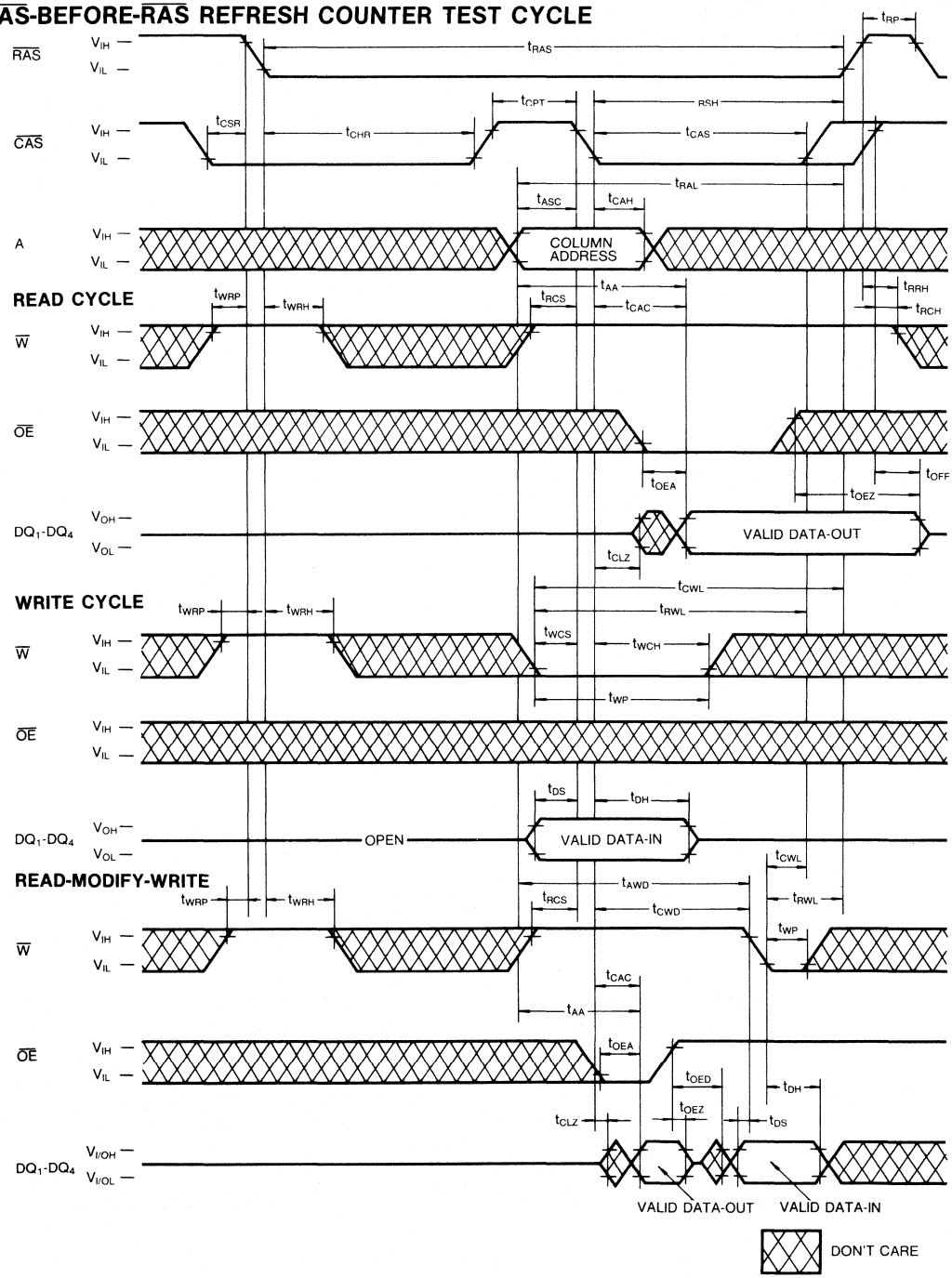


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

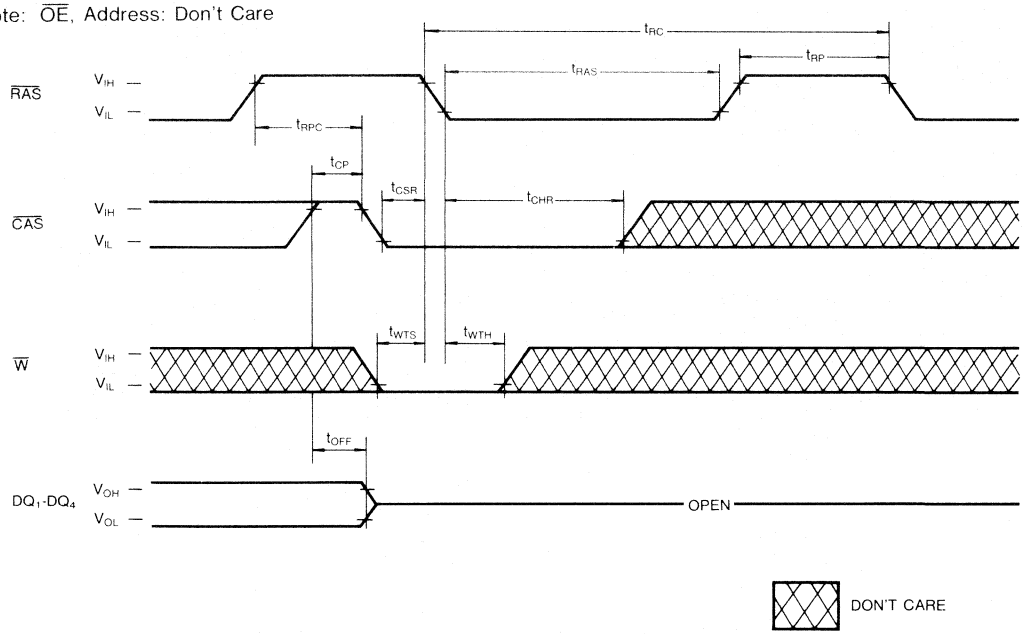
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



TEST MODE DESCRIPTION

The KM44C4100 is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0 and A_1 are not used. If, upon reading, four bits on one D/Q pin are equal (all "1"s or "0"s) the D/Q pin indicates a "1". If they were not equal, the D/Q pin would indicate a "0". In "Test Mode", the 4M×4 DRAM can be tested as if it were a 1M×4 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE "or" "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

DEVICE OPERATIONS

The KM44C4100 contains 4,194,304×4 memory locations. Twenty two address bit are required to address a particular 4-bit word in the memory array. Since the KM44C4100 has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM44C4100 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is trobed in by $\overline{CAS}$. This is the beginning of any KM44C4100 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C4100 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAC}(max), then the access time to valid data is specified by r_{RAC}(min). However, If $\overline{CAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max). The KM44C4100 has common data I/O pins.

The this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44C4100 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$ and $\overline{CAS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the three state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44C4100 has a three-state output buffer which is controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever $\overline{CAS}$ and $\overline{OE}$ are high (V_{IH}), the outputs are in the high impedance state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C4100 operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z output state: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} are not met)

Refresh

The data in the KM44C4100 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 32ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 2048 row address (A_0-A_{10}).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C4100 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuity is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C4100 hidden refresh cycle is actually a $\overline{CAS}$ before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C4100 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. These are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows:

Row Address—Bits A_0 through A_{10} are supplied by the on-chip refresh counter.

Column Address—Bits A_0 through A_{10} are strobedin by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-Before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 2048 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 2048 times so that highs are written into the 2048 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

If $\overline{RAS}$-V_{SS} during power-up, the KM44C4100 could possibly begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

DEVICE OPERATION (Continued)

An initial pause of 200 usec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 32 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C4100 inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C4100 input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

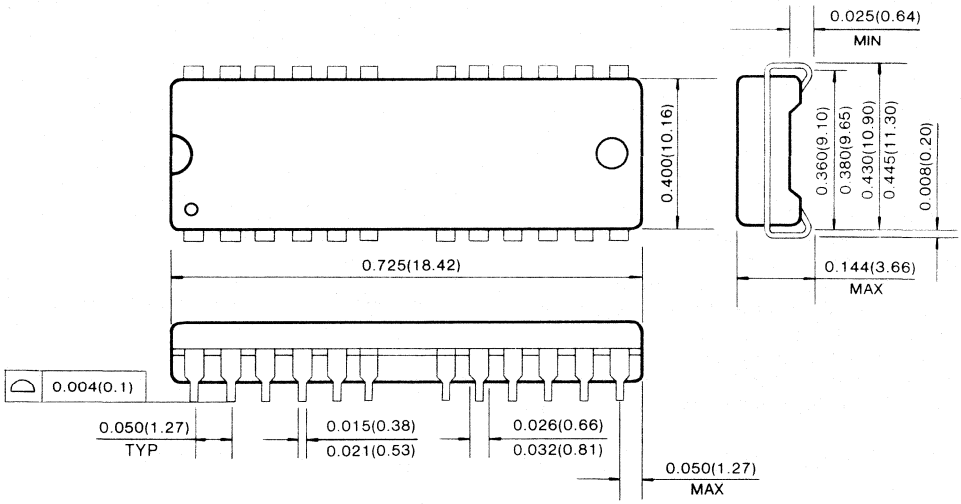
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM44C4100 using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C4100 and they supply much of the current used by the KM44C4100 during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1uF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

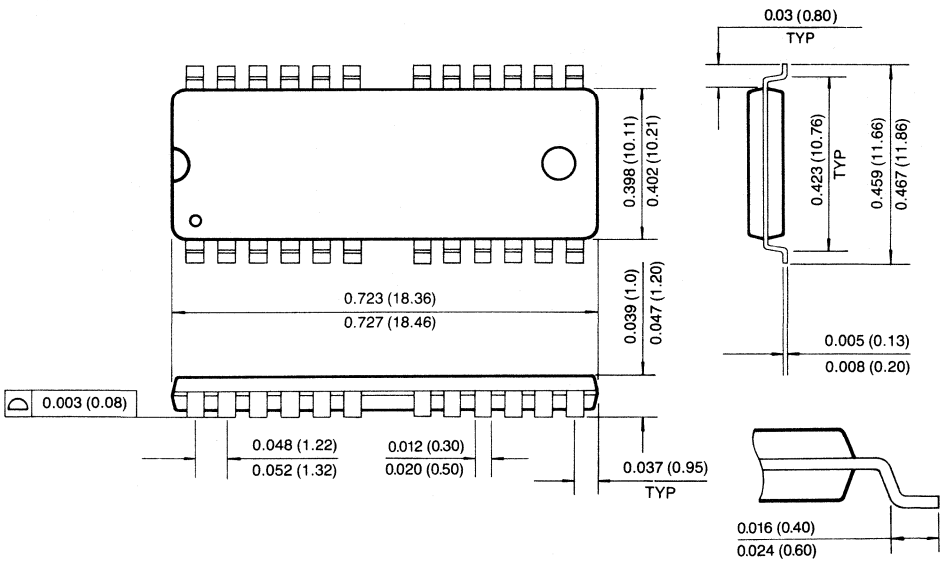
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (Forward and Reverse Type)



4M×4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM44C4100L-6	60ns	15ns	110ns
KM44C4100L-7	70ns	20ns	130ns
KM44C4100L-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Double +5V±10% power supply**
- **2048 cycles/ 256ms refresh**
- **JEDEC standard pinout**
- **Available in plastic SOJ, TSOP (II) packages**

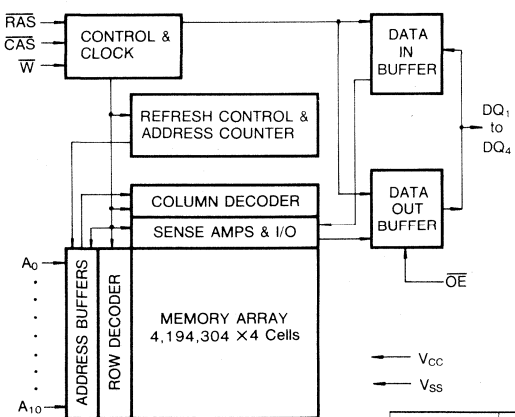
GENERAL DESCRIPTION

The Samsung KM44C4100L is a CMOS high speed 4,194,304 × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C4100L features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

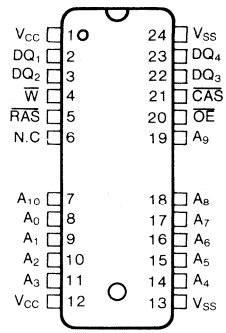
The KM44C4100L is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



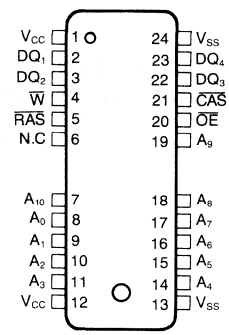
PIN CONFIGURATION (Top Views)

• KM44C4100LJ



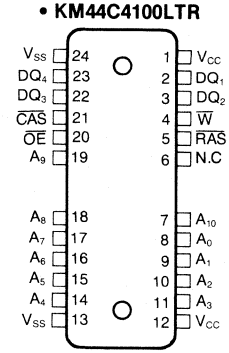
(SOJ)

• KM44C4100LT



(TSOP(II)-Forward)

• KM44C4100LTR



(TSOP (II)-Reverse)

Pin Name	Pin Function
A_0-A_{10}	Address Inputs
DQ_1-DQ_4	Data In/Data Out
$\overline{OE}$	Data out Enable
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC} = min.)	KM44C4100L-6	I_{CC1}	—	110	mA
	KM44C4100L-7		—	100	mA
	KM44C4100L-8		—	90	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM44C4100L-6	I_{CC3}	—	110	mA
	KM44C4100L-7		—	100	mA
	KM44C4100L-8		—	90	mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling @t_{PC} = min.)	KM44C4100L-6	I_{CC4}	—	90	mA
	KM44C4100L-7		—	80	mA
	KM44C4100L-8		—	70	mA
Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		I_{CC5}	—	300	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min.)	KM44C4100L-6	I_{CC6}	—	110	mA
	KM44C4100L-7		—	100	mA
	KM44C4100L-8		—	90	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V_{IH}) = V_{CC}-0.2V Input Low Voltage (V_{IL}) = 0.2V $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V DQ_{1-4} = Don't Care T_{RC} = 125 μs, T_{RAS} = t_{RAS} min. ~ 1μs		I_{CC7}	—	500	μA
Standby Current ($\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{OUT} Enable)		I_{CC8}	—	5	mA
Input Leakage Current (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$ = V_{IL}. In I_{CC4}, Address can be changed maximum once while $\overline{CAS}$ = V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{10})	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	KM44C4100L-6		KM44C4100L-7		KM44C4100L-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10

AC CHARACTERISTICS (Continued)

Parameter	Symbol	KM44C4100L-6		KM44C4100L-7		KM44C4100L-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (2,048 cycles)	t_{REF}		256		256		256	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	85		100		105		ns	
$\overline{RAS}$ pulse width (Fast Page Mode)	t_{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{OE}$ access time	t_{OEA}		15		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	15		20		20		ns	
Write command set-up time (test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ cycle)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ cycle)	t_{WRH}	10		10		10		ns	

TEST MODE CYCLE

(Note. 12)

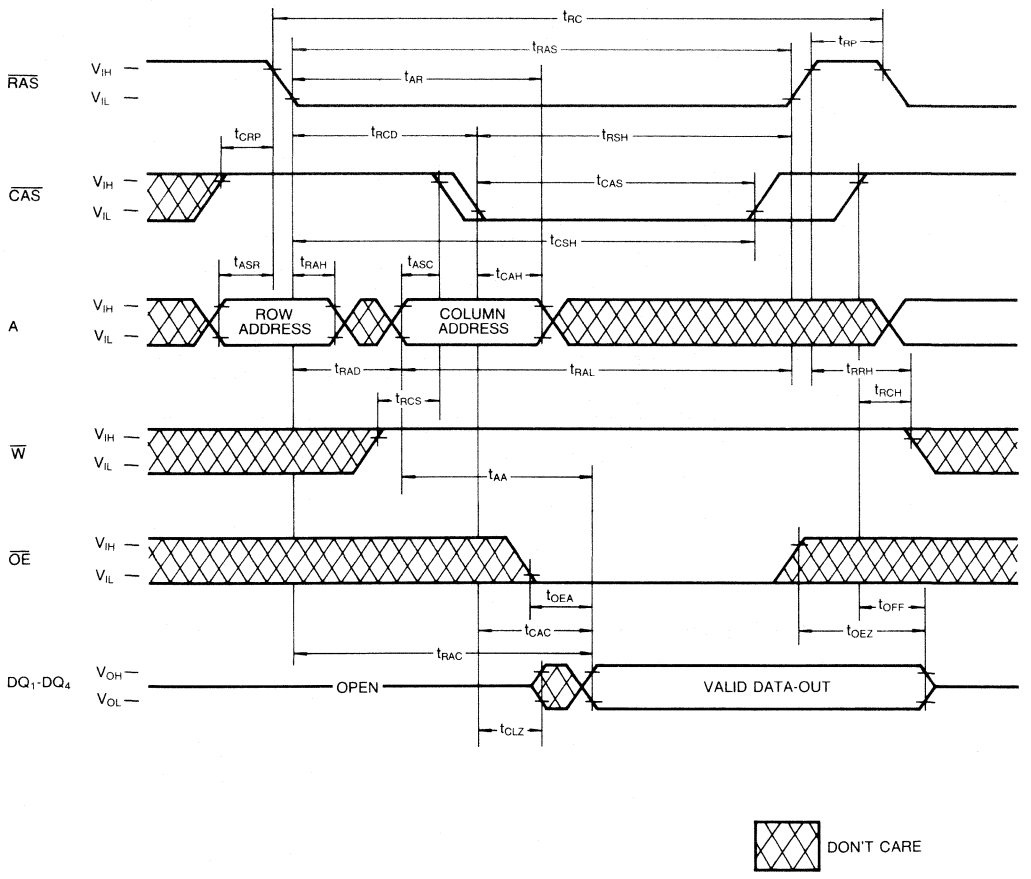
Parameter	Symbol	KM44C4100L-6		KM44C4100L-7		KM44C4100L-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	160		190		210		ns	
Access time from $\overline{RAS}$	t_{RAC}		65		75		85	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	65	10,000	75	10,000	85	10,000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		45		ns	
$\overline{CAS}$ to write enable delay	t_{CWD}	45		55		55		ns	8
$\overline{RAS}$ to write enable delay	t_{RWD}	90		105		115		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	60		70		75		ns	8
Fast mode cycle time	t_{PC}	45		50		55		ns	
Fast page mode read-modefy-write	t_{PRWC}	90		105		110		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	3
$\overline{OE}$ access time	t_{OEA}		20		25		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		25		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only Refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF(max)}$ and $t_{OEZ(max)}$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

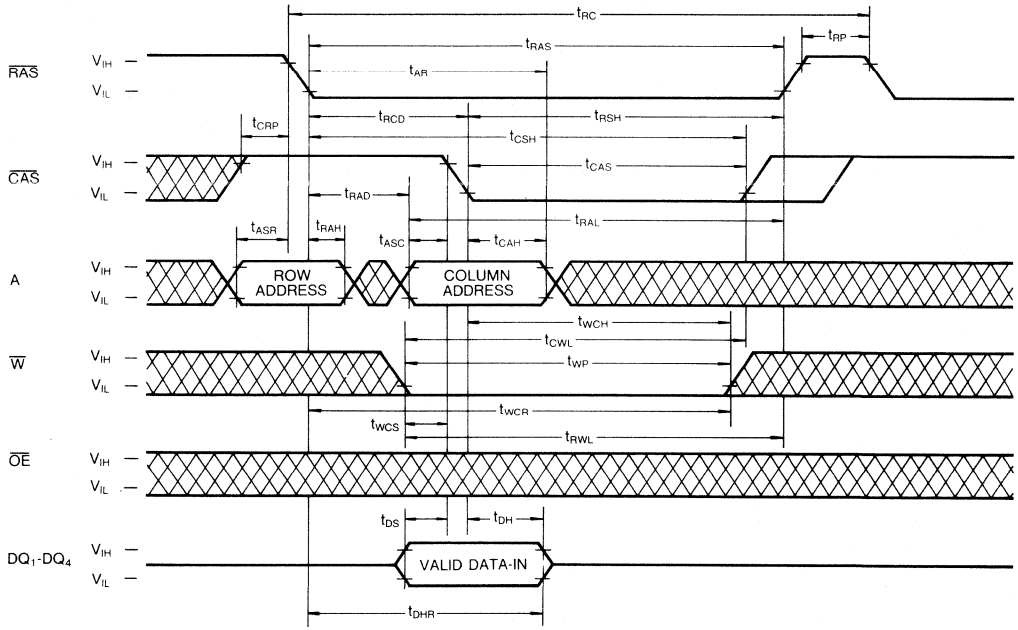
TIMING DIAGRAMS

READ CYCLE

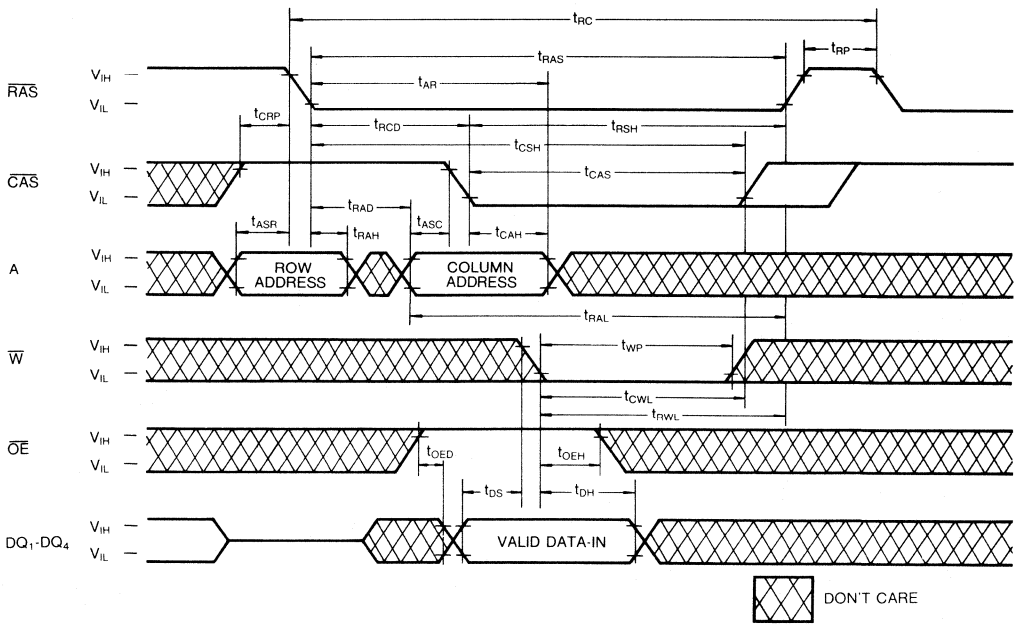


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)

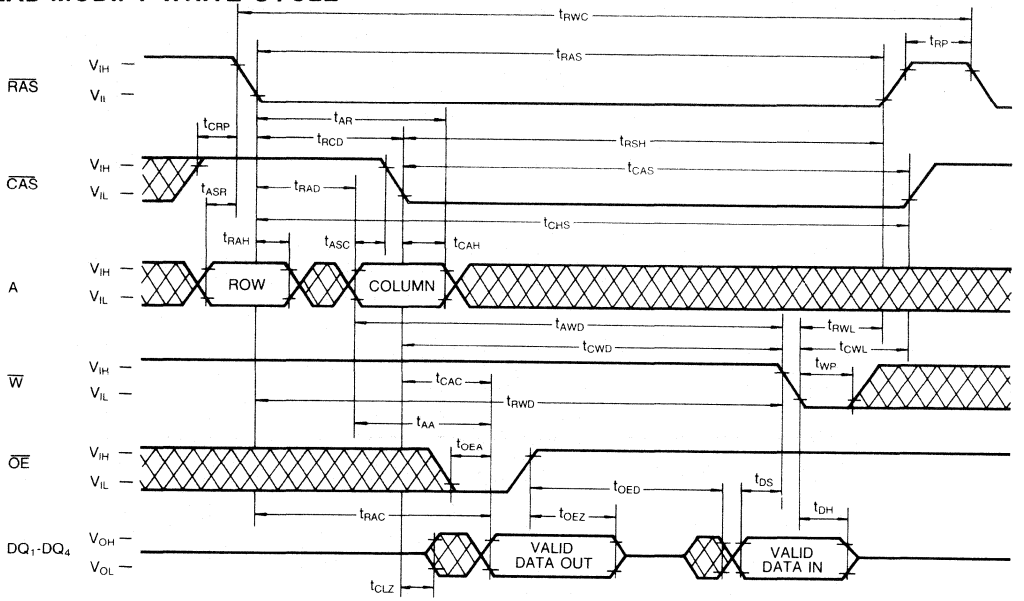


WRITE CYCLE (OE CONTROLLED WRITE)

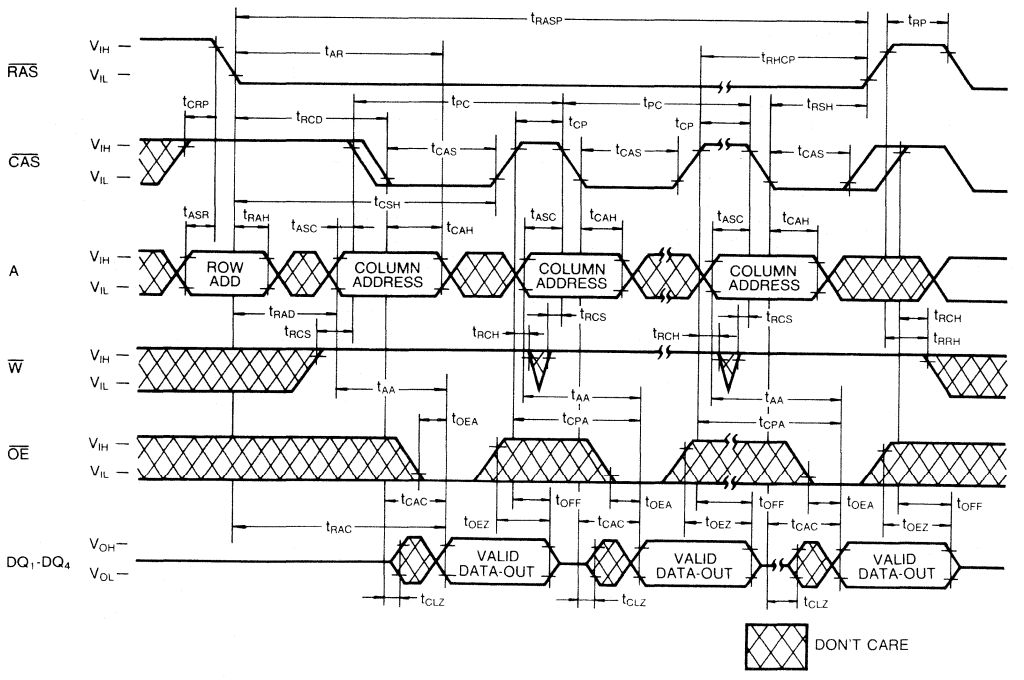


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE

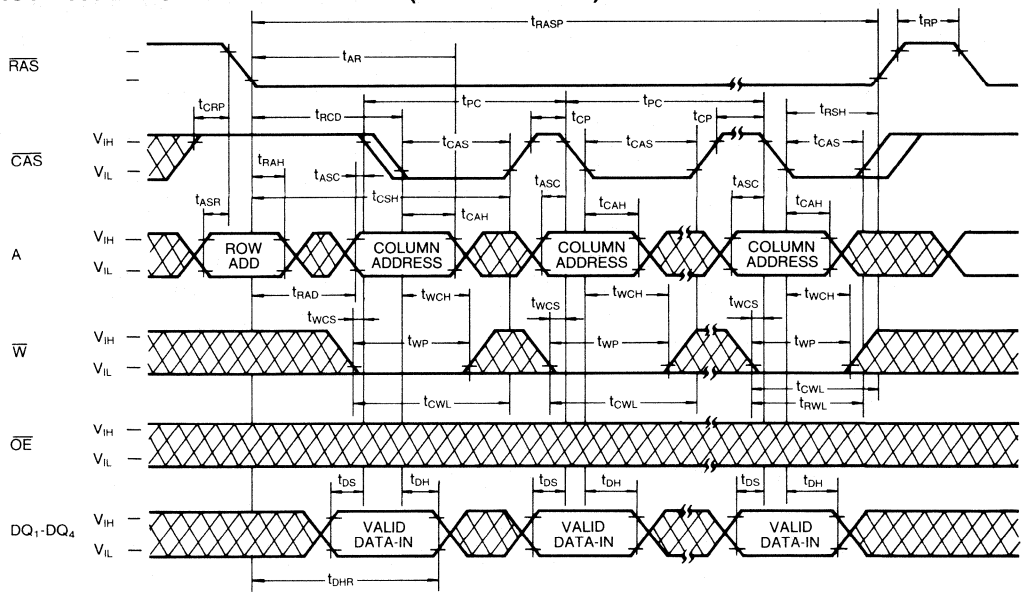


FAST PAGE MODE READ CYCLE

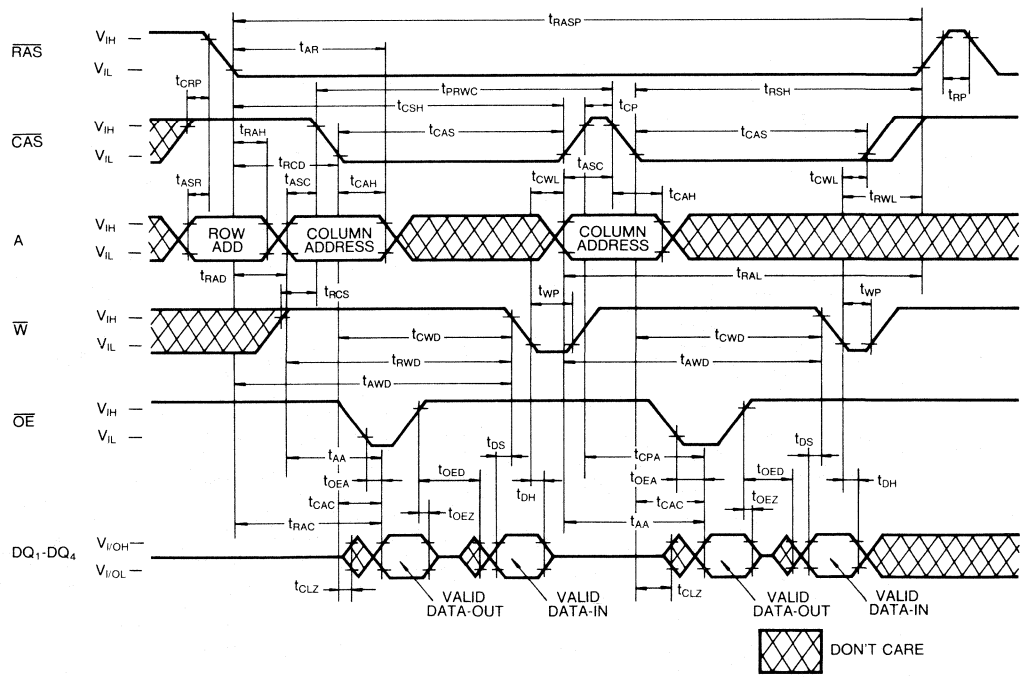


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



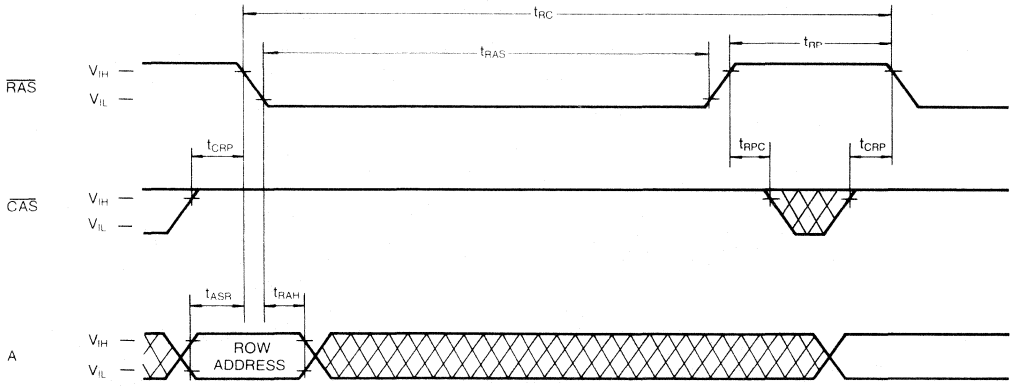
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

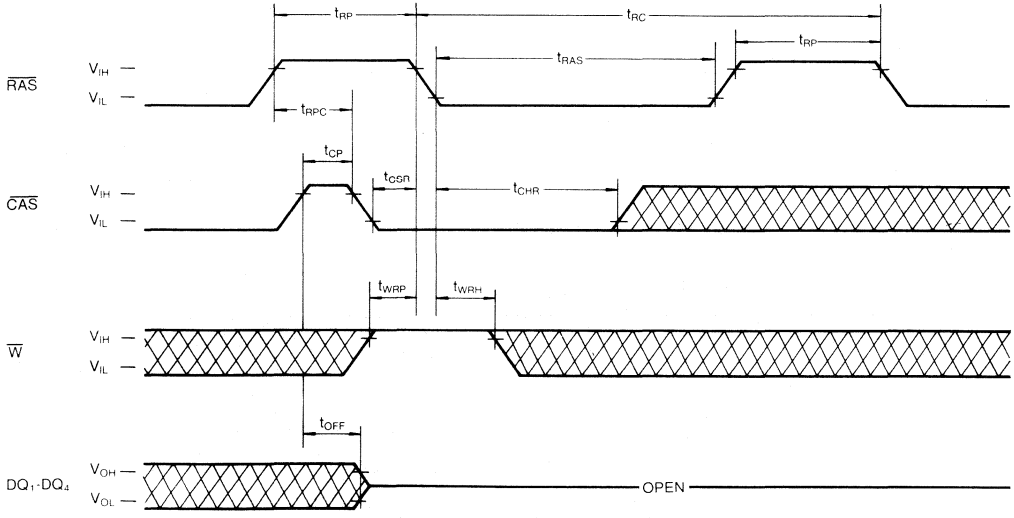
$\overline{RAS}$ ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$=Don't Care



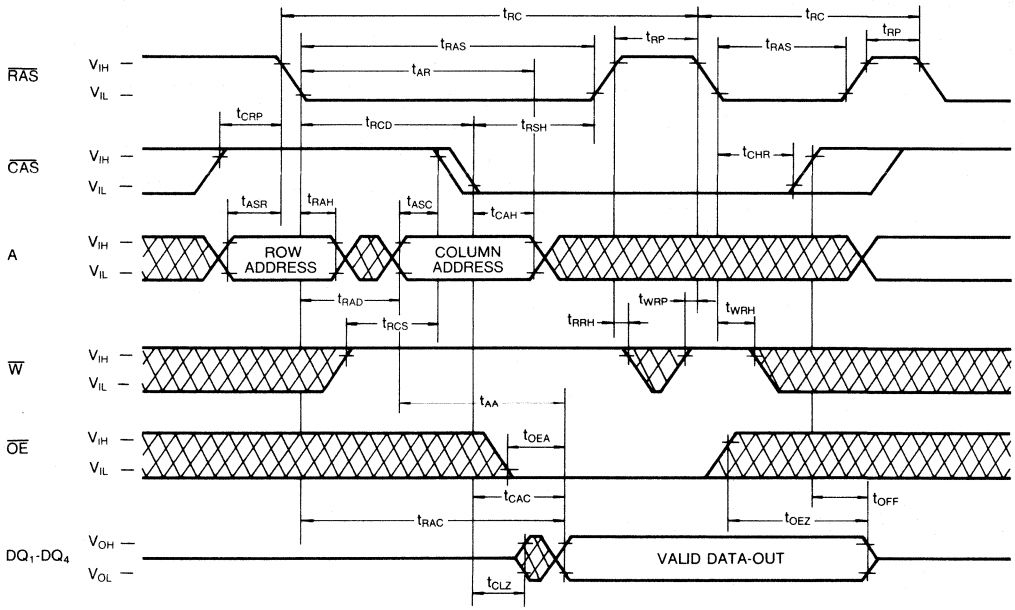
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

Note: $\overline{OE}$, Address=Don't Care

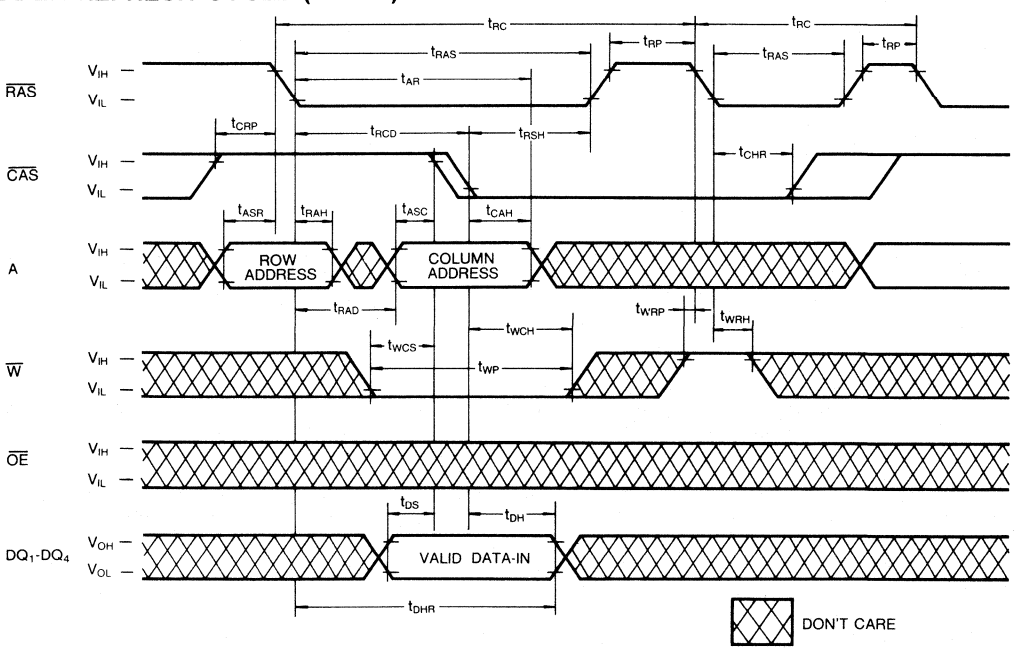


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

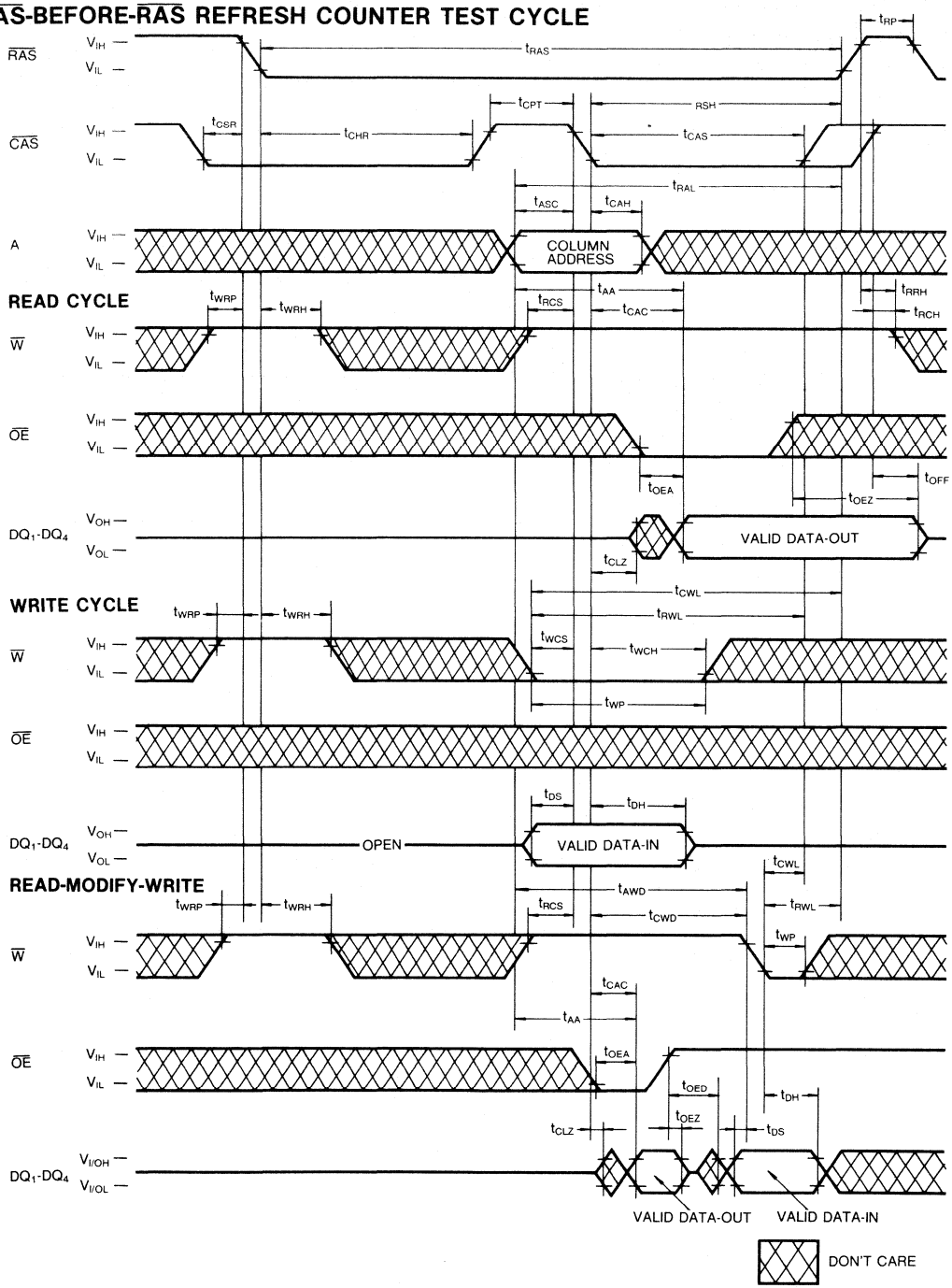


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

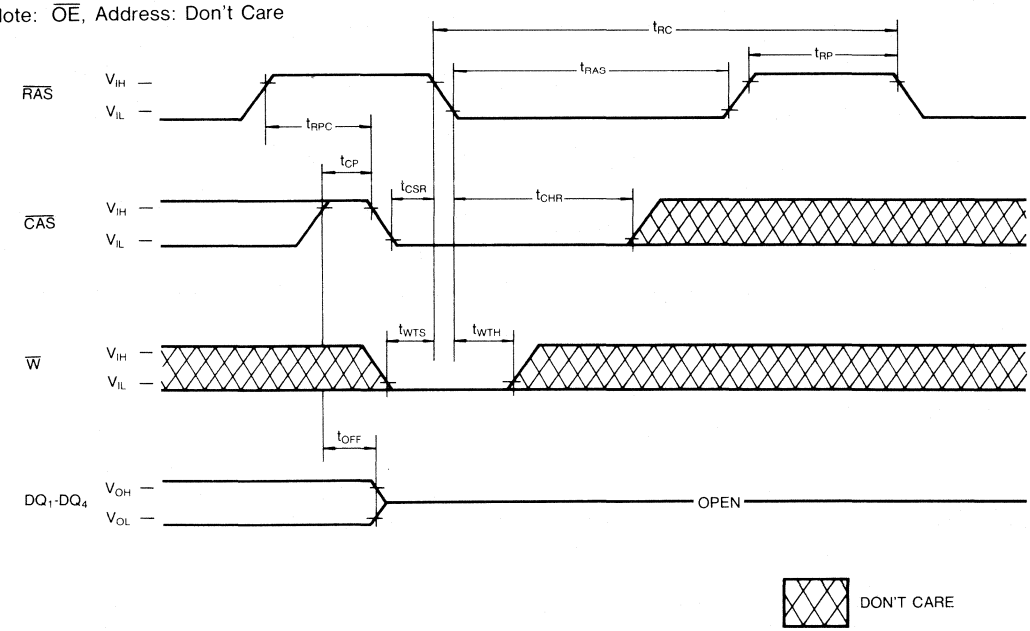
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: $\overline{OE}$, Address: Don't Care



TEST MODE DESCRIPTION

The KM44C4100L is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0 and $A_1$are not used. If, upon reading, four bits on one D/Q pin are equal (all "1"s or "0"s) the D/Q pin indicates a "1". If they were not equal, the D/Q pin would indicate a "0". In "Test Mode", the 4M×4 DRAM can be tested as if it were a 1M×4 DRAM. $\overline{W}$, $\overline{CAS}$-BEFORE-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE "or" "$\overline{RAS}$-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

DEVICE OPERATIONS

The KM44C4100L contains 4,194,304 x 4 memory locations. Twenty-four address bits are required to address a particular memory location. Since the KM44C4100L has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the KM44C4100L begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM44C4100L cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C4100L begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max). The KM44C4100L has common data I/O pins. The this reason an output enable control input ($\overline{OE}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{OE}$ must be low for the period of time defined by t_{OEA} and t_{OEZ}.

Write

The KM44C4100L can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$, $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the three state regardless of the state of the OE input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing W low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD}, t_{CWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44C4100L has a three-state output buffer which is controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever $\overline{CAS}$ and $\overline{OE}$ are high (V_{IH}), the outputs are in the high impedance state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM44C4100L operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} are not met)

Refresh

The data in the KM44C4100L is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 256 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 2048 row address (A_0-A_{10}).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM44C4100L has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM44C4100L hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C4100L by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, is $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows:

Row Address — Bits A_0 through A_{10} are supplied by tthe on-chip refresh counter.

Column Address — Bits A_0 through A_{10} are strobed-in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{CAS}$-before-$\overline{RAS}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 2048 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 2048 times so that highs are written into the 2048 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

If $\overline{RAS} = V_{SS}$ during power-up, the KM44C4100L could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid VIH in order to minimize the power-up current.

DEVICE OPERATION (Continued)

An initial pause of 200 μsec is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is assured. Eight initialization cycles are also required after any 256 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C4100L inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C4100L input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

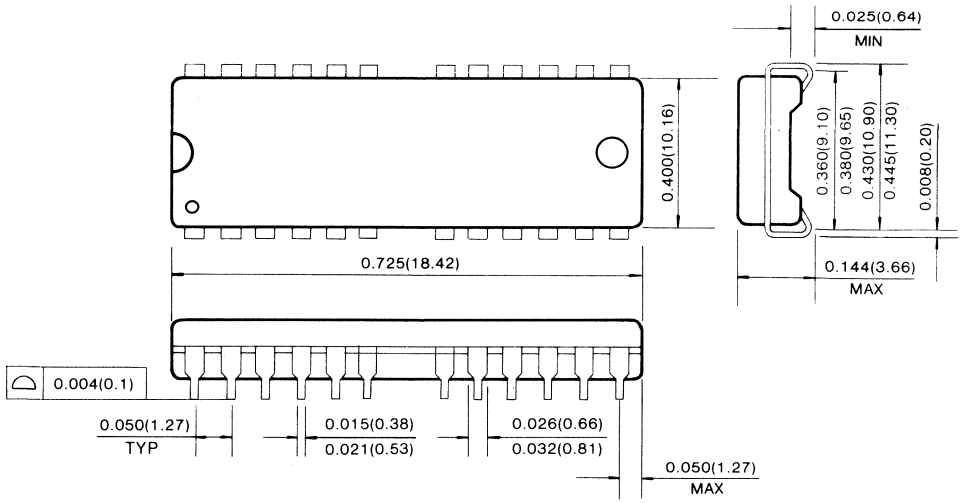
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM44C4100L using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C4100L and they supply much of the current used by the KM44C4100L during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

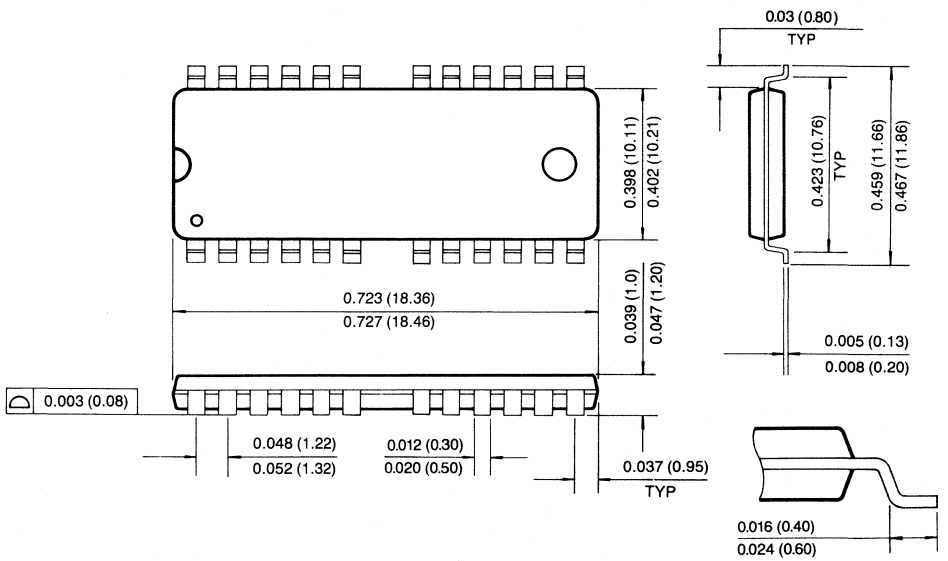
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (Forward and Reverse Type)



2M x 8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM48C2000-6	60ns	20ns	110ns
KM48C2000-7	70ns	20ns	130ns
KM48C2000-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Dual +5V ± 10% power supply**
- **4096 cycles/64ms refresh**
- **JEDEC Standard pinout**
- **Available in Plastic SOJ**

GENERAL DESCRIPTION

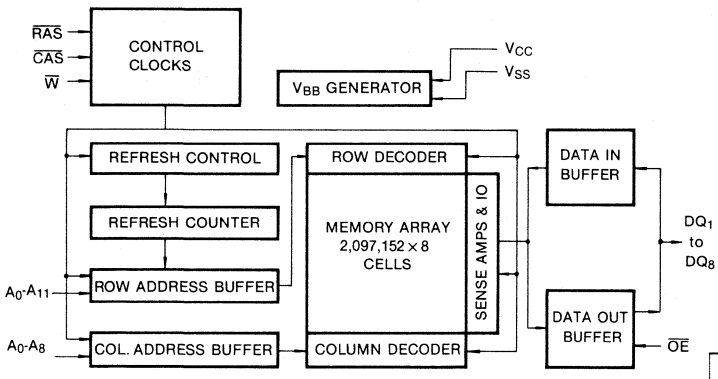
The Samsung KM48C2000 is a CMOS high speed 2,097,152 bit x 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance portable computers.

The KM48C2000 features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM48C2000 is fabricated using Samsung's advanced CMOS process.

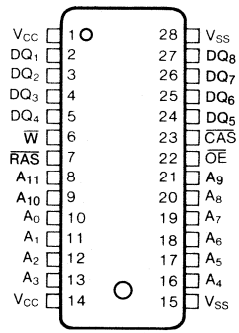
2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)

- **KM48C2000J**



Pin Name	Pin Function
A_0-A_{11}	Address Inputs
DQ_{1-8}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power (+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{STG}	−55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, $T_A = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	$V_{CC}+1$	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC} = min.)	KM48C2000-6	I_{CC1}	—	100	mA
	KM48C2000-7		—	90	mA
	KM48C2000-8		—	80	mA
Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS} = V_{IH}$, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM48C2000-6	I_{CC3}	—	100	mA
	KM48C2000-7		—	90	mA
	KM48C2000-8		—	80	mA
Fast Page Mode Current* ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling @t_{PC} = min.)	KM48C2000-6	I_{CC4}	—	100	mA
	KM48C2000-7		—	90	mA
	KM48C2000-8		—	80	mA
Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min.)	KM48C2000-6	I_{CC6}	—	100	mA
	KM48C2000-7		—	90	mA
	KM48C2000-8		—	80	mA
Standby Current ($\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IL}$, D_{OUT} = Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input $0 \le V_{IN} \le 6.5V$, all other pins not under test = 0V)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le 5.5V$)		I_{OL}	−10	10	μA
Output High Voltage Level ($I_{OH} = -5mA$)		V_{OH}	2.4	—	V
Output Low Voltage Level ($I_{OL} = 4.2mA$)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS} = V_{IL}$. In I_{CC4}, Address can be changed maximum once while $\overline{CAS} = V_{IH}$.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{11})	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	6	pF
Output Capacitance (DQ_1-DQ_8)	C_{DQ}	—	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$, See notes 1, 2)

Parameter	Symbol	KM48C2000-6		KM48C2000-7		KM48C2000-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	165		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	15		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	

AC CHARACTERISTICS (Continued)

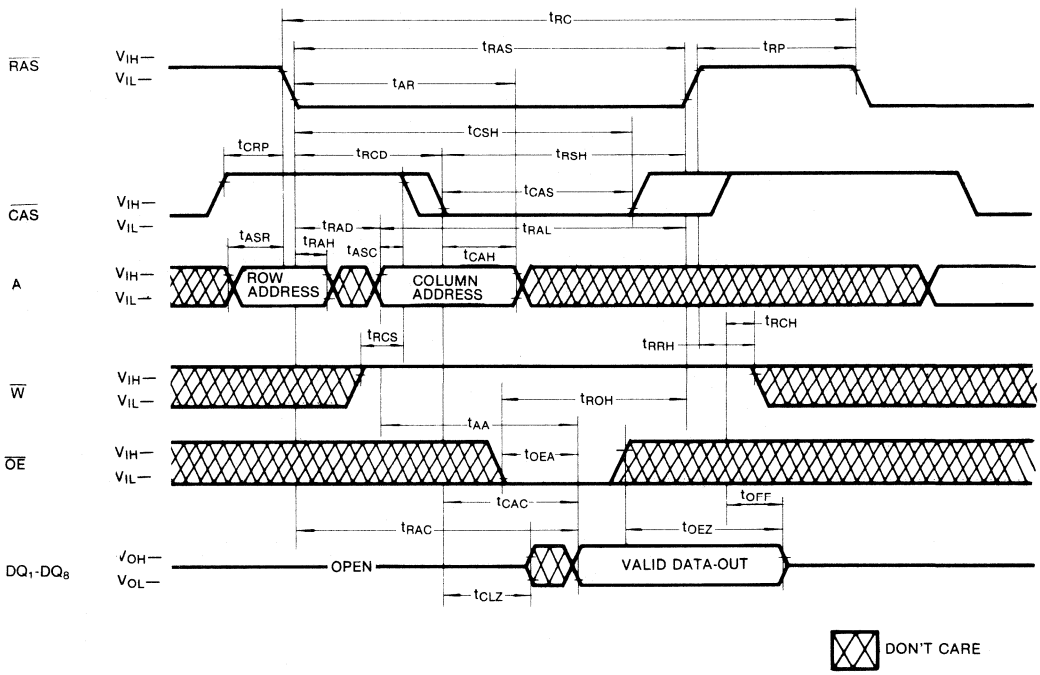
Parameter	Symbol	KM48C2000-6		KM48C2000-7		KM48C2000-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (4096 cycles)	t_{REF}		64		64		64	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	85		100		105		ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	20		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	15		20		20		ns	
Write command set-up time (test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} to V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or r_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point ony. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

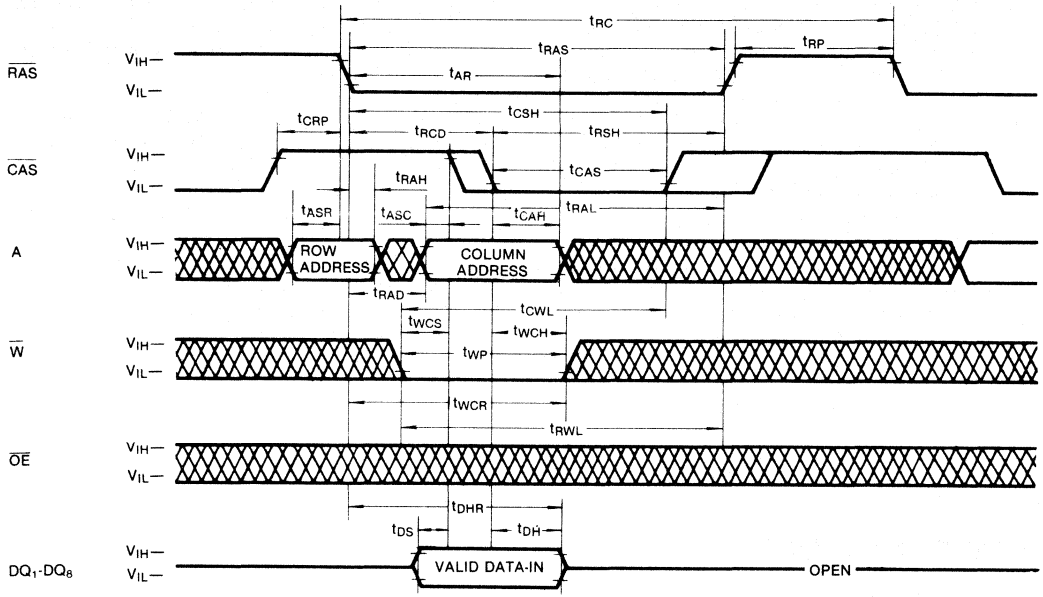
TIMING DIAGRAMS

READ CYCLE

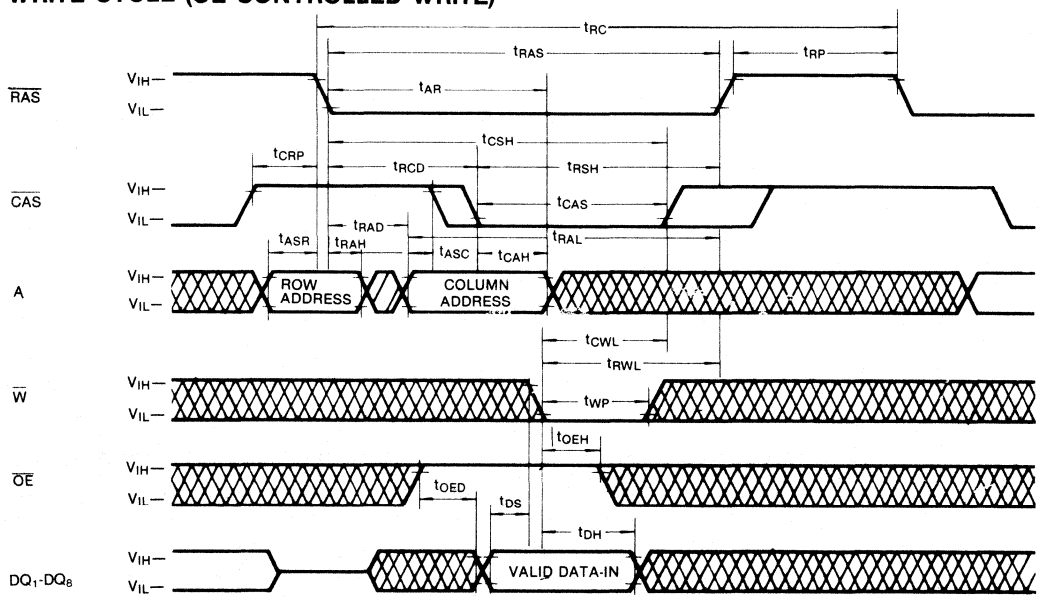


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



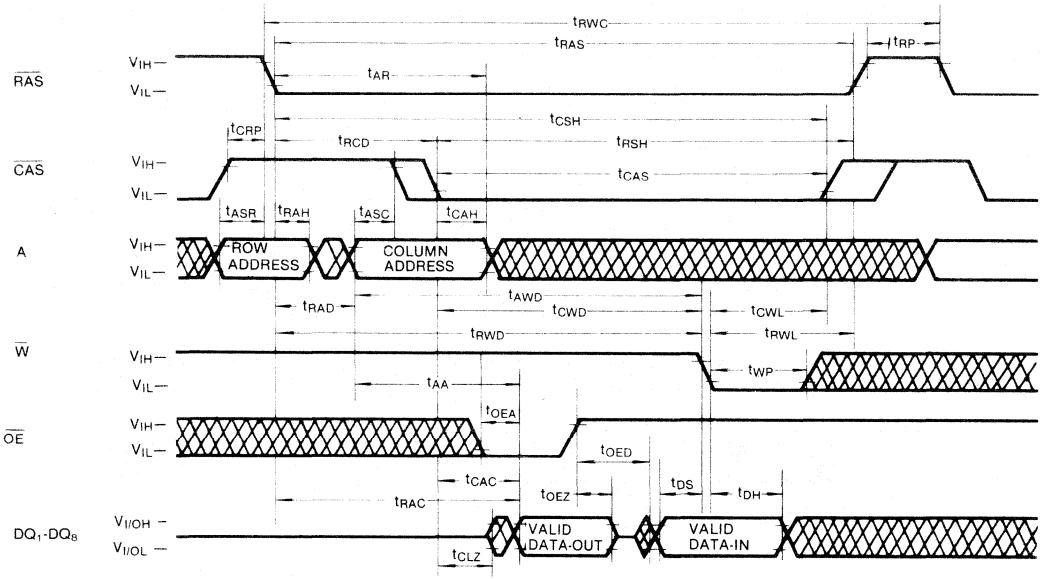
WRITE CYCLE (OE CONTROLLED WRITE)



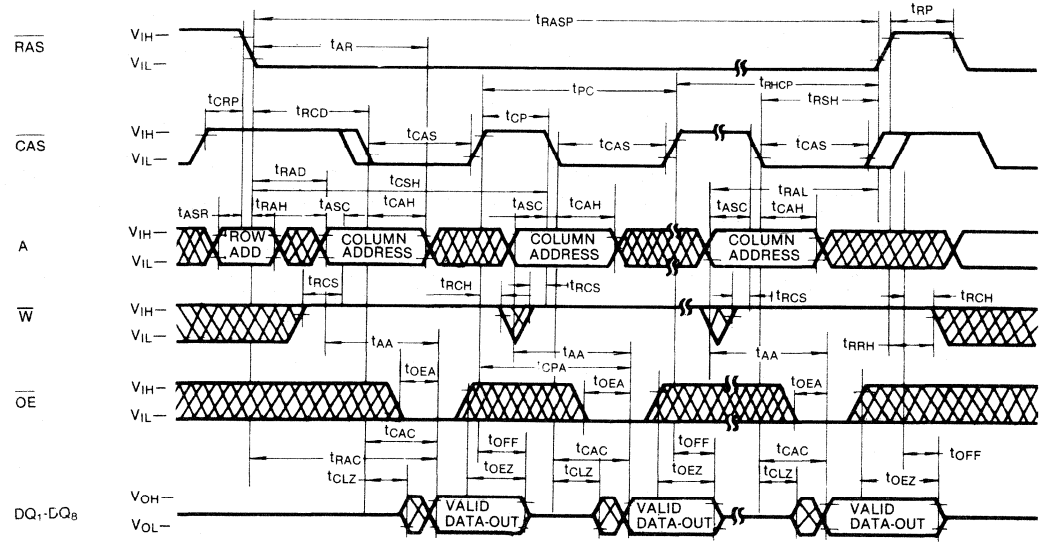
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



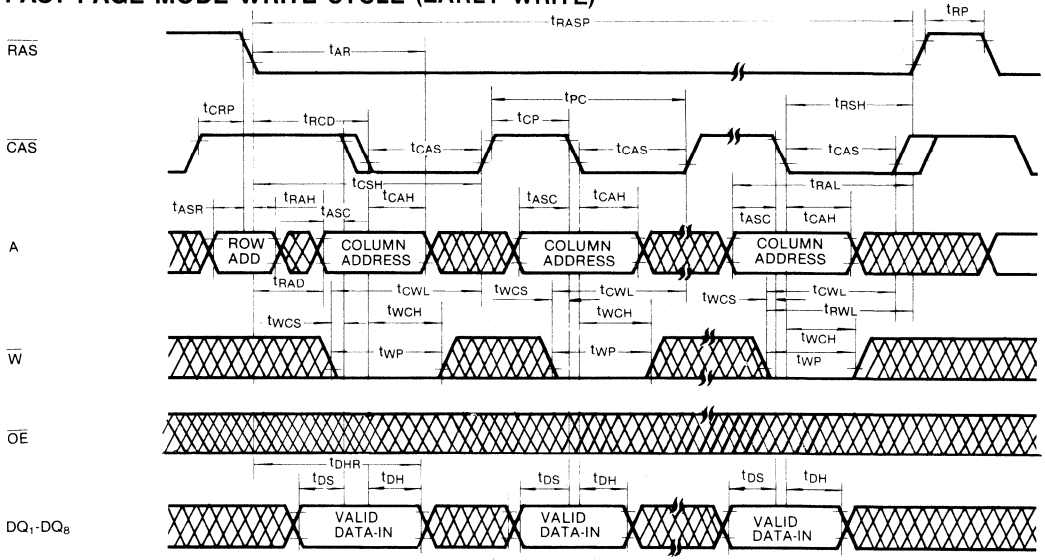
FAST PAGE MODE READ CYCLE



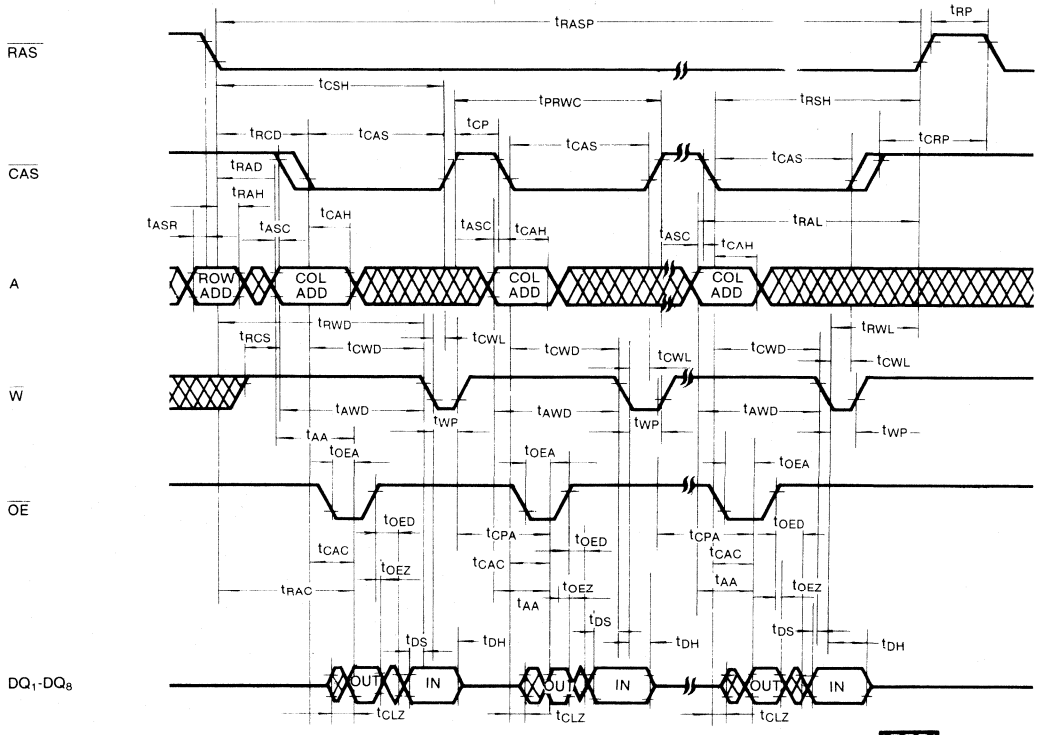
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



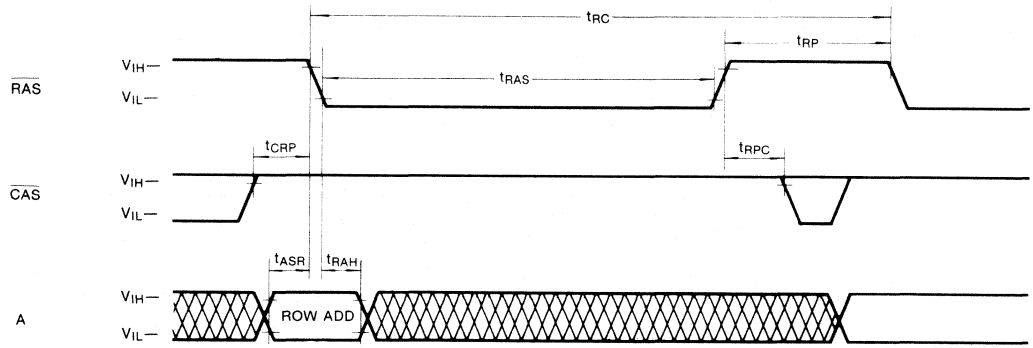
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

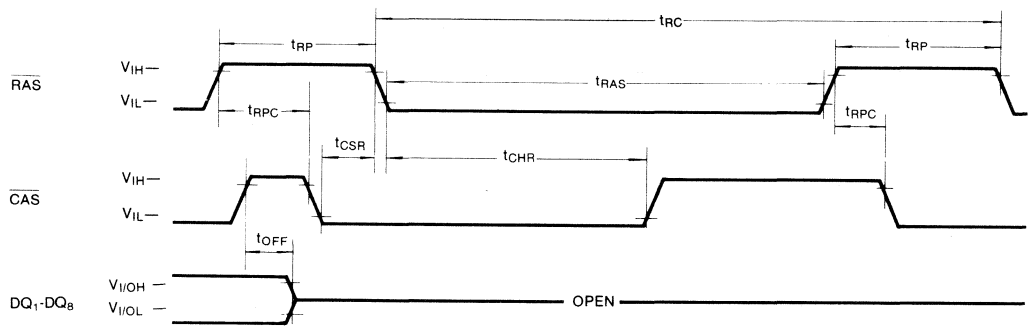
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

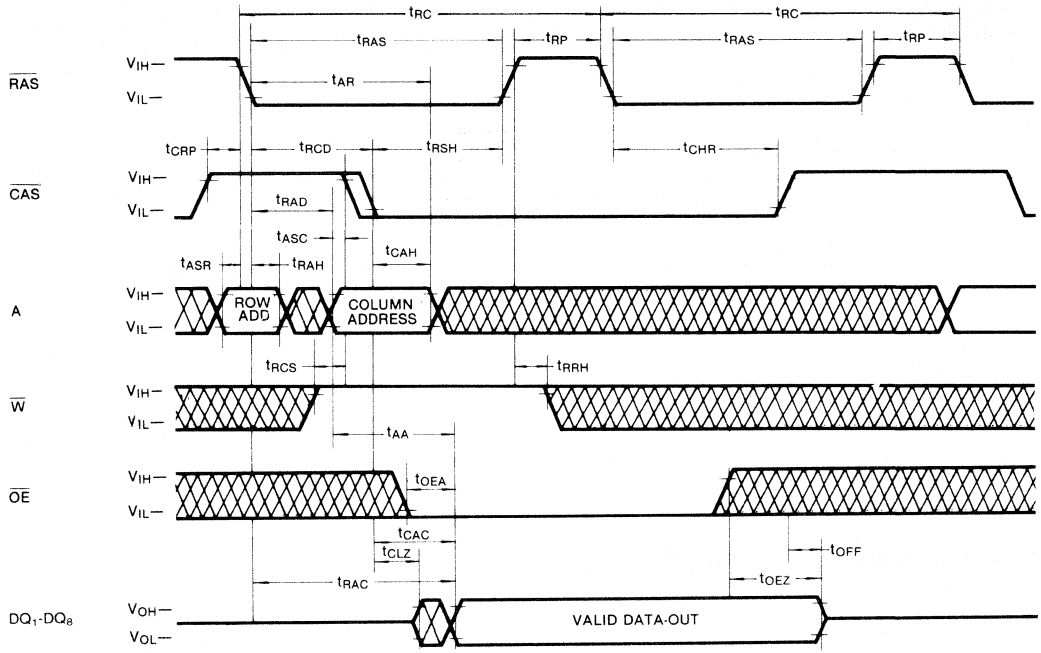
NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



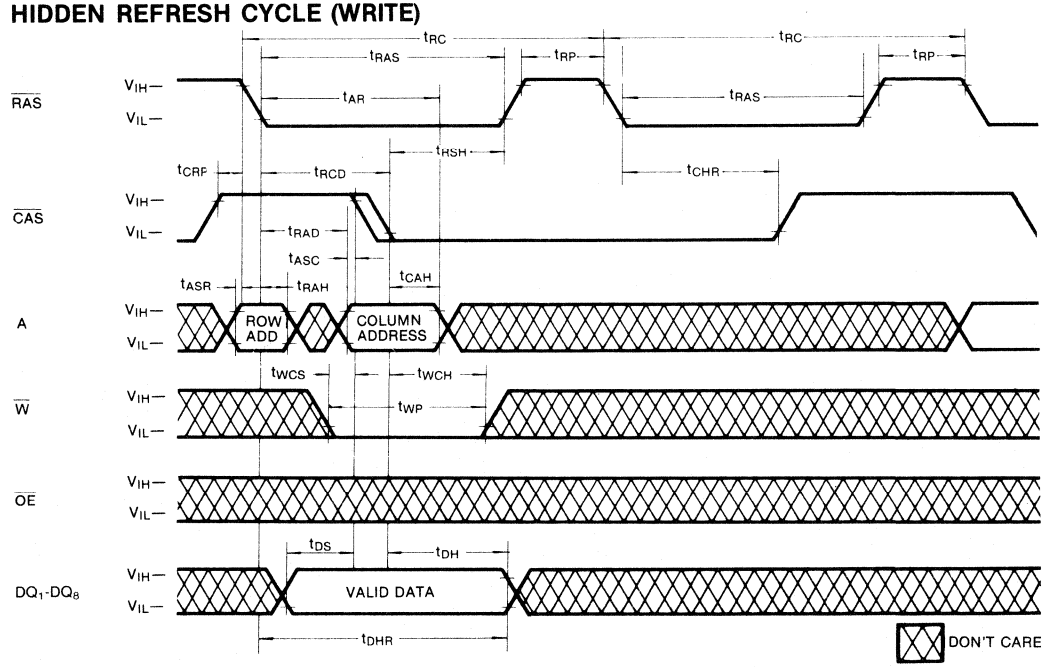
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

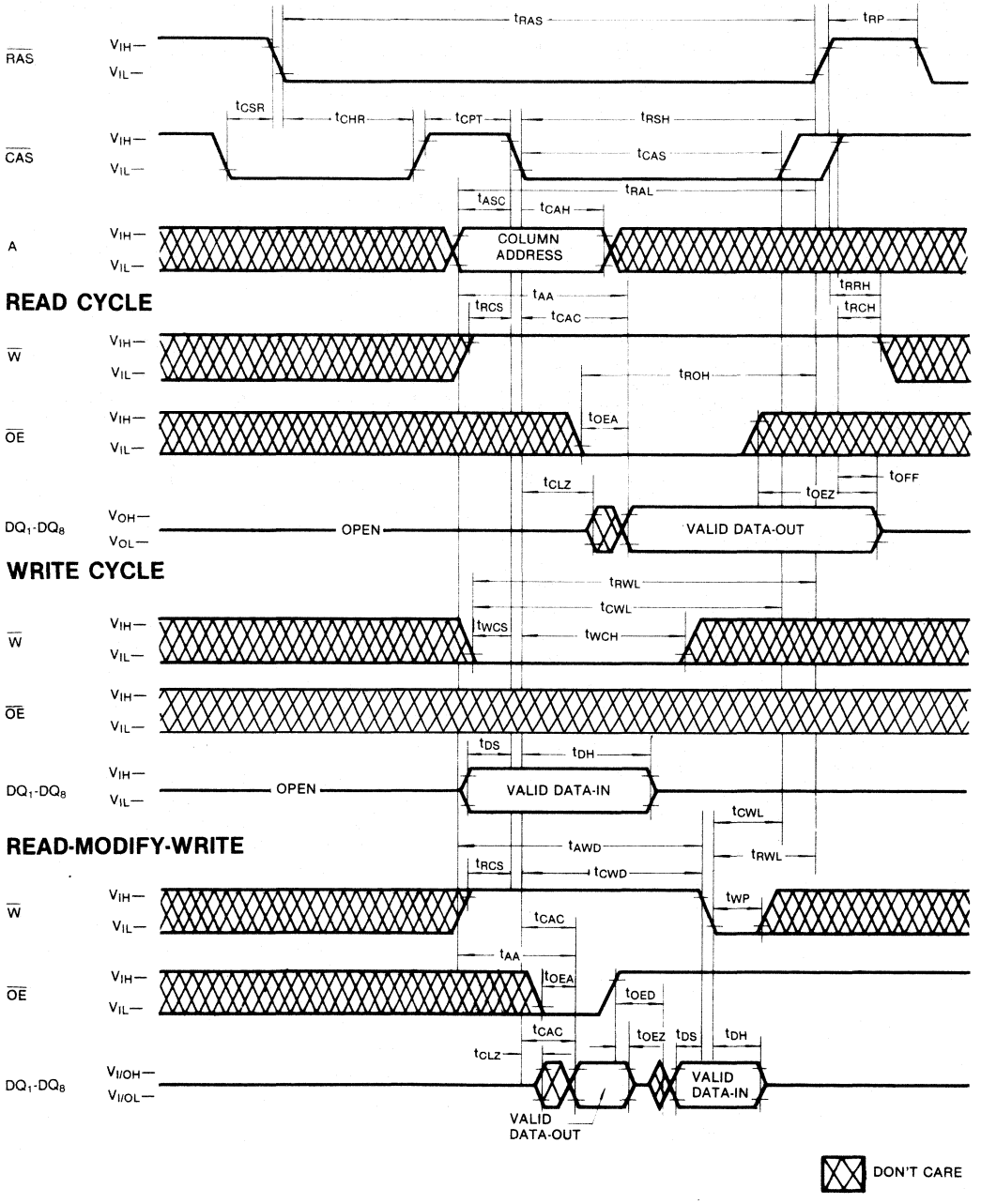


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM48C2000 contains 16,777,216 memory locations arranged in 8 groups of 2,097,152 x 1 bit each. Twenty-one address bits are required to address a particular memory location. Since the KM48C2000 has only 12 address input pins, time multiplexed addressing is used to input 12 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM48C2000 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 12 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM48C2000 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM48C2000 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. Additionally the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{CAS}$ transitions to a low before t_{RCD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ transitions low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM48C2000 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$, $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 8-bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cells appears at the output before and during the time that data is being written into the same cells. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The $\overline{OE}$ input must be low during the time defined by t_{OEA} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM48C2000 DQ pins.

Data Output

The KM48C2000 has a three-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}), the outputs are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs enter into the low impedance state in the time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM48C2000 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} times are not met)

DEVICE OPERATION (Continued)

Refresh

The data in the KM48C2000 is stored as a charge on microscopic capacitor within each memory cell. The stored charge tends to dissipate over time and will affect data integrity if the charge is not periodically refreshed. Refresh of the individual storage cells is accomplished by accessing all rows within the refresh period (t_{REF}) of within 64ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 4096 row address (A_0-A_{11}).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM48C2000 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If either $\overline{CAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ transitions low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending either $\overline{CAS}$ input active time and cycling $\overline{RAS}$. The hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM48C2000 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM48C2000 has Fast page mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is asserted high and then low again while $\overline{RAS}$ is asserted low, the read and write operations are enabled. In this method, the row address bits A0 through A11 are supplied by on chip refresh counter.

Power-up

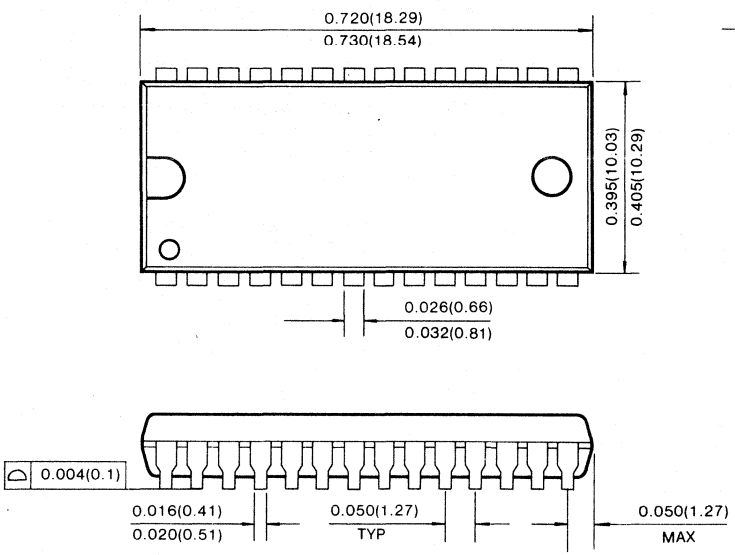
If $\overline{RAS} = V_{SS}$ during power-up, the KM48C2000 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200μs is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8ms period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



2M x 8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM48C2100-6	60ns	20ns	110ns
KM48C2100-7	70ns	20ns	130ns
KM48C2100-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Byte Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Dual +5V ± 10% power supply**
- **2048 cycles/32ms refresh**
- **JEDEC Standard pinout**
- **Available in Plastic SOJ**

GENERAL DESCRIPTION

The Samsung KM48C2100 is a CMOS high speed 2,097,152 bit x 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance portable computers.

The KM48C2100 features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM48C2100 is fabricated using Samsung's advanced CMOS process.

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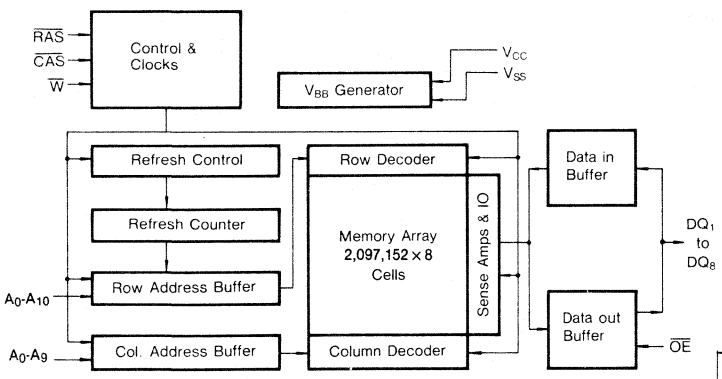
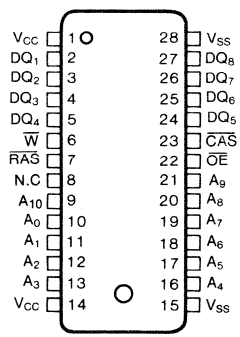
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)

- **KM48C2100J**



Pin Name	Pin Function
A_0-A_{10}	Address Inputs
DQ_{1-8}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power (+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{STG}	−55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, $T_A = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	$V_{CC}+1$	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @t_{RC} = min.)	KM48C2100-6	I_{CC1}	—	120	mA
	KM48C2100-7		—	110	mA
	KM48C2100-8		—	100	mA
Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS} = V_{IH}$, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM48C2100-6	I_{CC3}	—	120	mA
	KM48C2100-7		—	110	mA
	KM48C2100-8		—	100	mA
Fast Page Mode Current* ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling @t_{PC} = min.)	KM48C2100-6	I_{CC4}	—	110	mA
	KM48C2100-7		—	100	mA
	KM48C2100-8		—	90	mA
Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC} = min.)	KM48C2100-6	I_{CC6}	—	120	mA
	KM48C2100-7		—	110	mA
	KM48C2100-8		—	100	mA
Standby Current ($\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IL}$, D_{OUT} = Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input $0 \le V_{IN} \le 6.5V$, all other pins not under test = 0V)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le 5.5V$)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS} = V_{IL}$. In I_{CC4}, Address can be changed maximum once while $\overline{CAS} = V_{IH}$.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{10})	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	6	pF
Output Capacitance (DQ_1-DQ_8)	C_{DQ}	—	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$, See notes 1, 2)

Parameter	Symbol	KM48C2100-6		KM48C2100-7		KM48C2100-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	165		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	6
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	6
Write command pulse width	t_{WP}	15		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		20		ns	

AC CHARACTERISTICS (Continued)

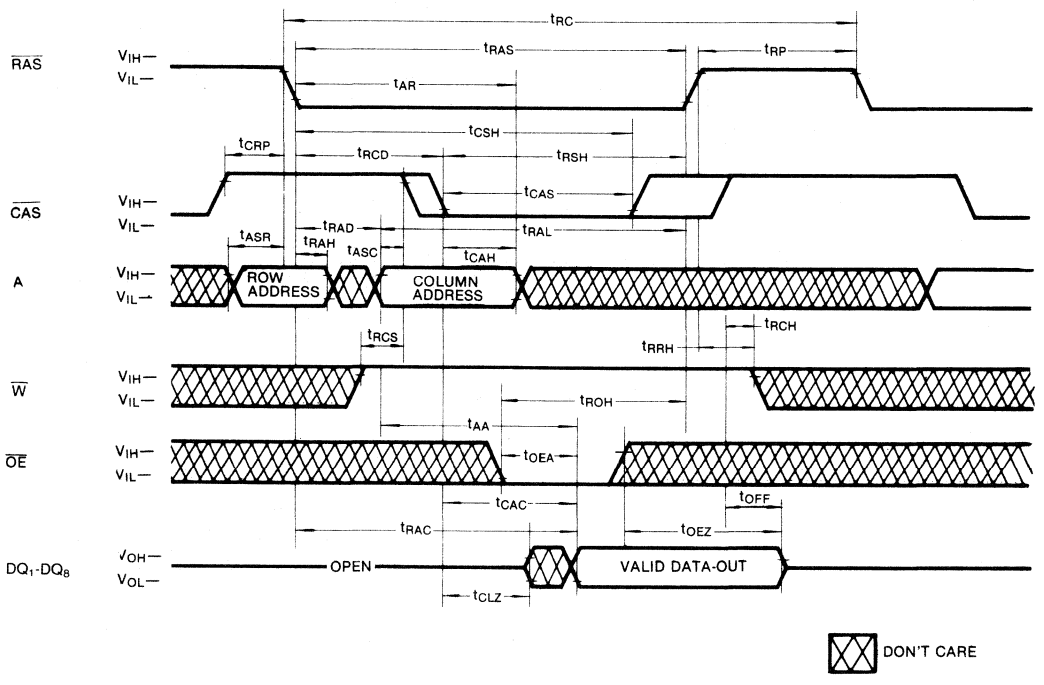
Parameter	Symbol	KM48C2100-6		KM48C2100-7		KM48C2100-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		15		ns	10
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	6
Refresh period (2048 cycles)	t_{REF}		32		32		32	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	85		100		110		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	55		65		70		ns	8
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	20		30		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40		45	ns	3
Fast page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write cycle time	t_{PRWC}	85		100		105		ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		20		20	ns	
$\overline{OE}$ to data delay	t_{OED}	20		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t_{OEH}	15		20		20		ns	
Write command set-up time (test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (test mode in)	t_{WTH}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ only or $\overline{CAS}$-before-$\overline{RAS}$ refresh-cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

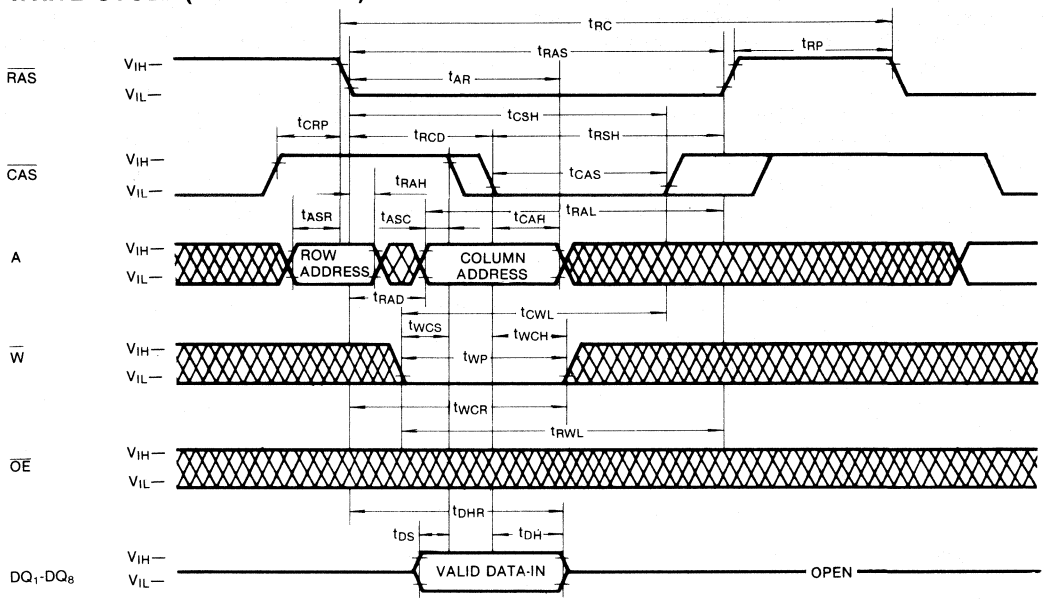
TIMING DIAGRAMS

READ CYCLE

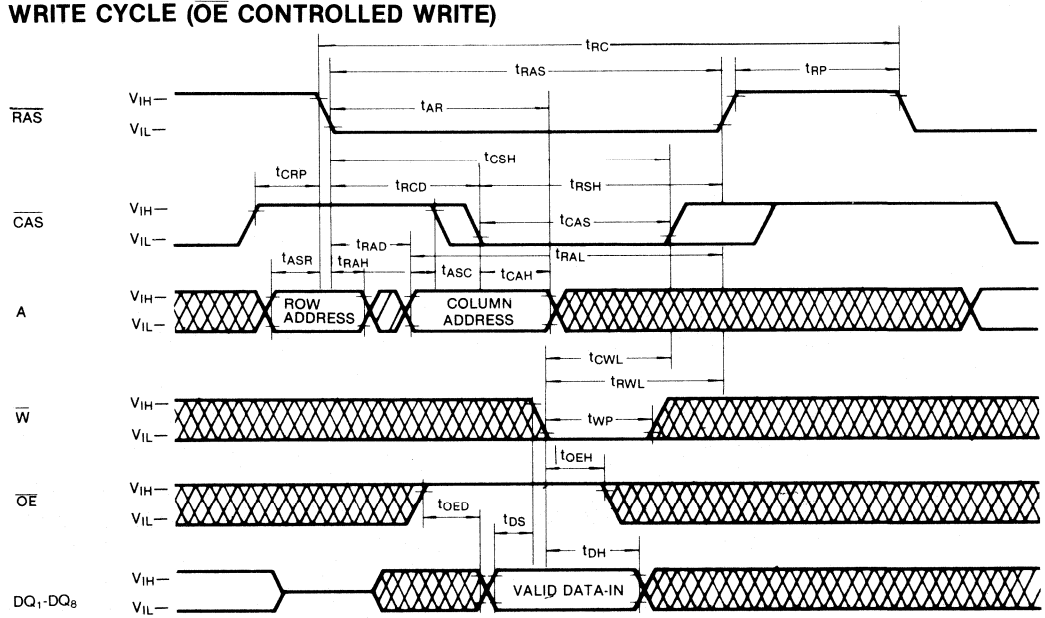


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



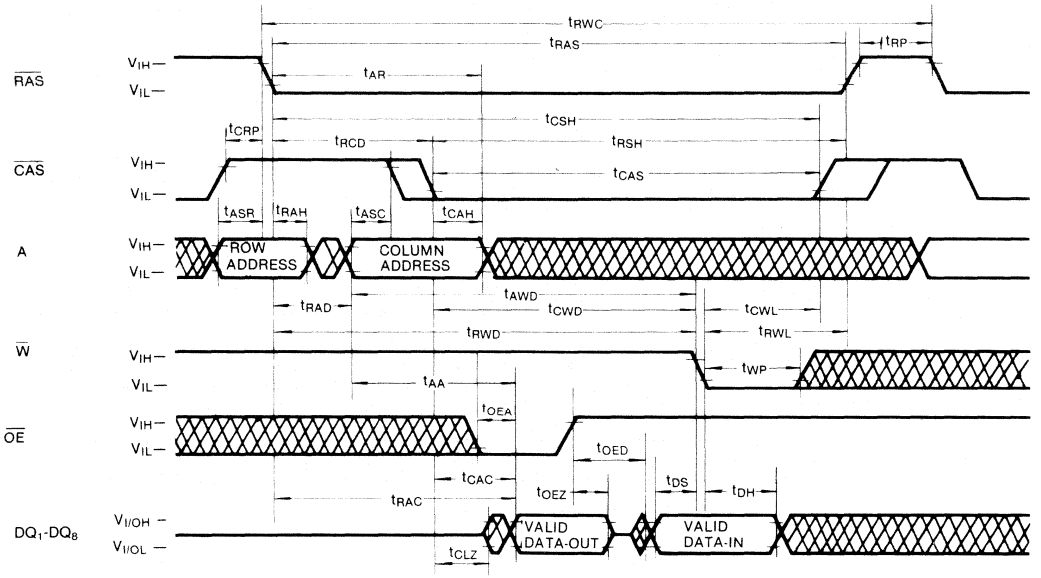
WRITE CYCLE (OE CONTROLLED WRITE)



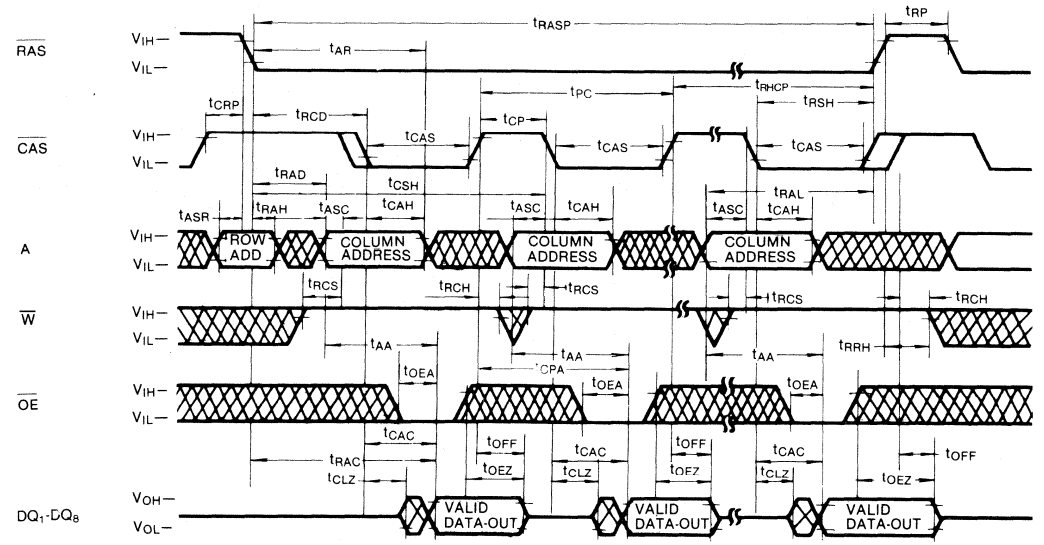
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



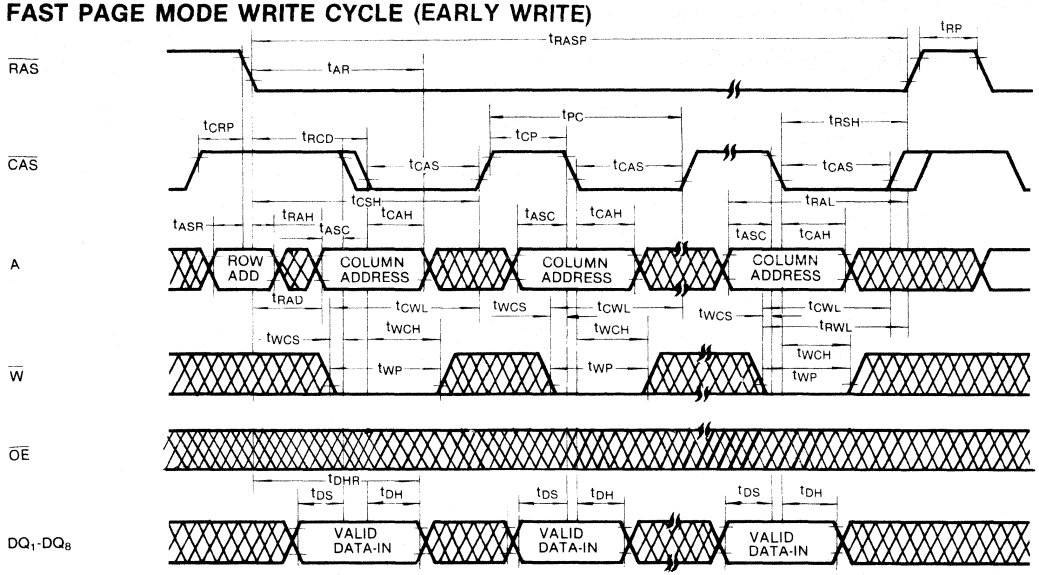
FAST PAGE MODE READ CYCLE



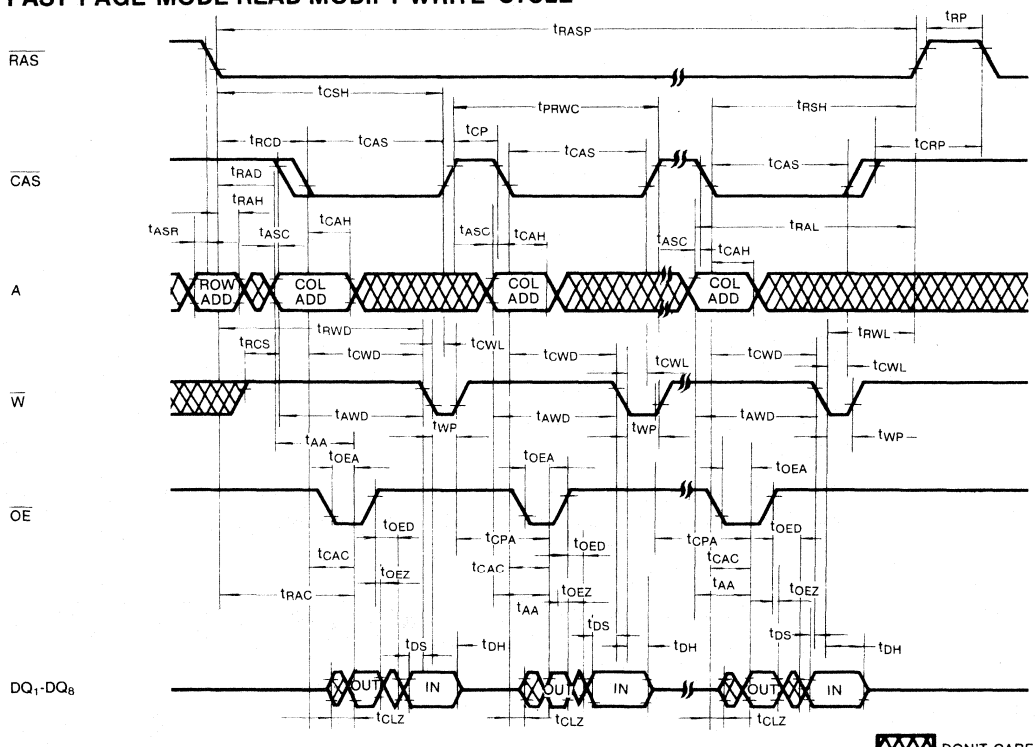
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



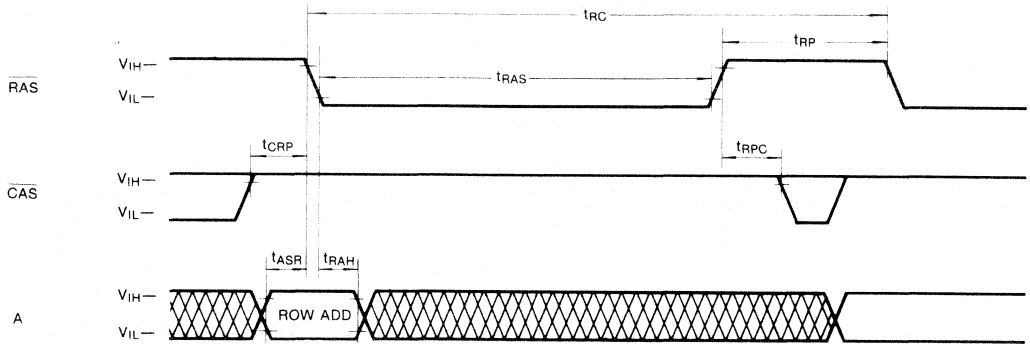
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

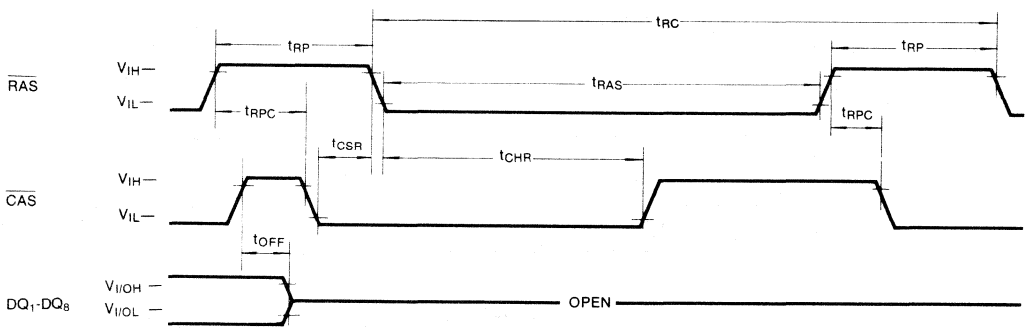
$\overline{RAS}$-ONLY REFRESH CYCLE

Note: $\overline{W}$, $\overline{OE}$ = Don't care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

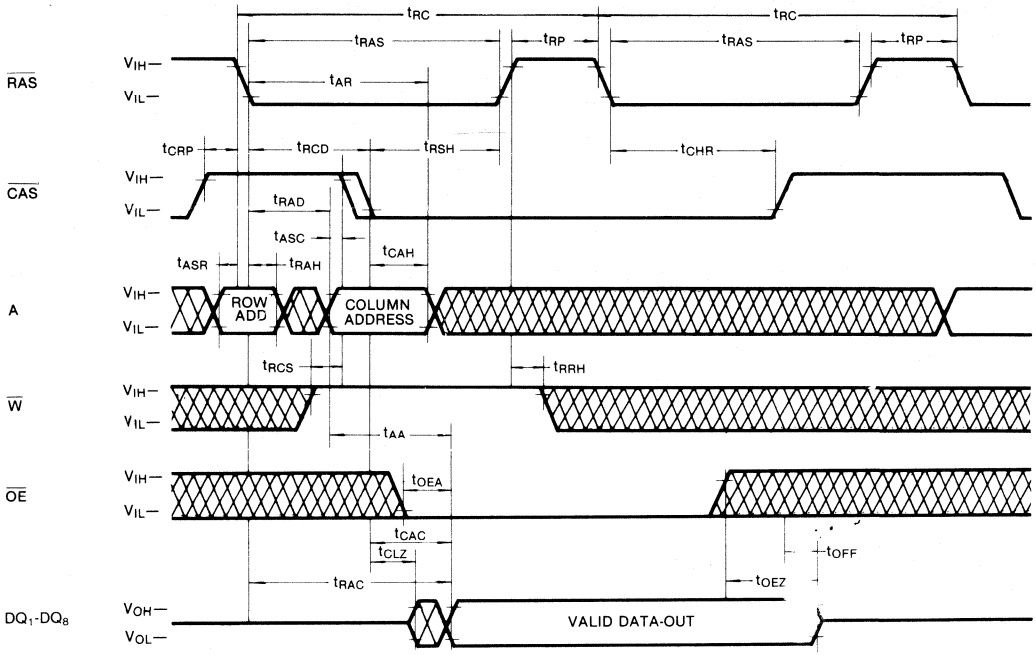
NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



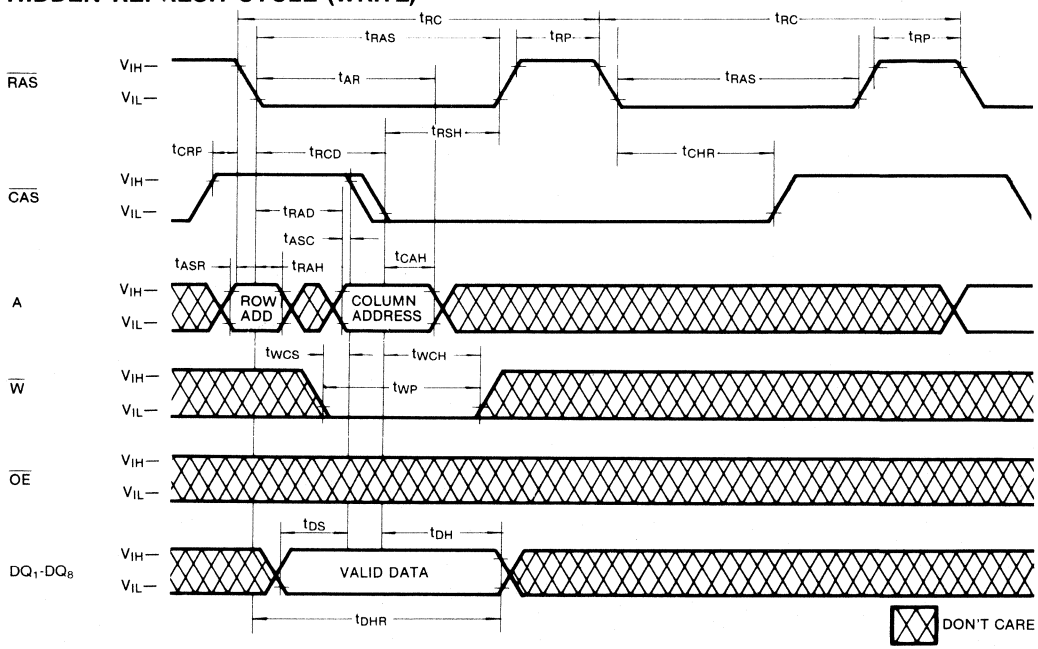
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

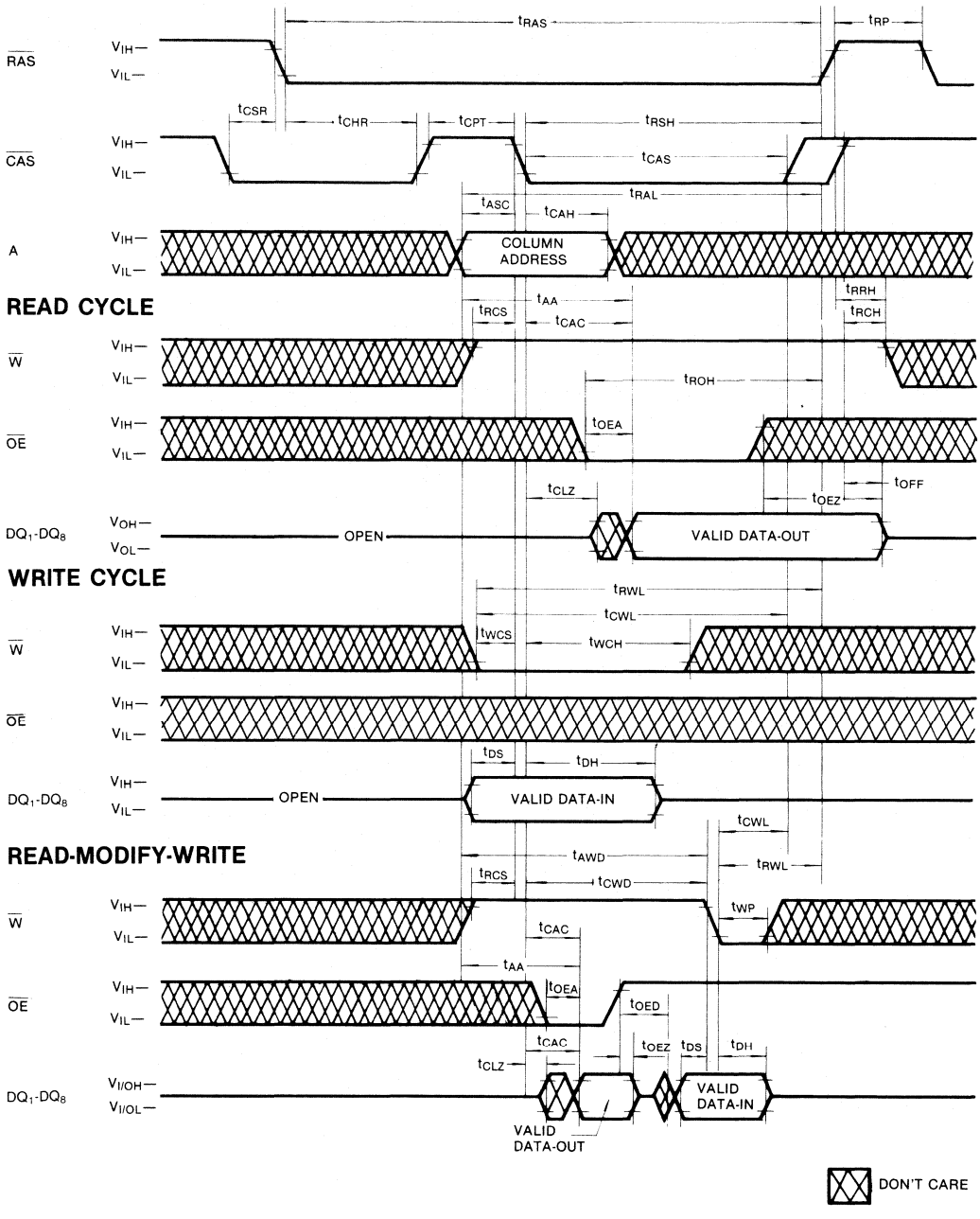


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM48C2100 contains 16,777,216 memory locations arranged in 8 groups of 2,097,152 x 1 bit each. Twenty-one address bits are required to address a particular memory location. Since the KM48C2100 has only 11 address input pins, time multiplexed addressing is used to input 11 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM48C2100 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM48C2100 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM48C2100 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. Additionally the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{CAS}$ transitions to a low before t_{RCD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ transitions low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM48C2100 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$, $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The 8-bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cells appears at the output before and during the time that data is being written into the same cells. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The $\overline{OE}$ input must be low during the time defined by t_{OEA} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM48C2100 DQ pins.

Data Output

The KM48C2100 has a three-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}), the outputs are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs enter into the low impedance state in the time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM48C2100 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} times are not met)

DEVICE OPERATION (Continued)

Refresh

The data in the KM48C2100 is stored as a charge on microscopic capacitor within each memory cell. The stored charge tends to dissipate over time and will affect data integrity if the charge is not periodically refreshed. Refresh of the individual storage cells is accomplished by accessing all rows within the refresh period (t_{REF}) of within 32ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 2048 row address (A_0-A_{10}).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM48C2100 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If either $\overline{CAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ transitions low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending either $\overline{CAS}$ input active time and cycling $\overline{RAS}$. The hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM48C2100 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM48C2100 has Fast page mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is asserted high and then low again while $\overline{RAS}$ is asserted low, the read and write operations are enabled. In this method, the row address bits A0 through A10 are supplied by on chip refresh counter.

Power-up

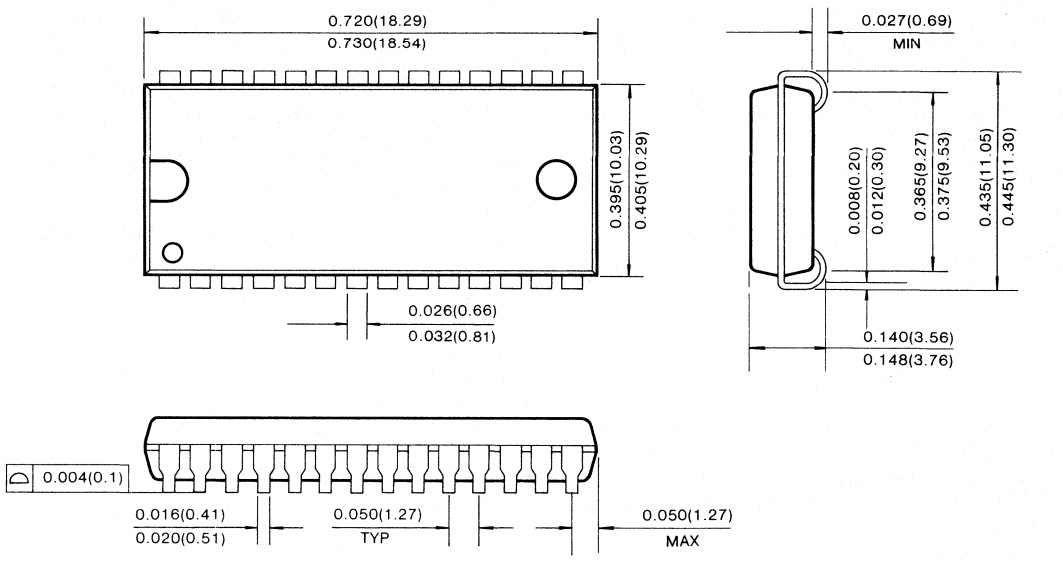
If $\overline{RAS} = V_{SS}$ during power-up, the KM48C2100 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200μs is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8ms period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



1M x 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM416C1000-7	70ns	20ns	130ns
KM416C1000-8	80ns	20ns	150ns
KM416C1000-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Triple +5V ± 10% power supply**
- **4096 cycles/64ms refresh**
- **JEDEC Standard pinout**
- **Available in Plastic SOJ**

GENERAL DESCRIPTION

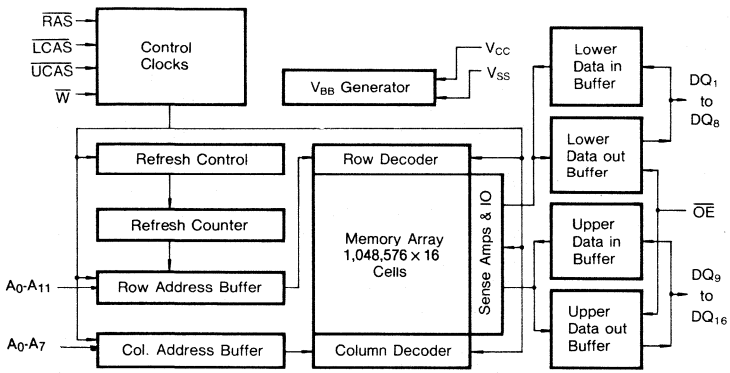
The Samsung KM416C1000 is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM416C1000 features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM416C1000 is fabricated using Samsung's advanced CMOS process.

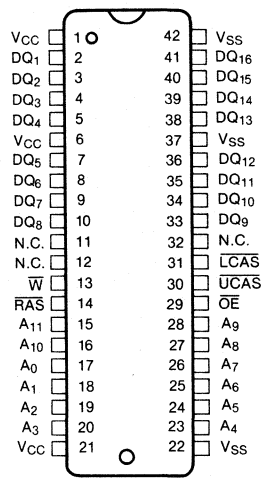
2

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)

• KM416C1000J



Pin Name	Pin Function
A_0-A_{11}	Address Inputs
DQ_{1-16}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power (+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$, or $\overline{LCAS}$, Address Cycling @t_{RC} = min.)	KM416C1000-7	I_{CC1}	—	100	mA
	KM416C1000-8		—	90	mA
	KM416C1000-10		—	80	mA
Standby Current ($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$)		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$ = $\overline{LCAS}$, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM416C1000-7	I_{CC3}	—	100	mA
	KM416C1000-8		—	90	mA
	KM416C1000-10		—	80	mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{PC} = min.)	KM416C1000-7	I_{CC4}	—	100	mA
	KM416C1000-8		—	90	mA
	KM416C1000-10		—	80	mA
Standby Current ($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ ≥ V_{CC} − 0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @t_{RC} = min.)	KM416C1000-7	I_{CC6}	—	100	mA
	KM416C1000-8		—	90	mA
	KM416C1000-10		—	80	mA
Standby Current ($\overline{RAS}$ = V_{IH}, $\overline{UCAS}$ or $\overline{LCAS}$ = V_{IL} D_{OUT} = Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC8} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$ = V_{IL}. In I_{CC4}, Address can be changed maximum once while $\overline{UCAS}$ and $\overline{UCAS}$ = V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{11})	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_{16})	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	KM416C1000-7		KM416C1000-8		KM416C1000-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	185		205		245		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10

AC CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC}=5.0V \pm 10\%$, See notes 1,2)

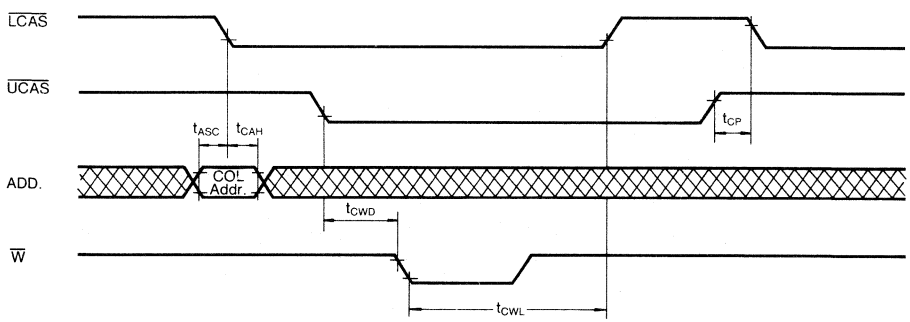
Parameter	Symbol	KM416C1000-7		KM416C1000-8		KM416C1000-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (4096 cycles)	t_{REF}		64		64		64	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	50		50		60		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	100		110		135		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	65		70		85		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		55	ns	3
Fast page mode cycle time	t_{PC}	45		50		60		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	100		105		125		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	45		45		55		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

KM416C1000 Truth Table

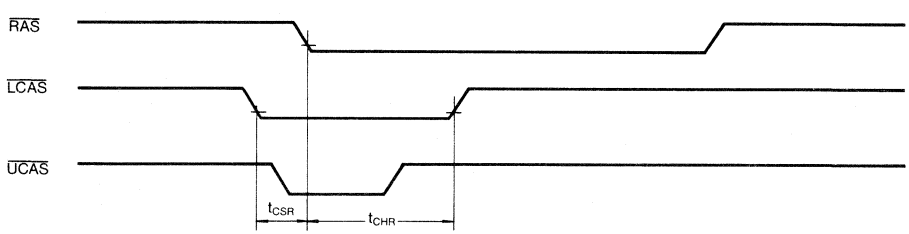
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	$DQ_{1\sim8}$	$DQ_{9\sim16}$	State
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Lower Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-In	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	—

NOTES

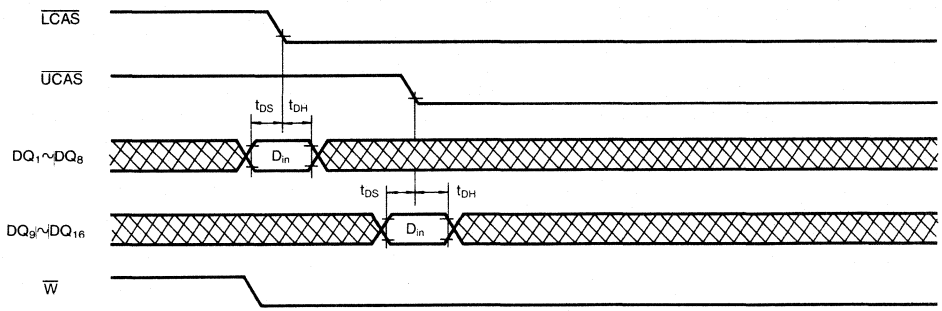
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating aprameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
17. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.

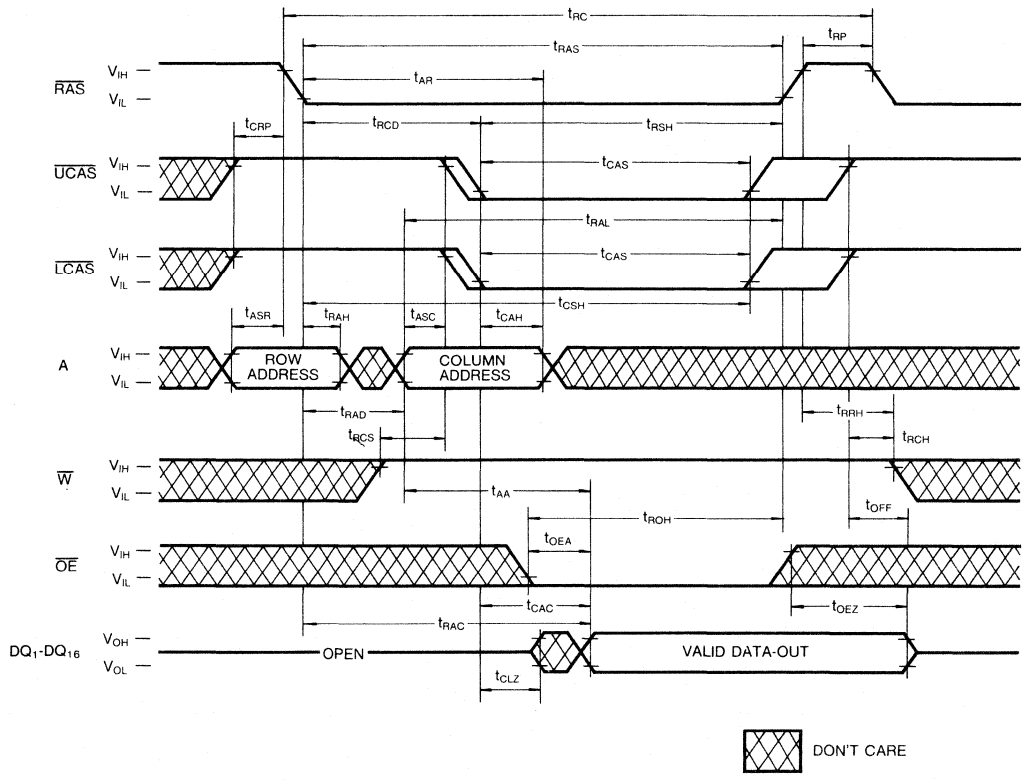


18. t_{DS}, t_{DH} is independetly specified for lower byte $D_{in(1\sim8)}$, upper byte $D_{in(9\sim16)}$



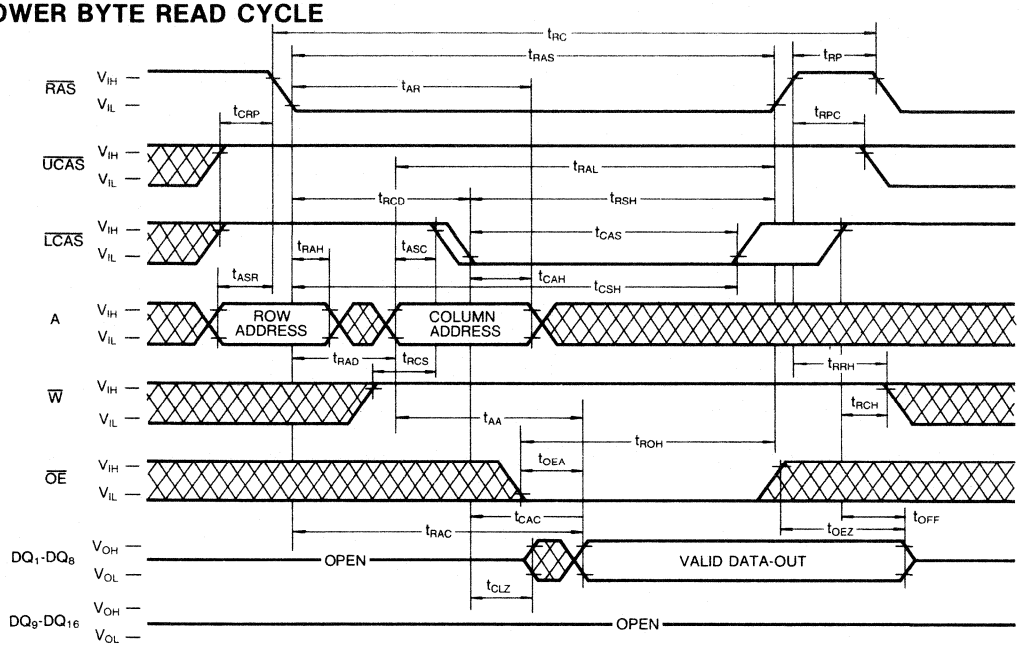
TIMING DIAGRAMS

WORD READ CYCLE

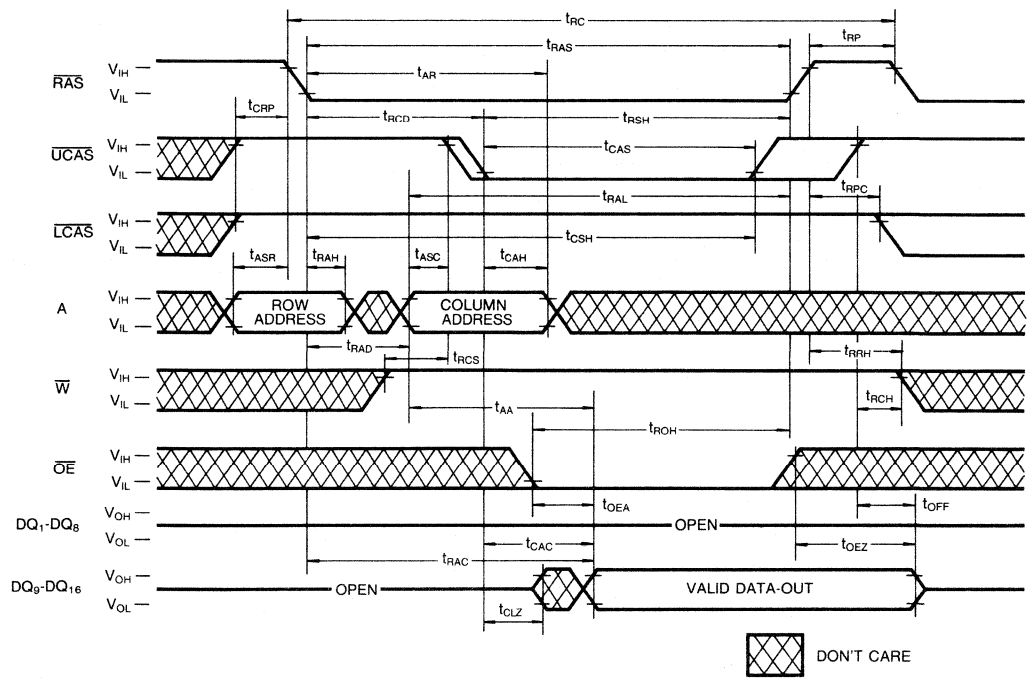


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE

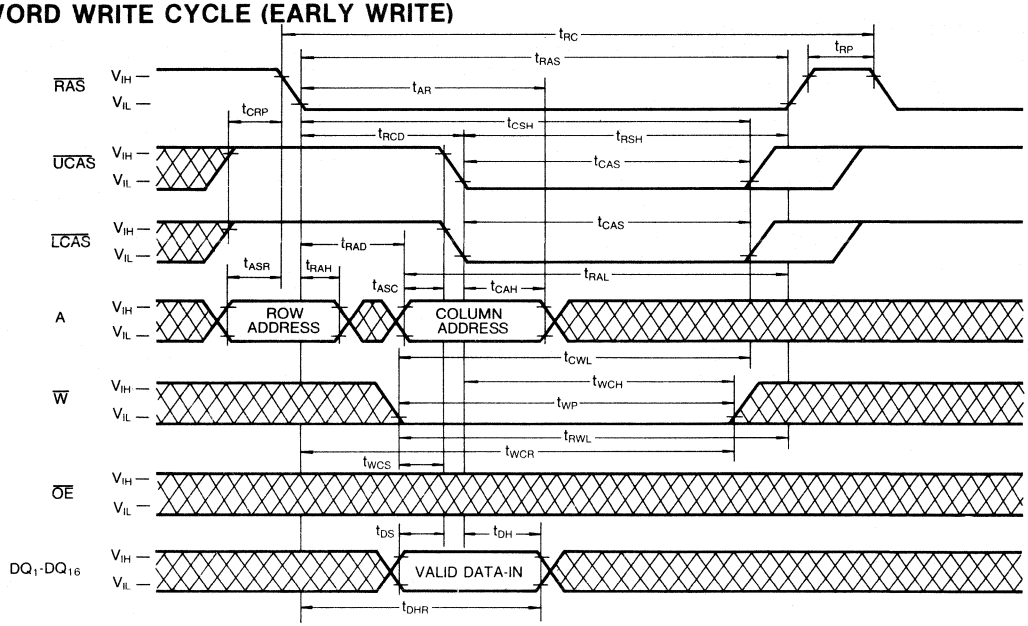


UPPER BYTE READ CYCLE

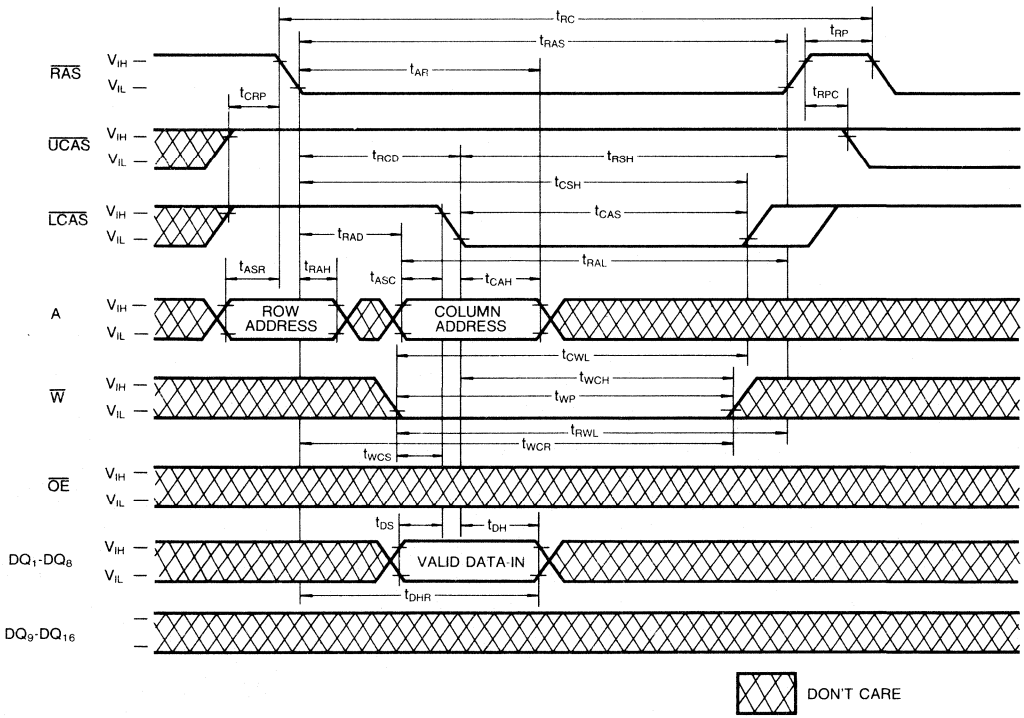


TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)

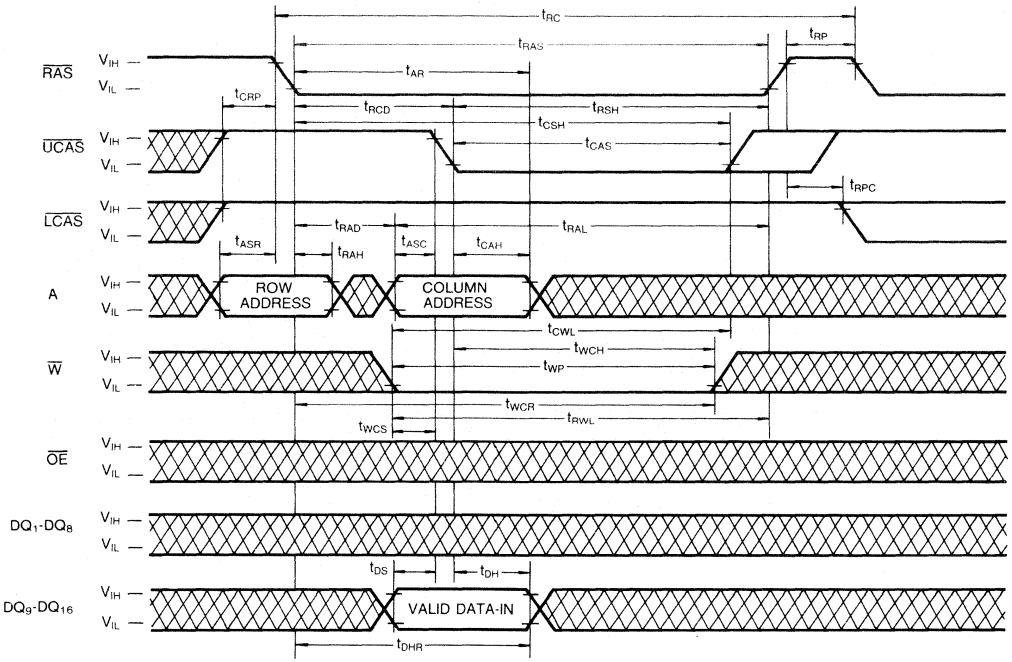


LOWER BYTE WRITE CYCLE (EARLY WRITE)

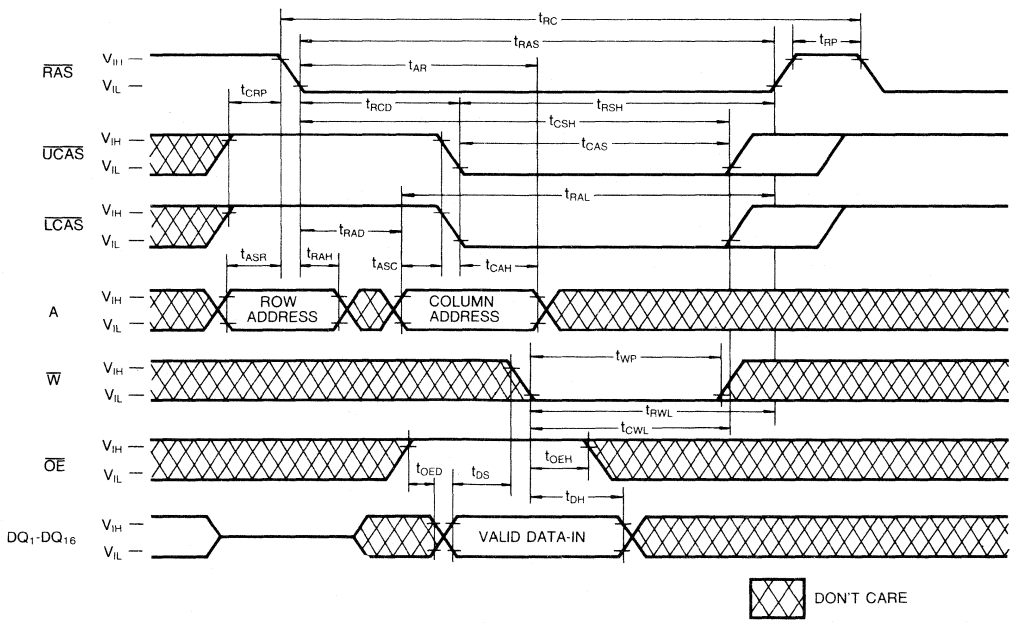


TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)

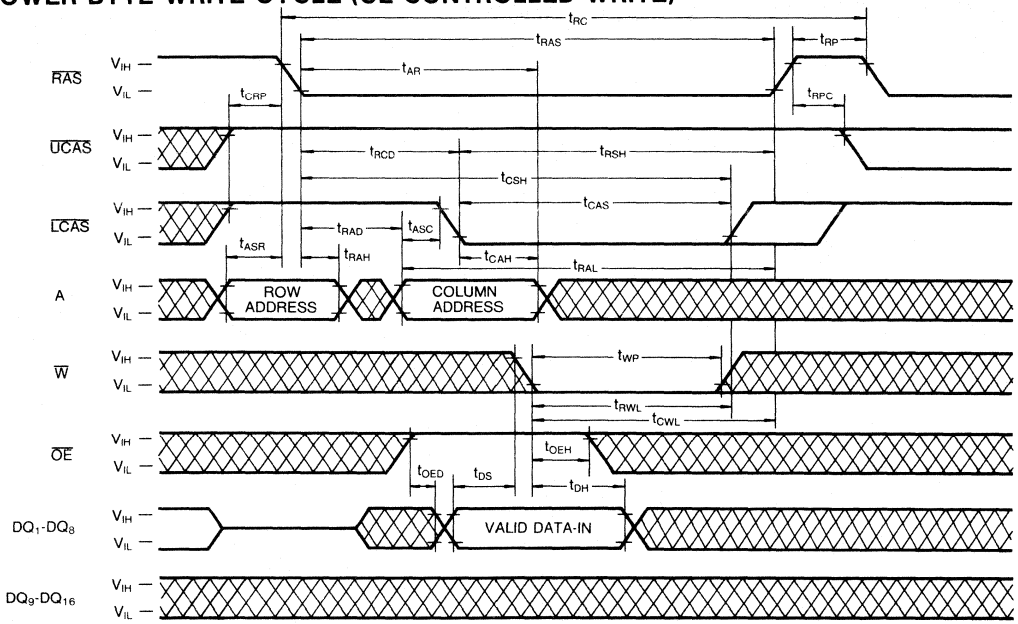


WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

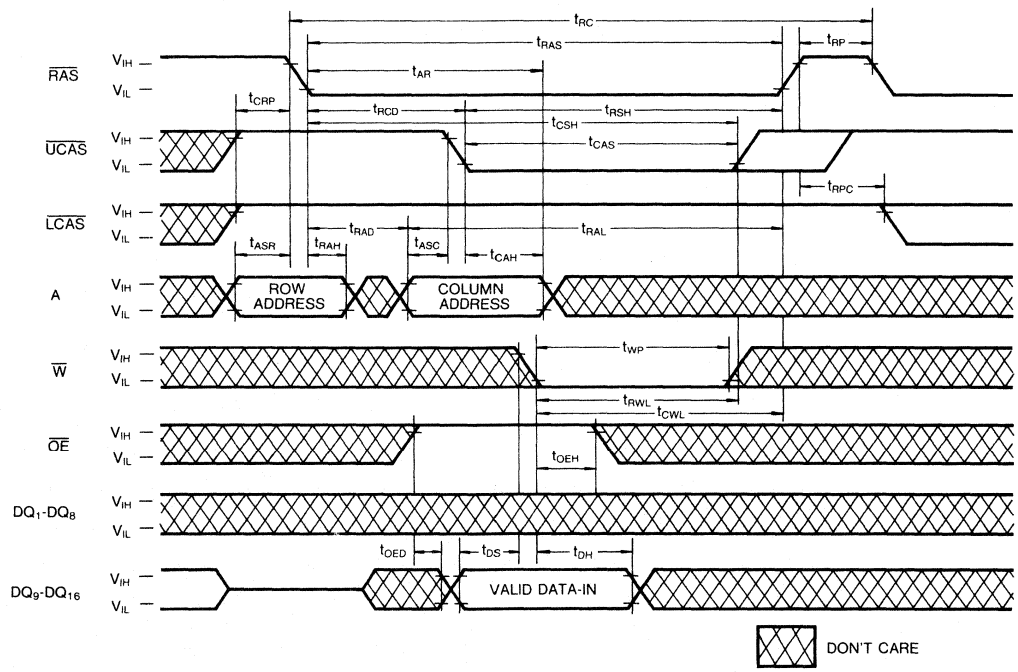


TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

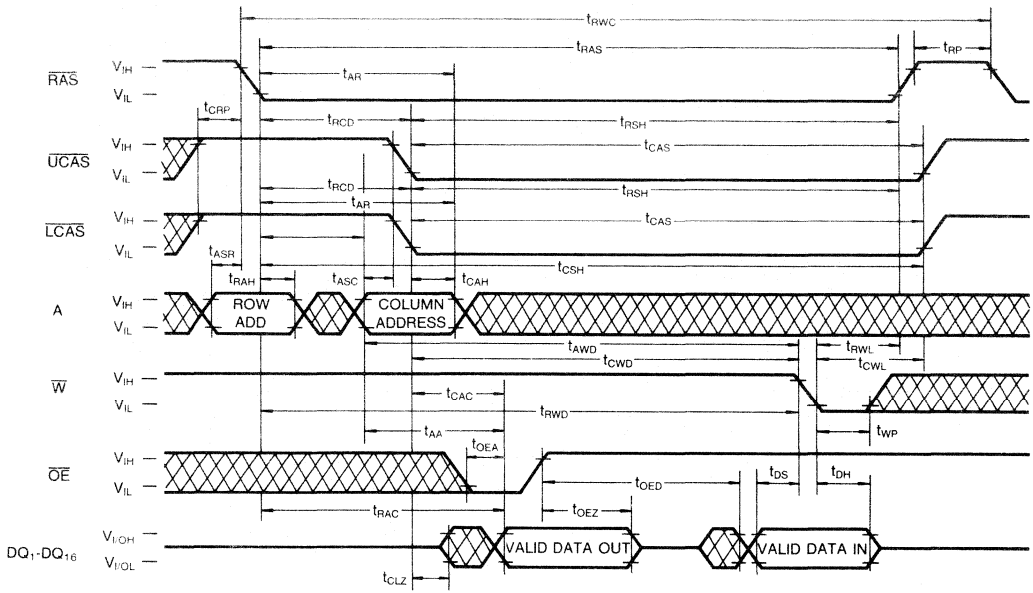


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

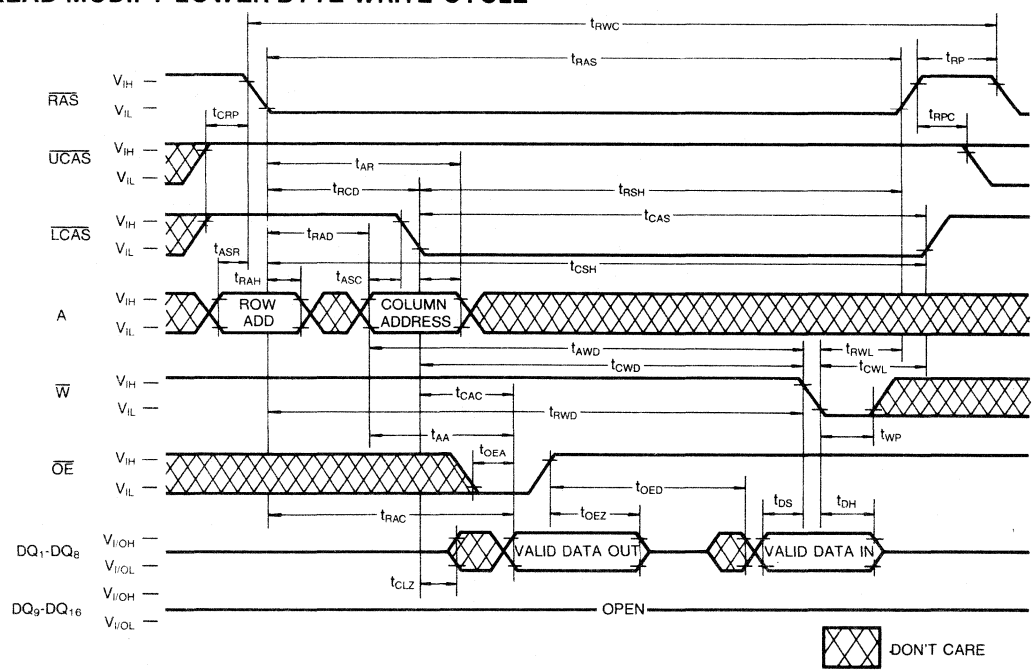


TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE

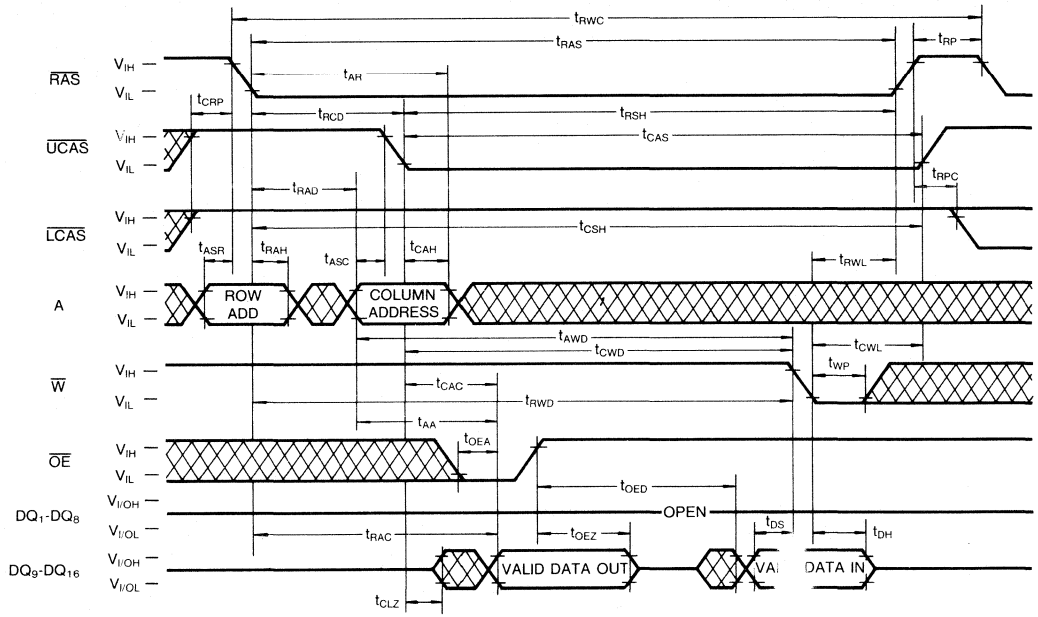


READ-MODIFY-LOWER-BYTE-WRITE CYCLE

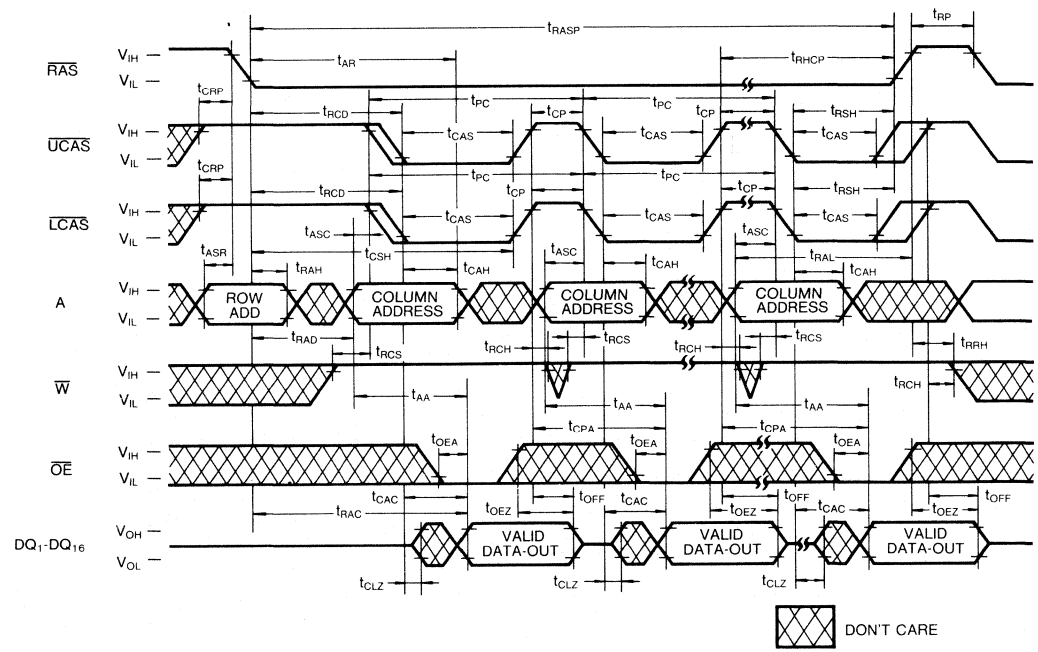


TIMING DIAGRAMS (Continued)

READ-MODIFY-UPPER-BYTE-WRITE CYCLE

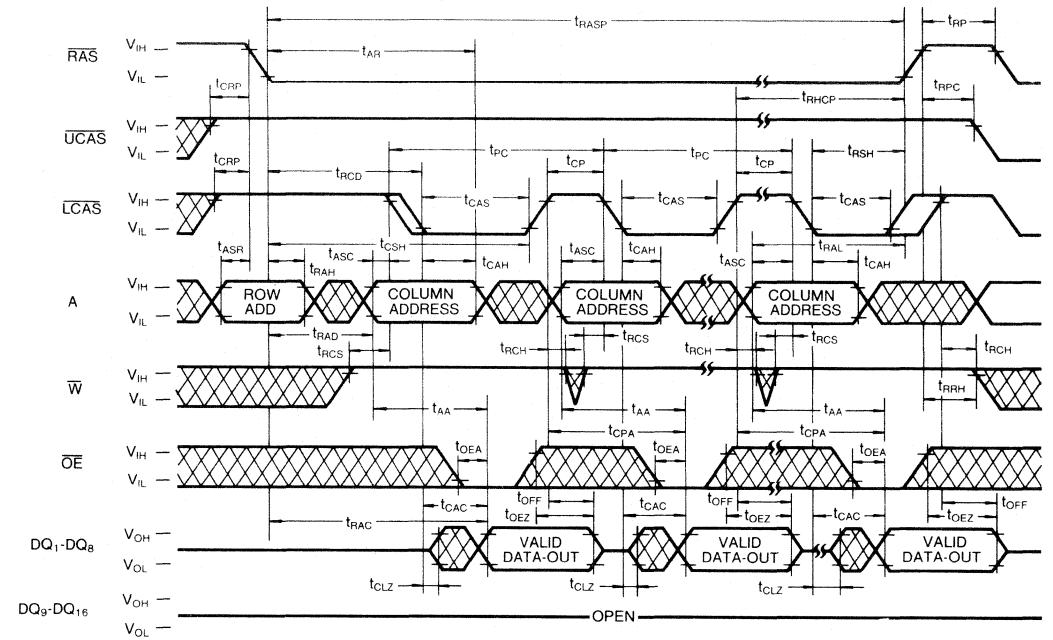


FAST PAGE MODE WORD READ CYCLE

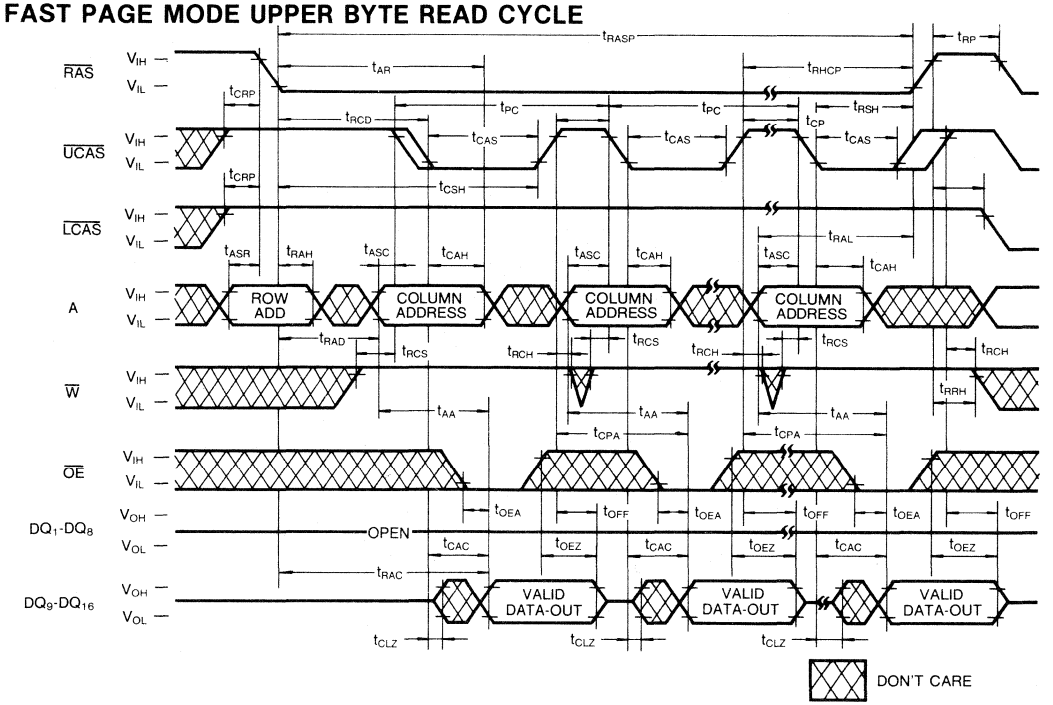


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE

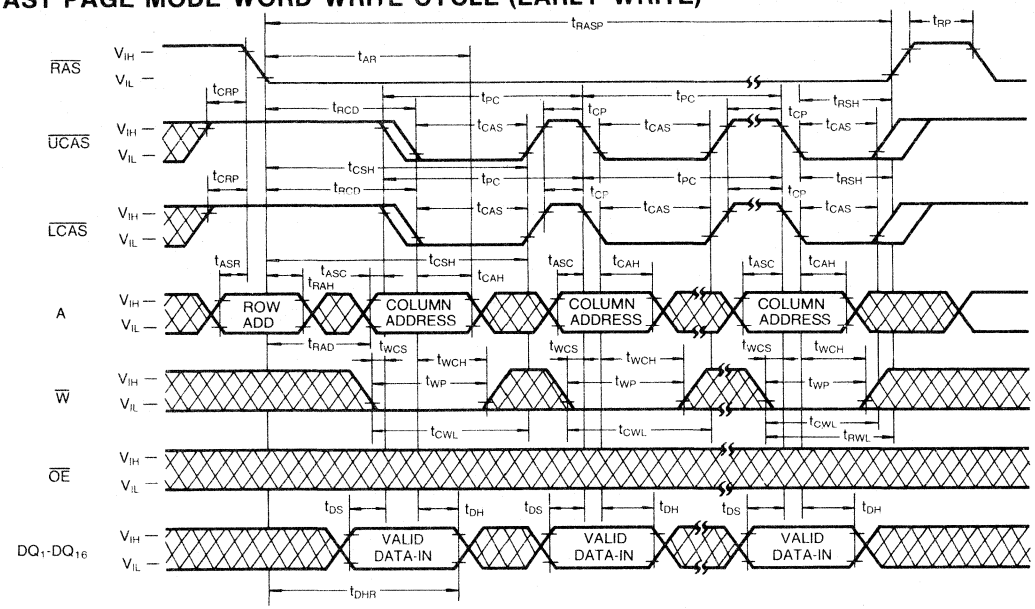


FAST PAGE MODE UPPER BYTE READ CYCLE

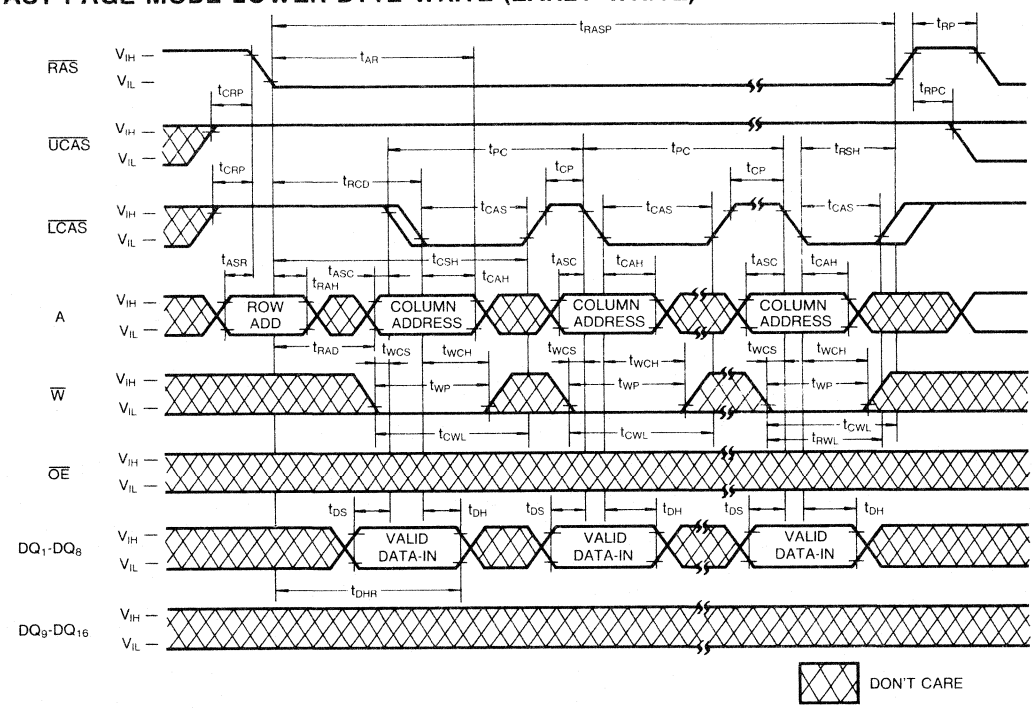


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

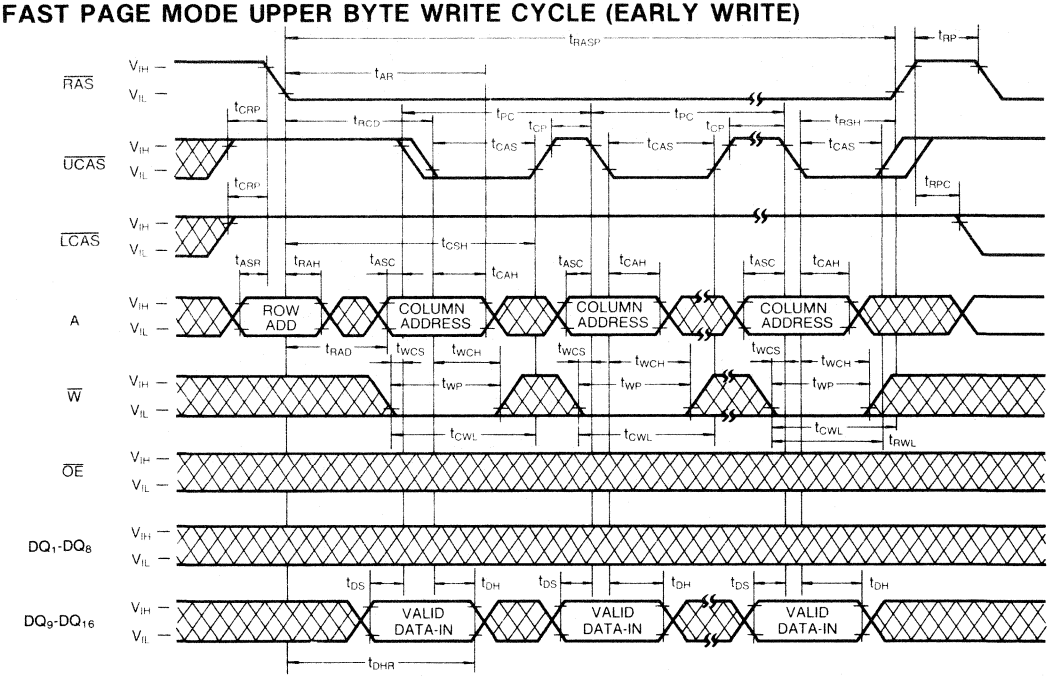


FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)

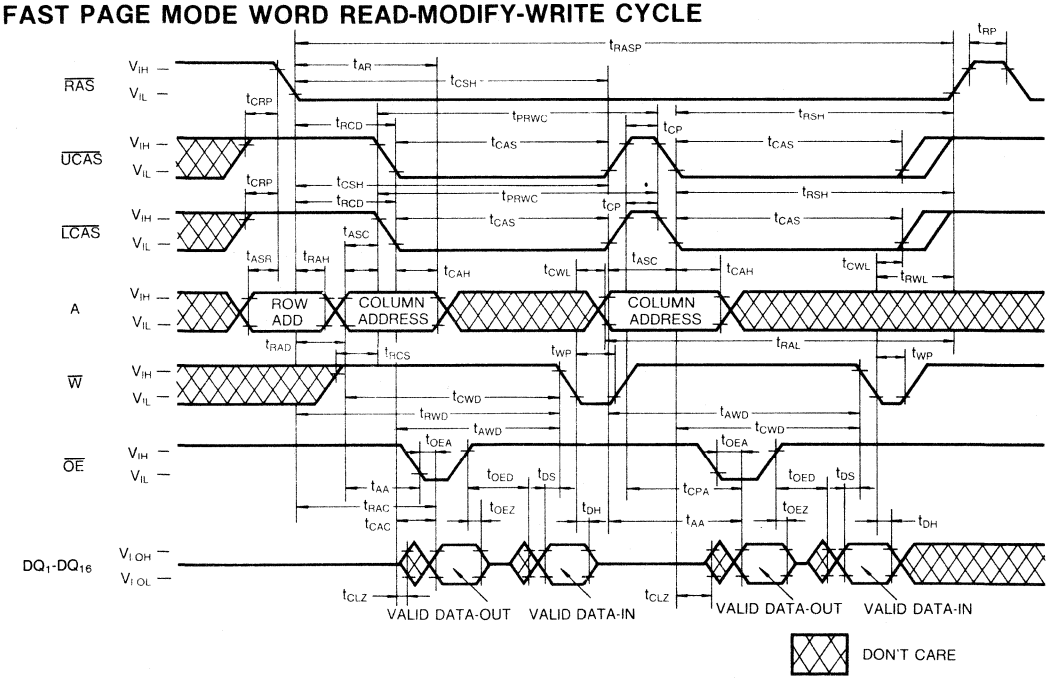


TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

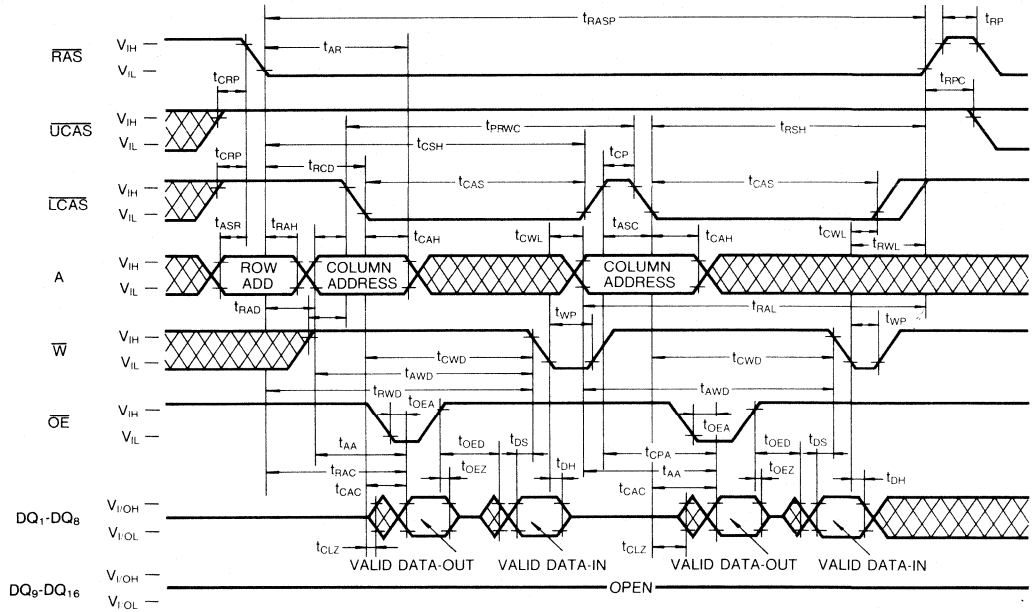


FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE

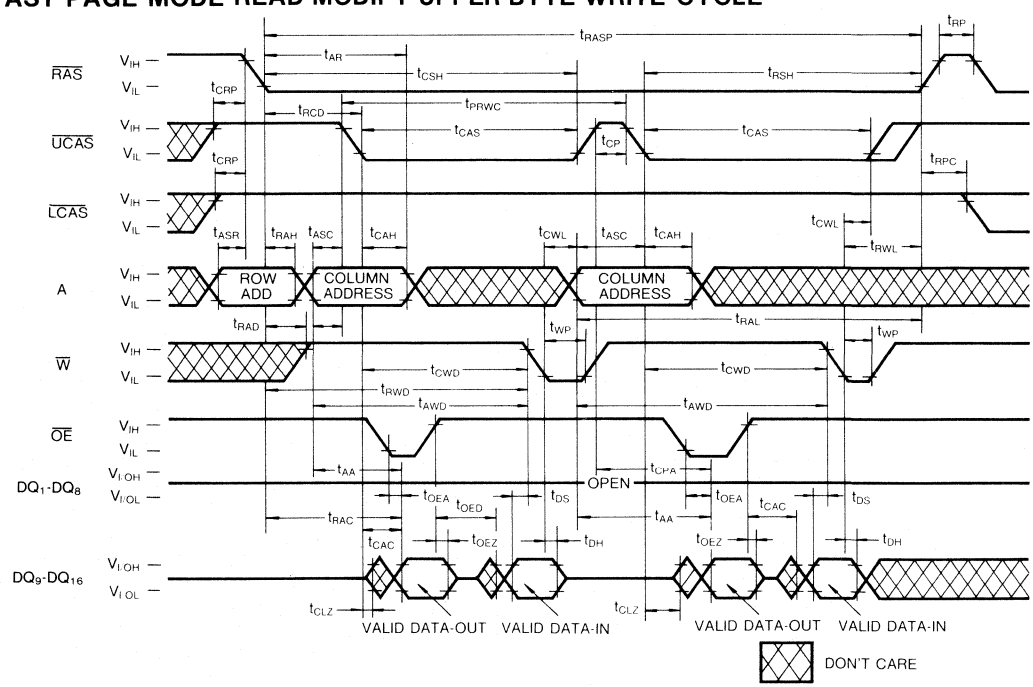


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE



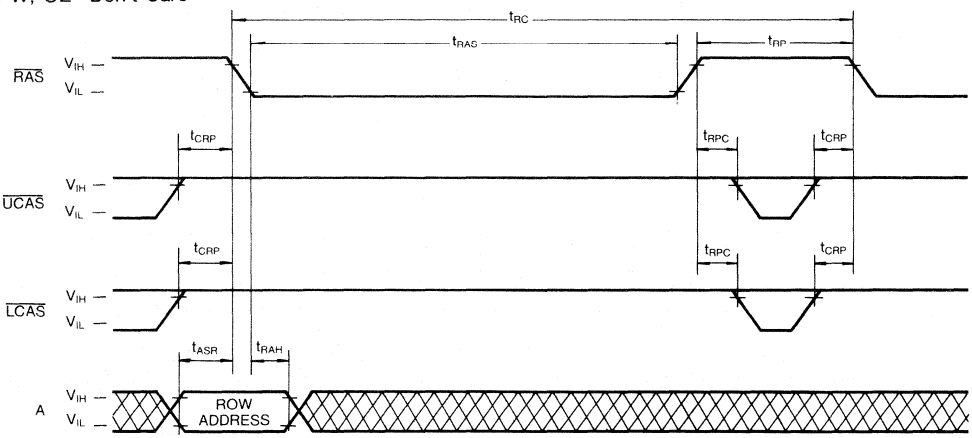
FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



TIMING DIAGRAMS (Continued)

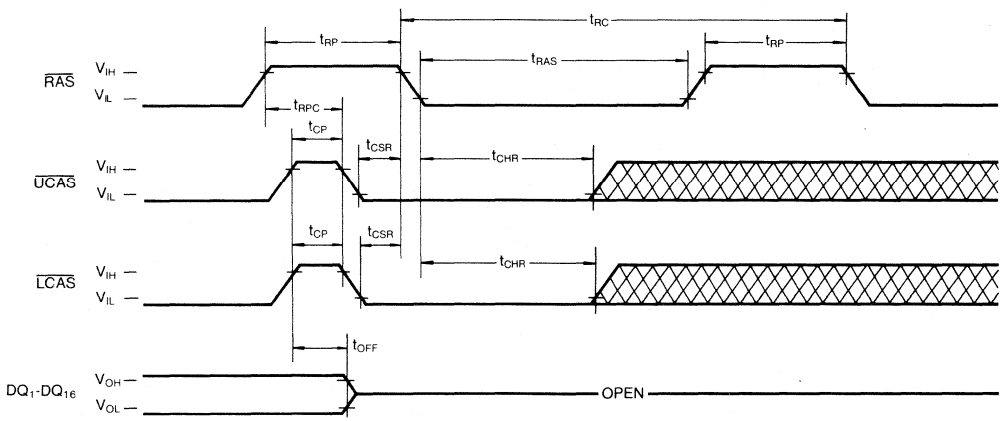
$\overline{RAS}$ ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$=Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

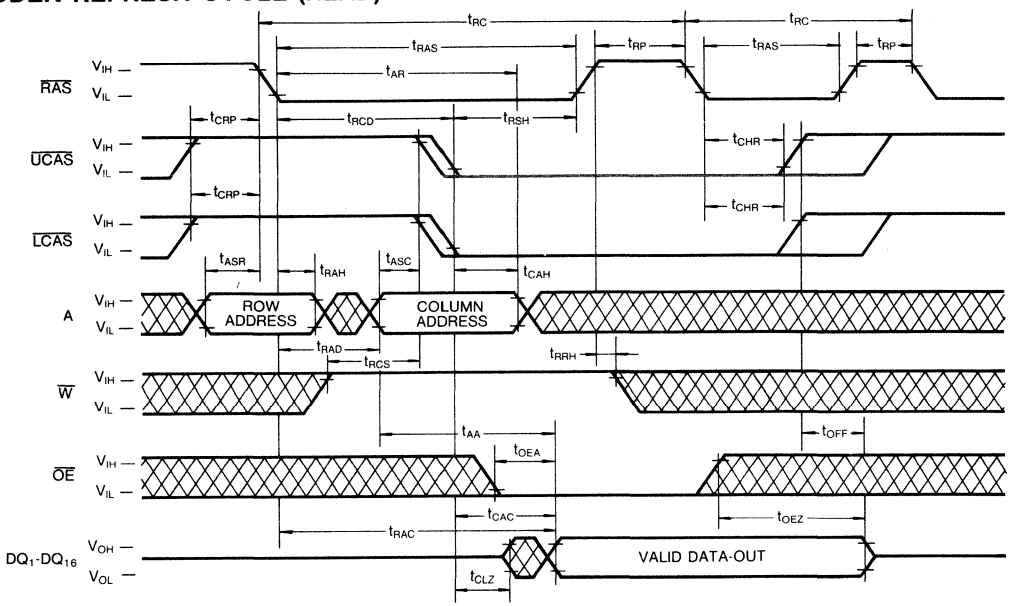
NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



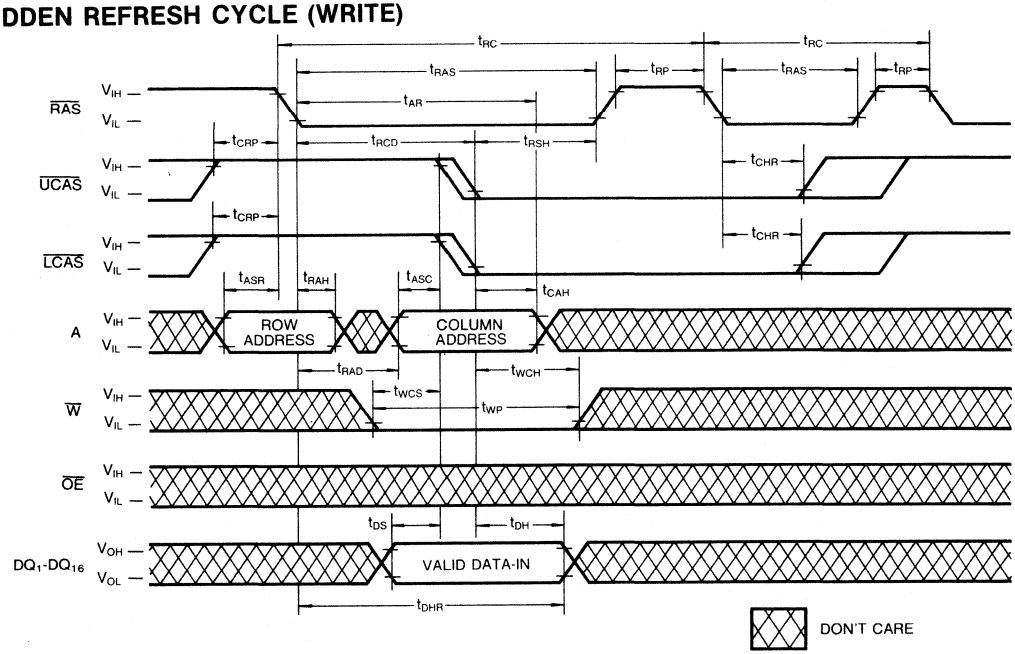
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

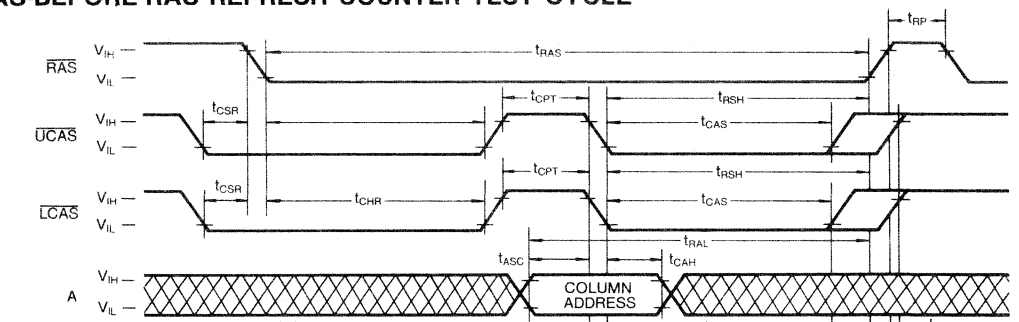


HIDDEN REFRESH CYCLE (WRITE)

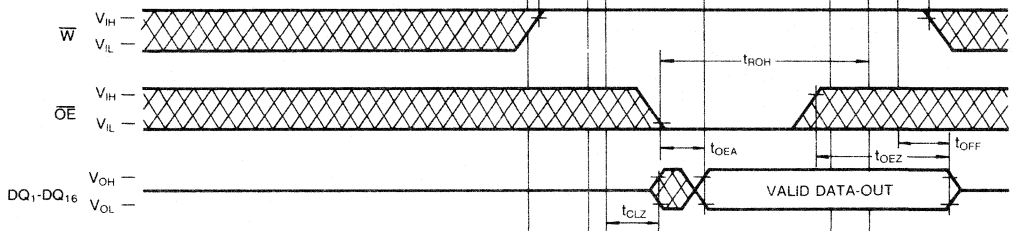


TIMING DIAGRAMS (Continued)

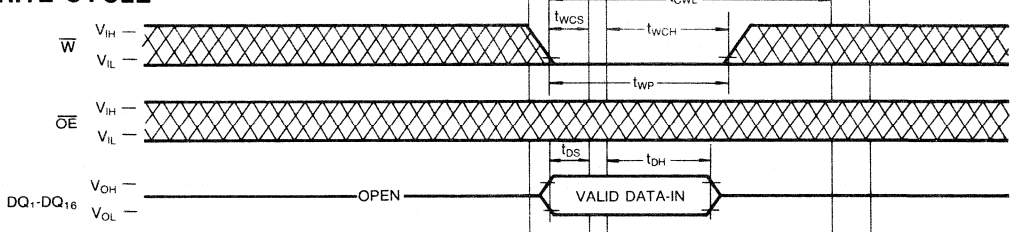
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



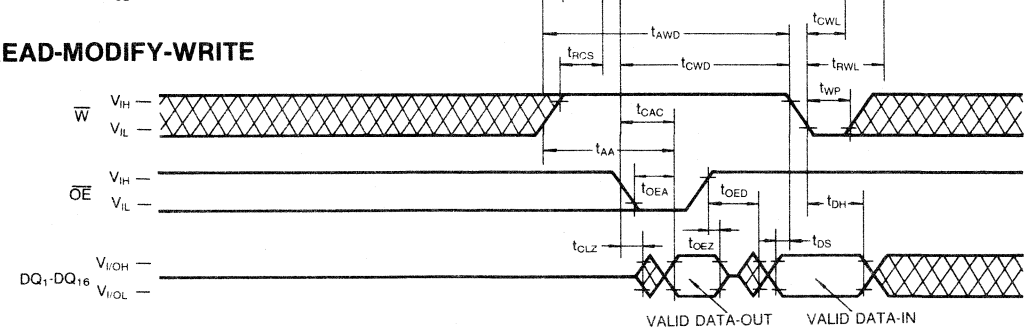
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE



DEVICE OPERATION

Device Operation

The KM416C1000 contains 16,777,216 memory locations arranged in 16 groups of 1,048,576 x 1 bit each. Twenty address bits are required to address a particular memory location. Since the KM416C1000 has only 12 address input pins, time multiplexed addressing is used to input 12 row and 8 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{LCAS}$, $\overline{UCAS}$) and the valid row and column address inputs.

Operation of the KM416C1000 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{LCAS}$ ($\overline{UCAS}$) remains high. Then the address on the 12 address input pins is changed from a row address to a column address and is strobed in by $\overline{LCAS}$ ($\overline{UCAS}$). This is the beginning of any KM416C1000 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{LCAS}$ ($\overline{UCAS}$) have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM416C1000 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/x$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. Additionally the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If x$\overline{CAS}$ transitions to a low before t_{RCD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if x$\overline{CAS}$ transitions low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM416C1000 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$, $\overline{LCAS}$ and $\overline{UCAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or x$\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before x$\overline{CAS}$. The 16 Bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cells appears at the output before and during the time that data is being written into the same cells. This cycle is achieved by bringin $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The $\overline{OE}$ input must be low during the time defined by t_{OEA} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM416C1000 DQ pins.

Data Output

The KM416C1000 has a three-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}), the outputs are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs enter into the low impedance state in the time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM416C1000 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} times are not met)

Refresh

The data in the KM416C1000 is stored as a charge on microscopic capacitor within each memory cell. The stored charge tends to dissipate over time and will af-

DEVICE OPERATION (Continued)

fect data integrity if the charge is not periodically refreshed. Refresh of the individual storage cells is accomplished by accessing all rows within the refresh period (t_{REF}) of within 64ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 4096 row address (A0-A11).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM416C1000 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If either $\overline{LCAS}$ or $\overline{UCAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ transitions low, the onchip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending either $\overline{LCAS}$ or $\overline{UCAS}$ input active time and cycling $\overline{RAS}$. The hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM416C1000 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM416C1000 has Fast page mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter test cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is asserted high and then low again while $\overline{RAS}$ is asserted low, the read and write operations are enabled. In this method, the row address bits A0 through A11 are supplied by on chip refresh counter.

Power-Up

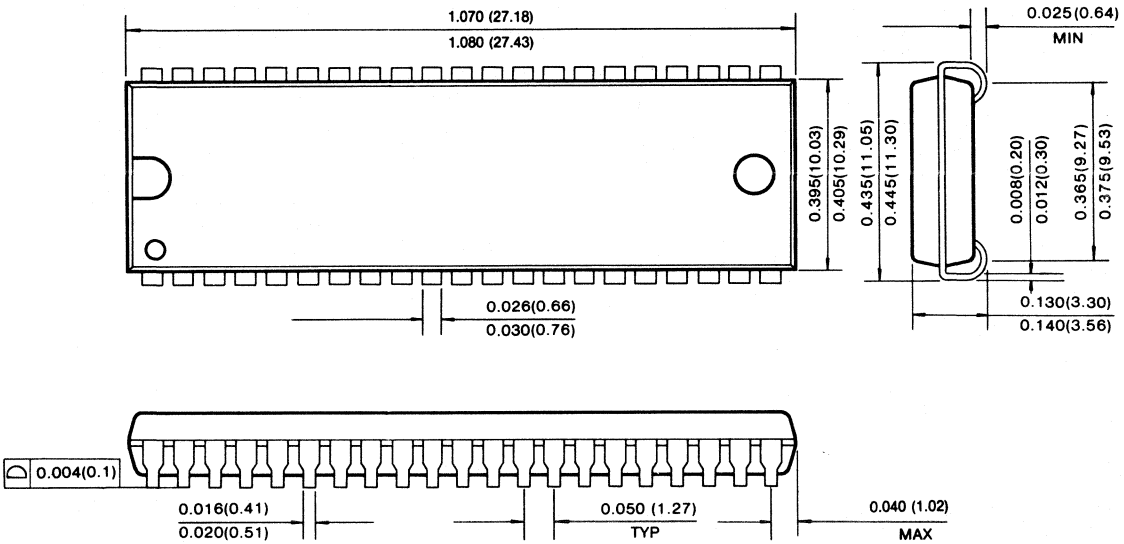
If $\overline{RAS} = V_{SS}$ during power-up, the KM416C1000 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held a valid V_{IH} in order to minimize power-up current.

An initial pause of 200μs is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8ms period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

PACKAGE DIMENSION

42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



1M x 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM416C1200-7	70ns	20ns	130ns
KM416C1200-8	80ns	20ns	150ns
KM416C1200-10	100ns	25ns	180ns

- **Fast Page Mode operation**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early Write or output enable controlled write**
- **Triple +5V ± 10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC Standard pinout**
- **Available in Plastic SOJ**

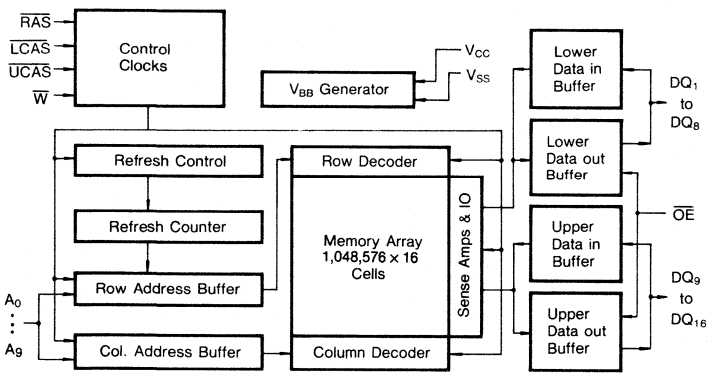
GENERAL DESCRIPTION

The Samsung KM416C1200 is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM416C1200 features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

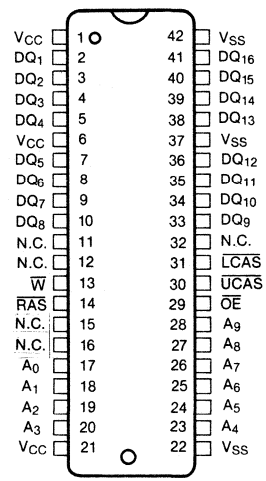
The KM416C1200 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)

- **KM416C1200J**



Pin Name	Pin Function
A_0-A_9	Address Inputs
DQ_{1-16}	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe

Pin Name	Pin Function
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power (+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	700	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC}+1	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$, or $\overline{LCAS}$, Address Cycling @t_{RC} = min.)	KM416C1200-7	I_{CC1}	—	160	mA
	KM416C1200-8		—	140	mA
	KM416C1200-10		—	120	mA
Standby Current ($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$)		I_{CC2}	—	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$ = $\overline{LCAS}$, $\overline{RAS}$, Address Cycling @t_{RC} = min.)	KM416C1200-7	I_{CC3}	—	160	mA
	KM416C1200-8		—	140	mA
	KM416C1200-10		—	120	mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{PC} = min.)	KM416C1200-7	I_{CC4}	—	140	mA
	KM416C1200-8		—	120	mA
	KM416C1200-10		—	100	mA
Standby Current ($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ ≥ V_{CC} − 0.2V)		I_{CC5}	—	1	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @t_{RC} = min.)	KM416C1200-7	I_{CC6}	—	160	mA
	KM416C1200-8		—	140	mA
	KM416C1200-10		—	120	mA
Standby Current ($\overline{RAS}$ = V_{IH}, $\overline{UCAS}$ or $\overline{LCAS}$ = V_{IL} D_{OUT} = Enable)		I_{CC7}	—	5	mA
Input Leakage Current (Any input 0 ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)		I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	μA
Output High Voltage Level (I_{OH} = −5mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL} = 4.2mA)		V_{OL}	—	0.4	V

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}$ = V_{IL}. In I_{CC4}, Address can be changed maximum once while $\overline{UCAS}$ and $\overline{UCAS}$ = V_{IH}.

CAPACITANCE (T_A=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ_1-DQ_{16})	C_{DQ}	—	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	KM416C1200-7		KM416C1200-8		KM416C1200-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	185		205		245		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	3,4,5
Access time from column address	t_{AA}		35		40		50	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	6
Column Address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	6
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	10
Data-in hold time	t_{DH}	15		15		20		ns	10

AC CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC}=5.0V \pm 10\%$, See notes 1,2)

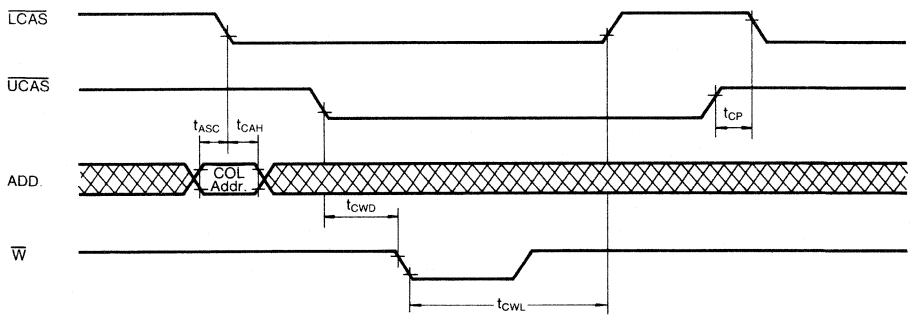
Parameter	Symbol	KM416C1200-7		KM416C1200-8		KM416C1200-10		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	50		50		60		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	100		110		135		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	65		70		85		ns	8
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20		30		30		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	t_{CPT}	35		40		50		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		55	ns	3
Fast page mode cycle time	t_{PC}	45		50		60		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	100		105		125		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	45		45		55		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
$\overline{OE}$ access time	t_{OEA}		20		20		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		20		25		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20		20		25		ns	

KM416C1200 Truth Table

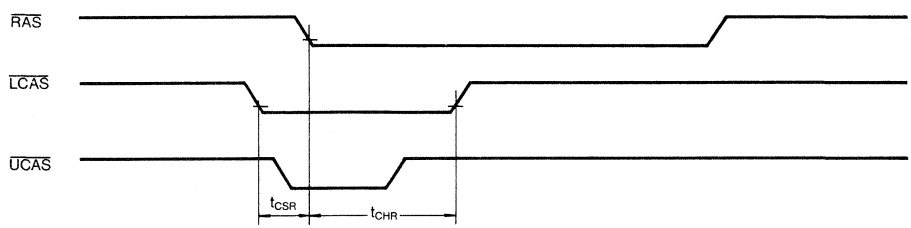
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	$DQ_{1\sim8}$	$DQ_{9\sim16}$	State
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Lower Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-In	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	—

NOTES

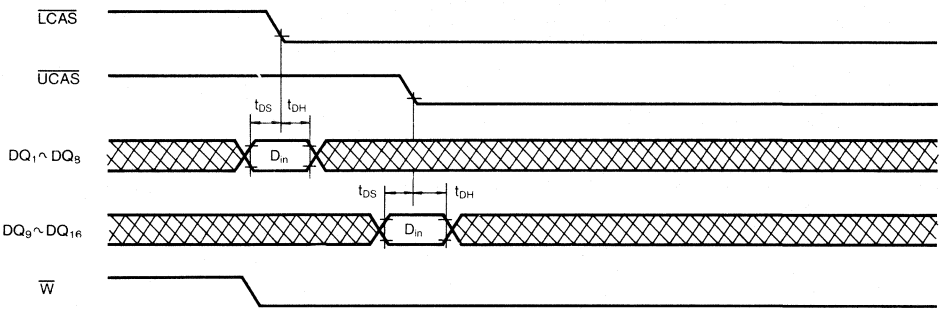
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating aprameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
17. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.

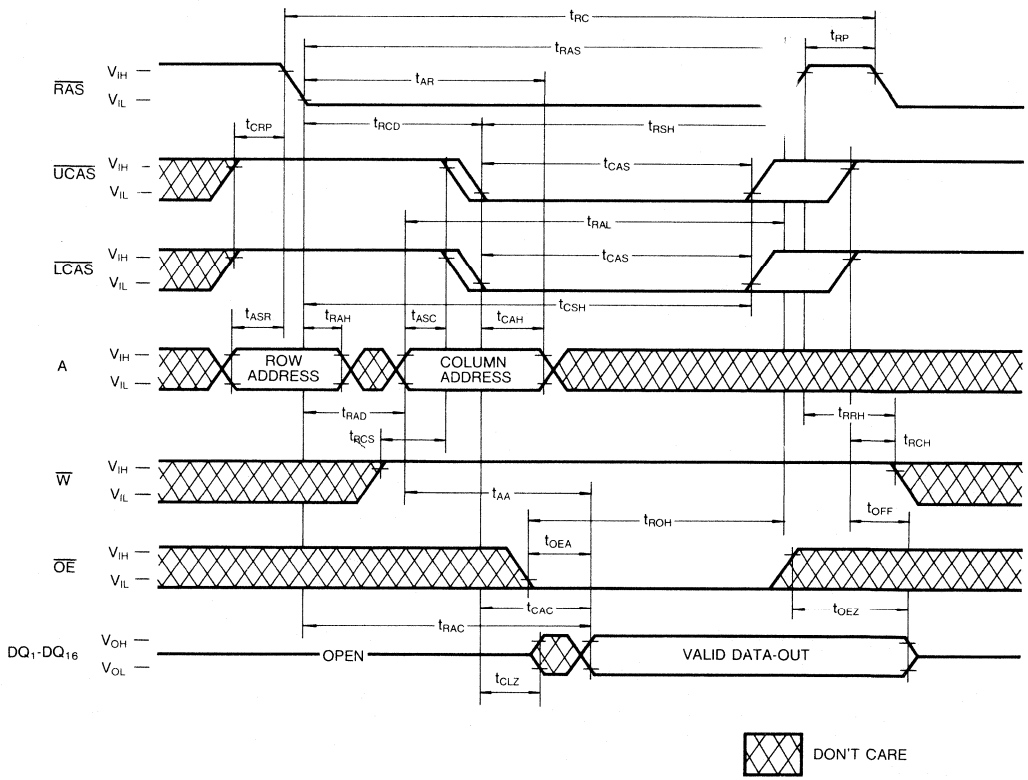


18. t_{DS}, t_{DH} is independetly specified for lower byte $D_{in(1\sim8)}$, upper byte $D_{in(9\sim16)}$



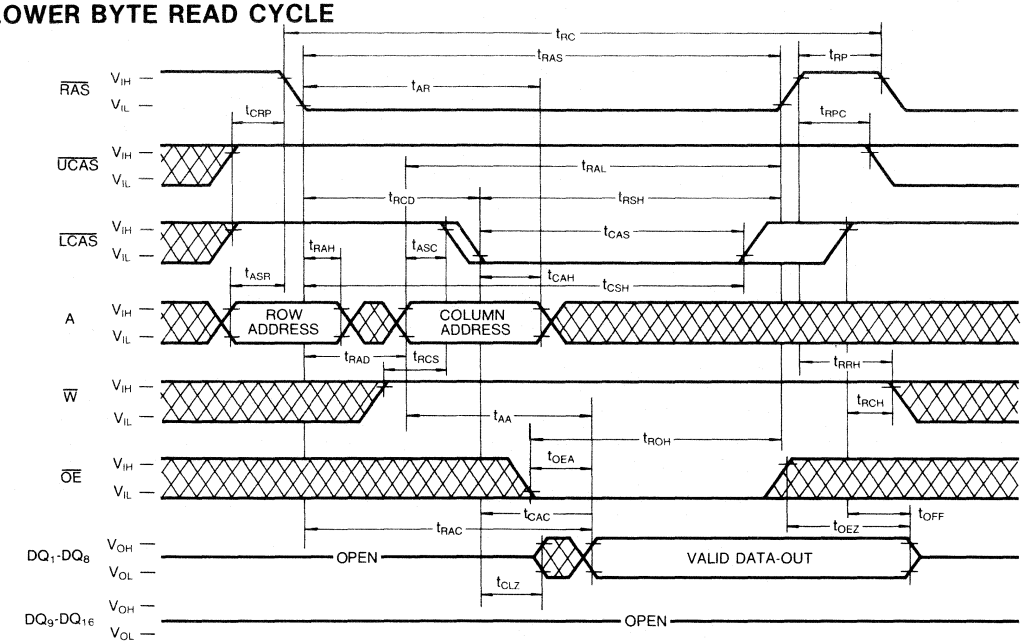
TIMING DIAGRAMS

WORD READ CYCLE

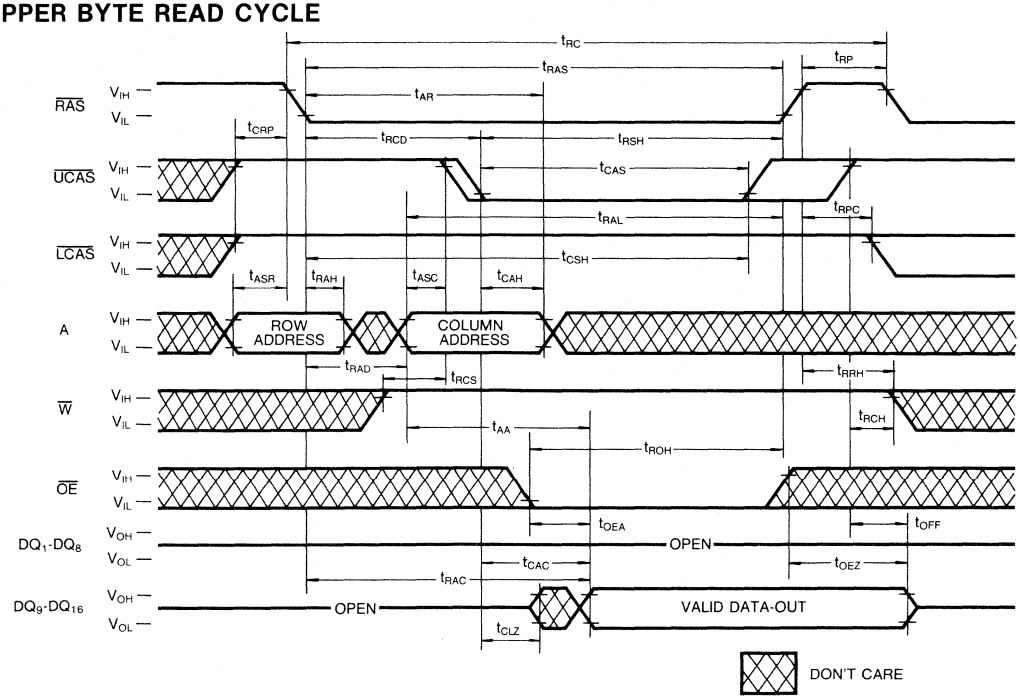


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE

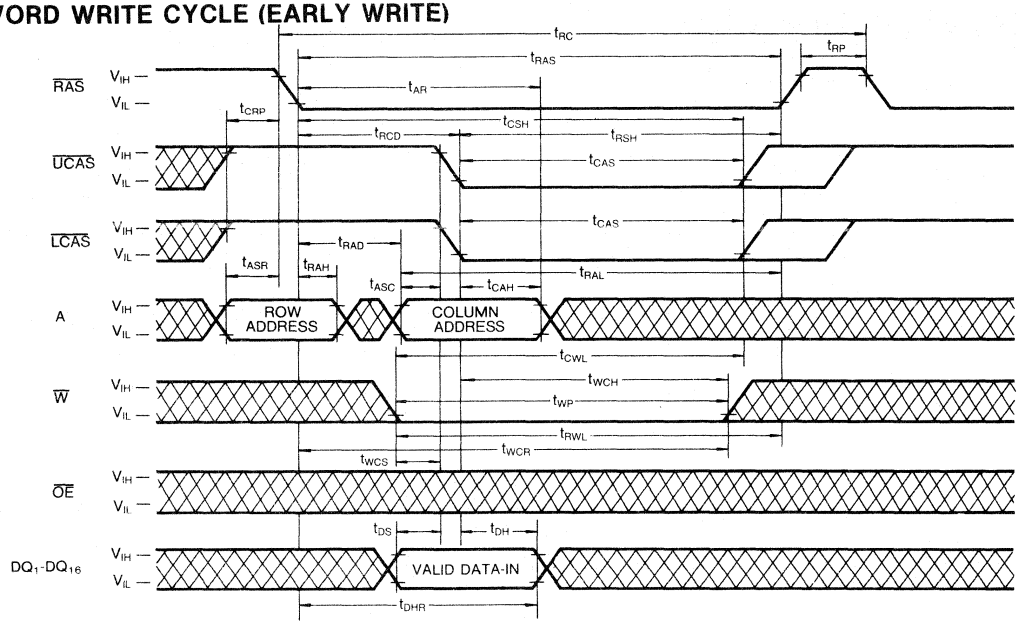


UPPER BYTE READ CYCLE

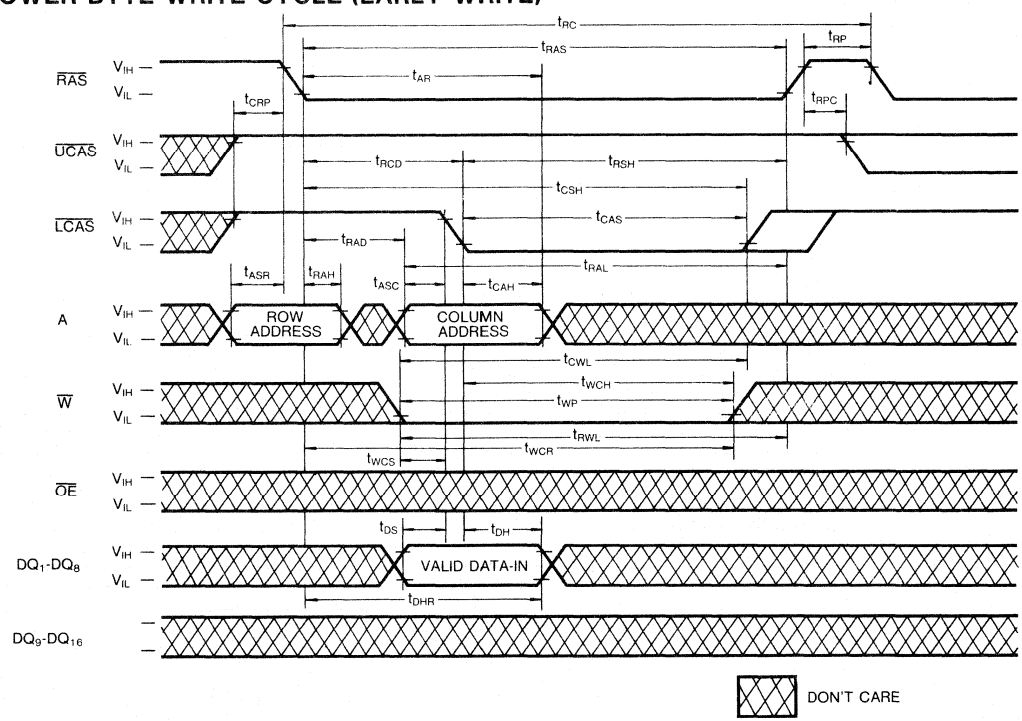


TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)

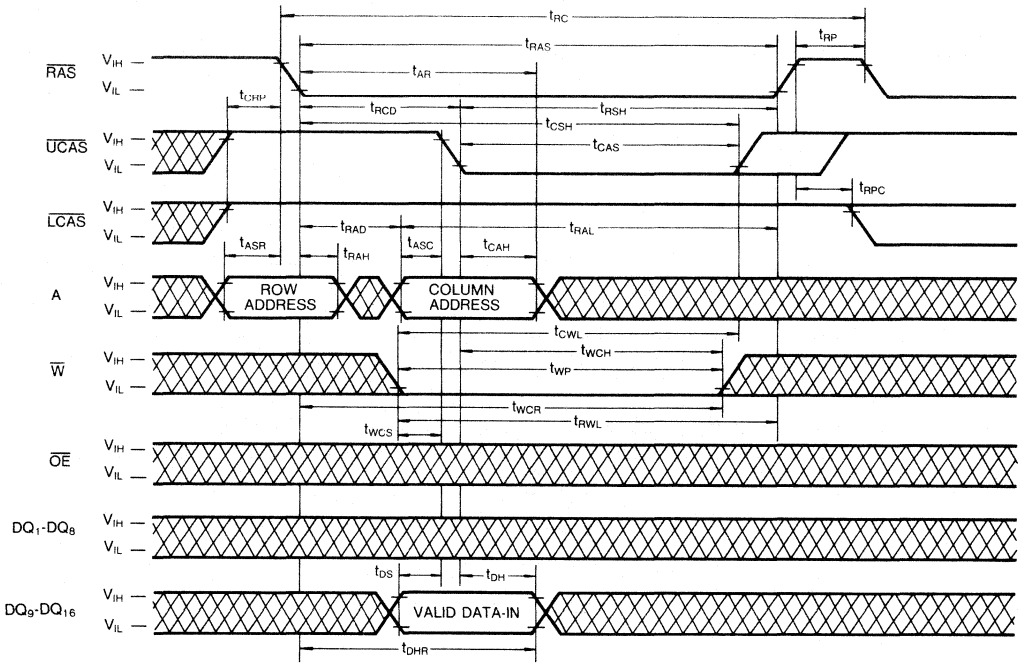


LOWER BYTE WRITE CYCLE (EARLY WRITE)

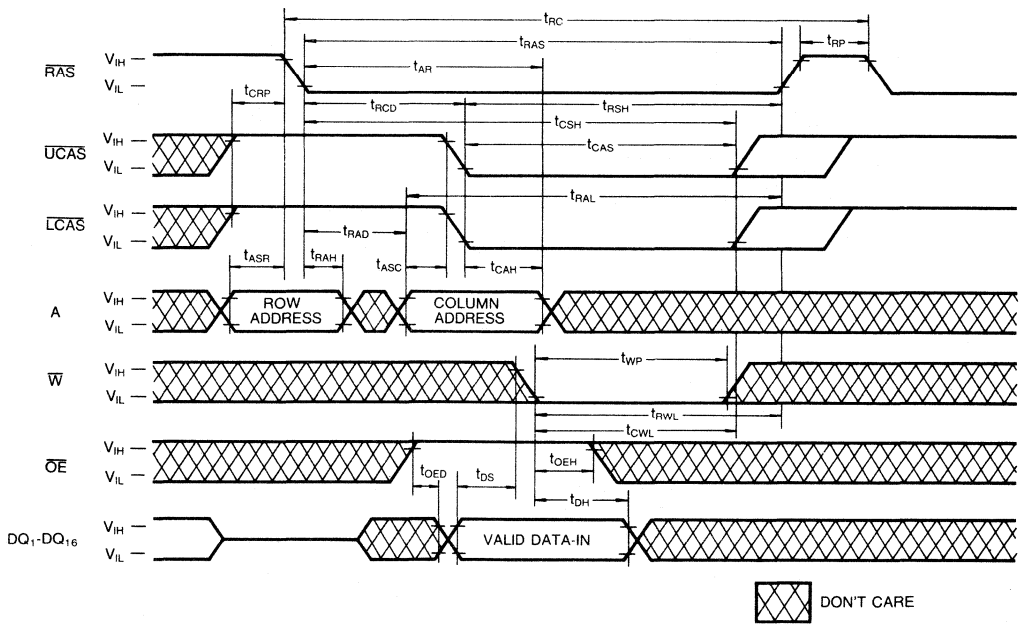


TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)

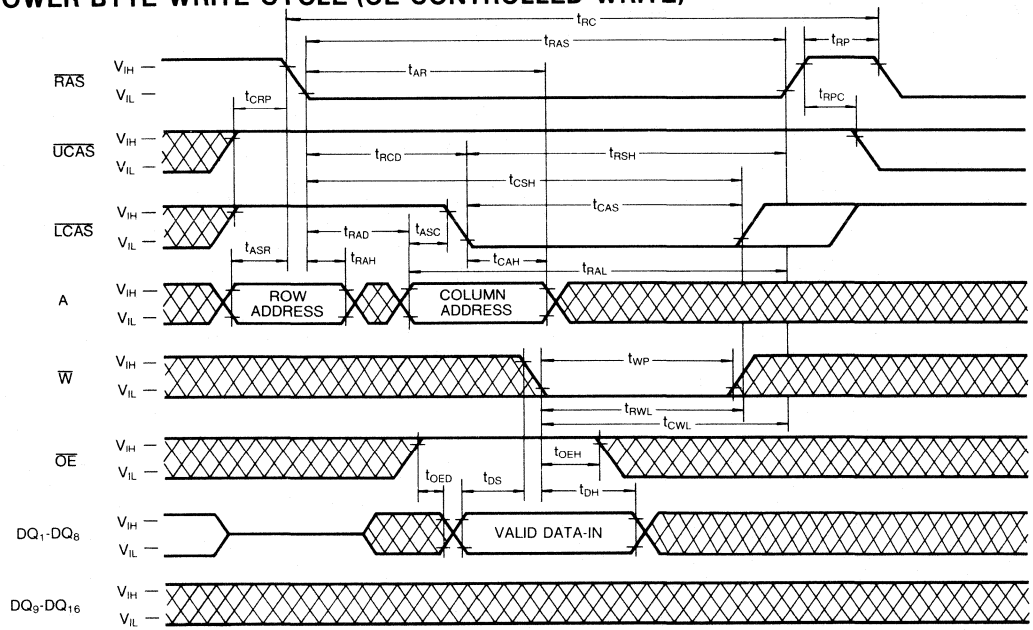


WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

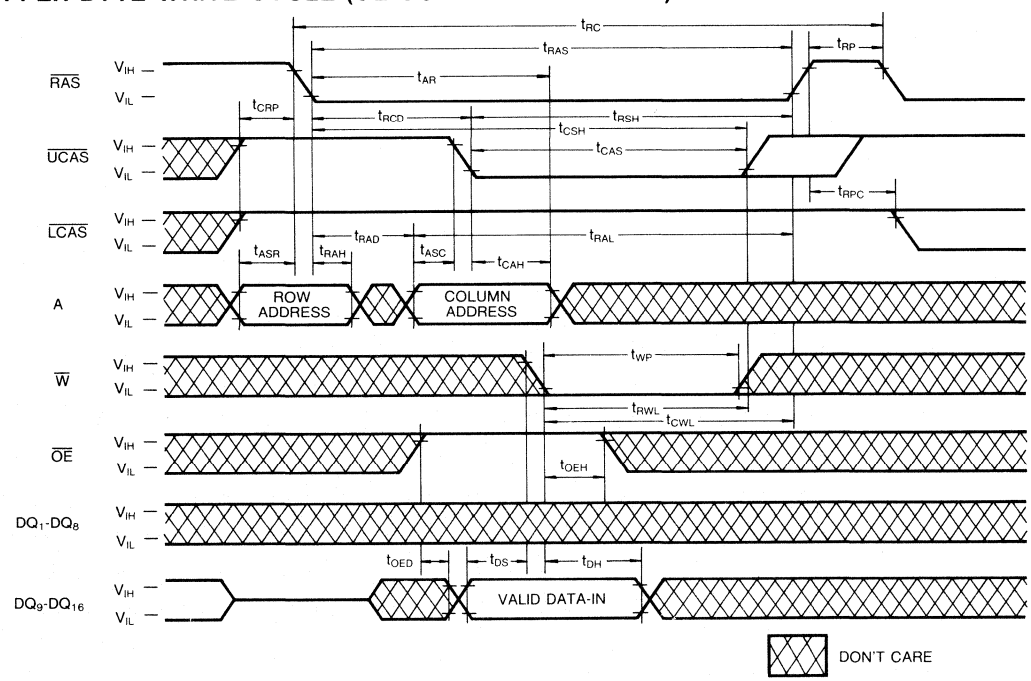


TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

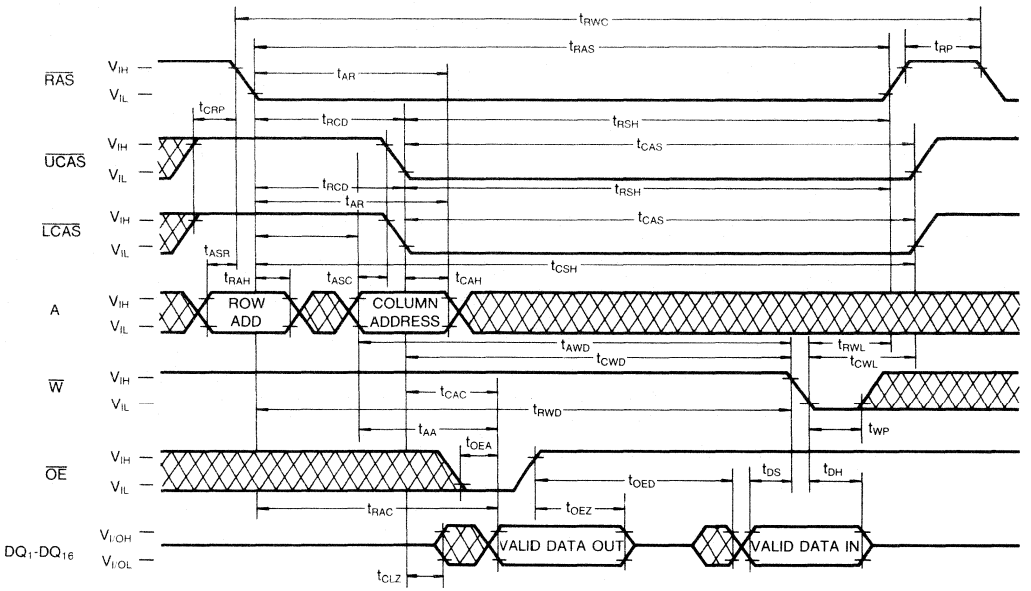


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

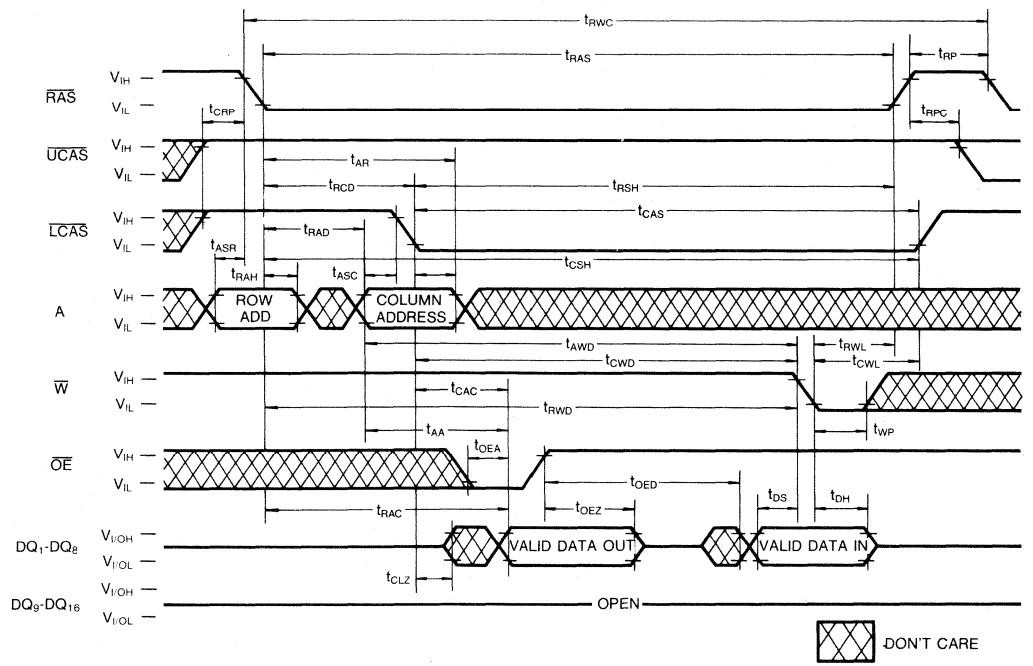


TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE

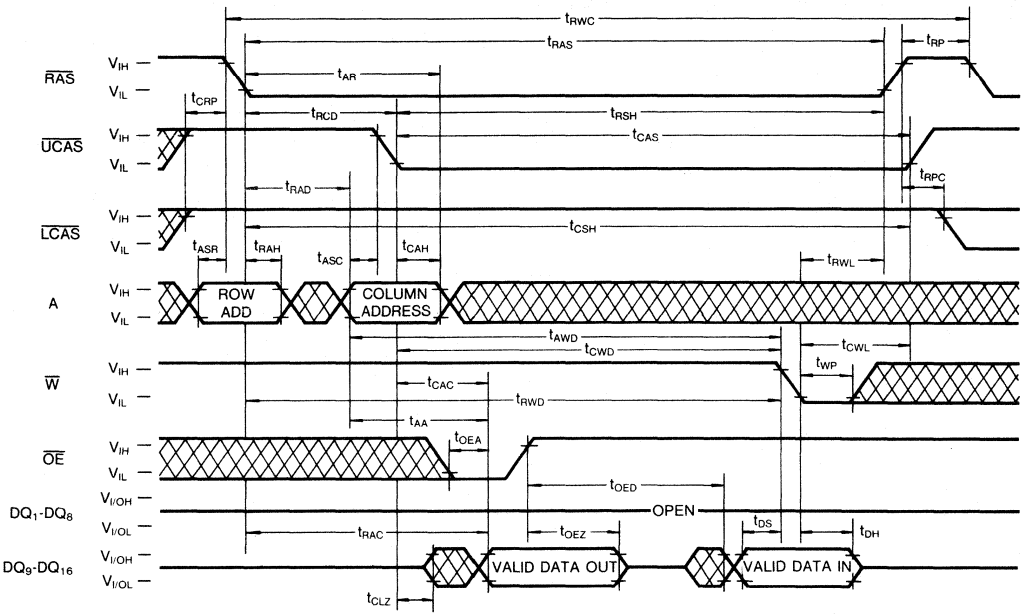


READ-MODIFY-LOWER-BYTE-WRITE CYCLE

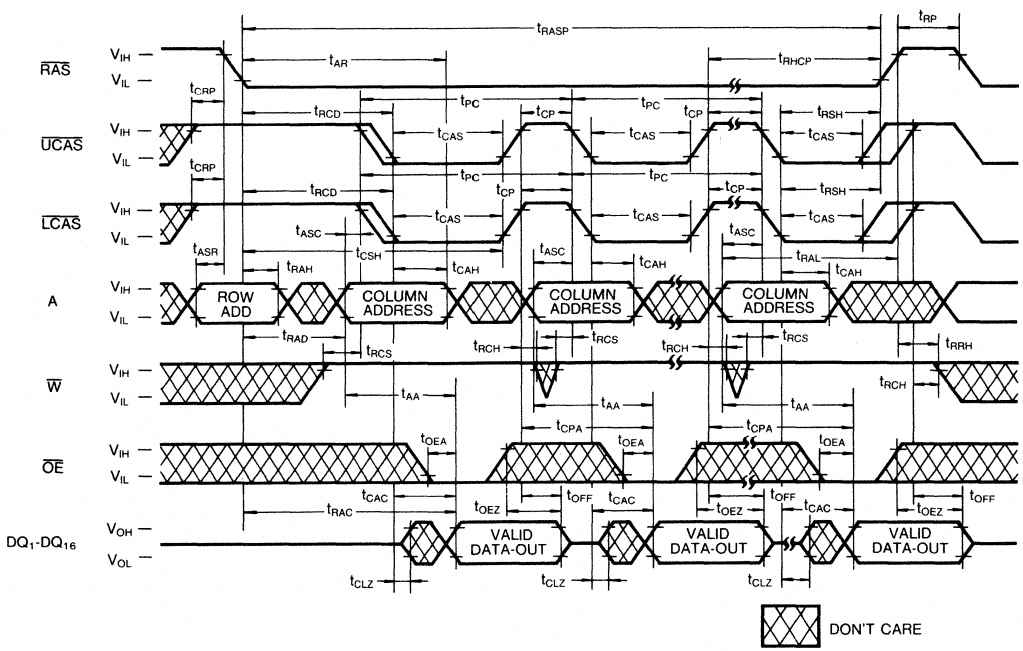


TIMING DIAGRAMS (Continued)

READ-MODIFY-UPPER-BYTE-WRITE CYCLE

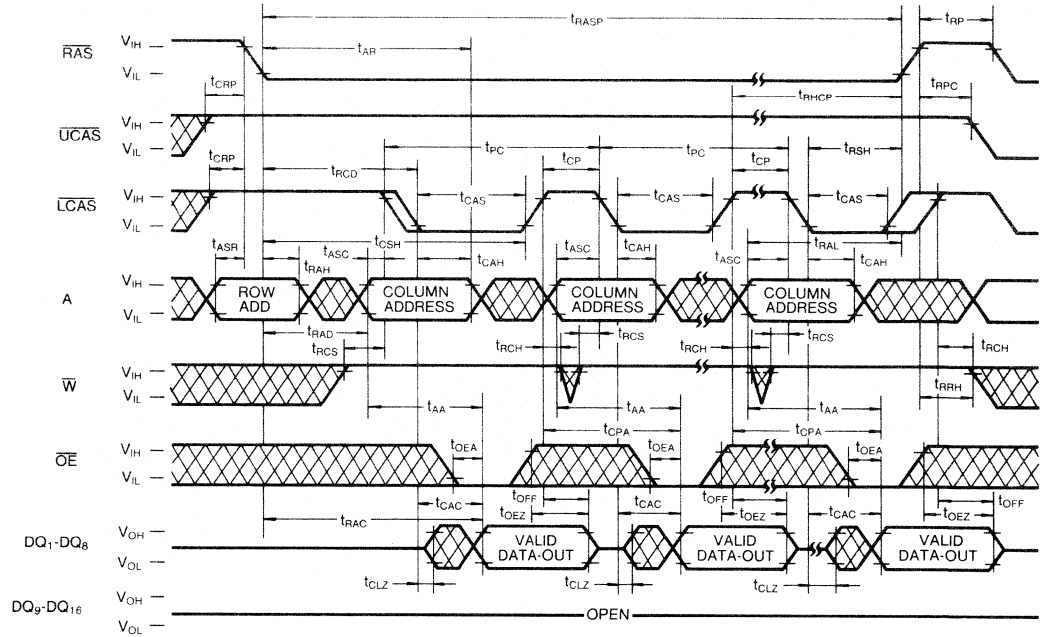


FAST PAGE MODE WORD READ CYCLE

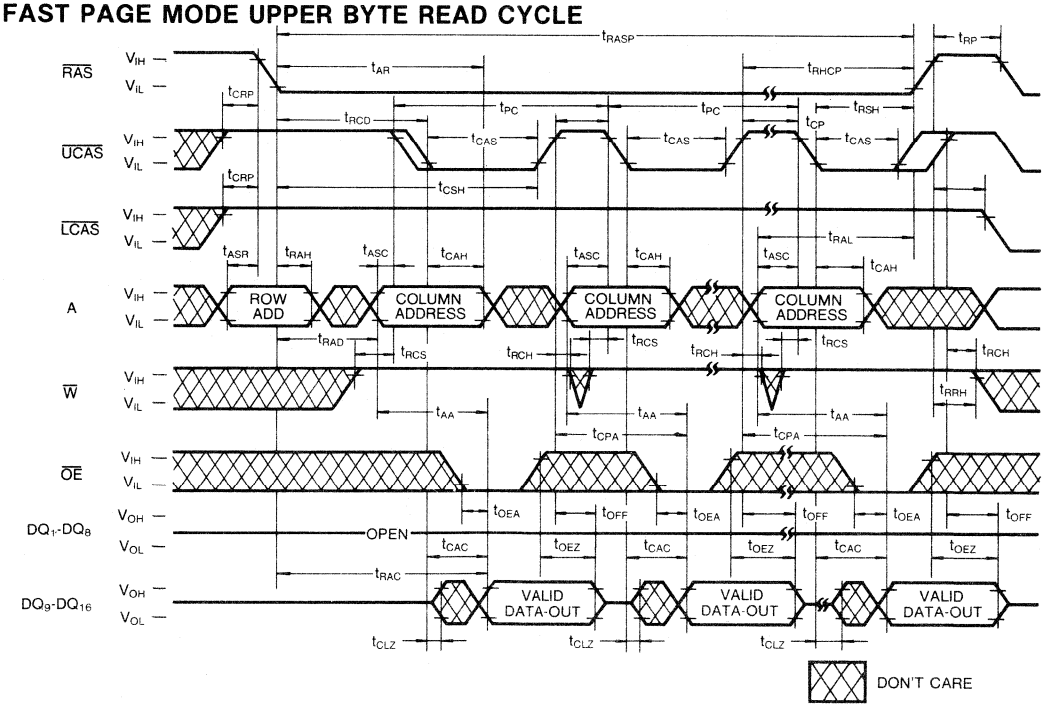


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE

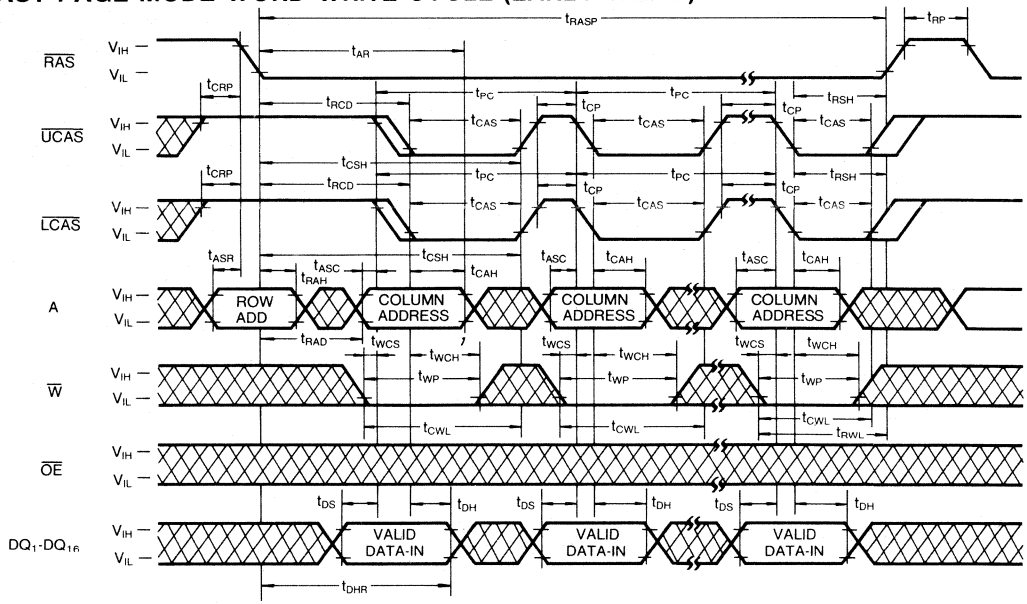


FAST PAGE MODE UPPER BYTE READ CYCLE

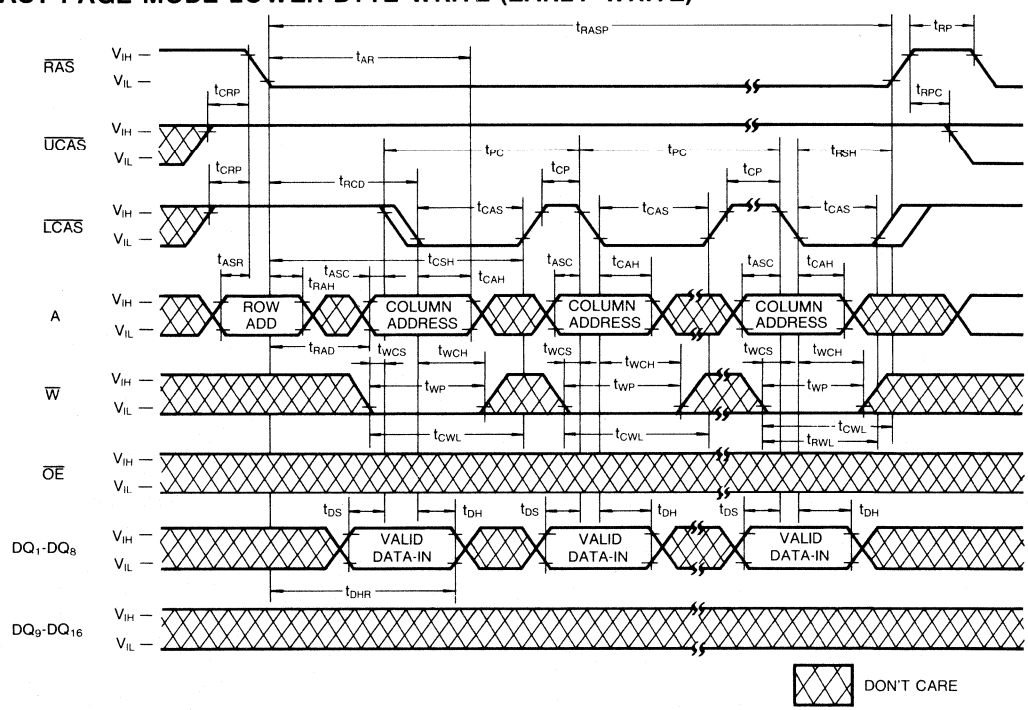


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

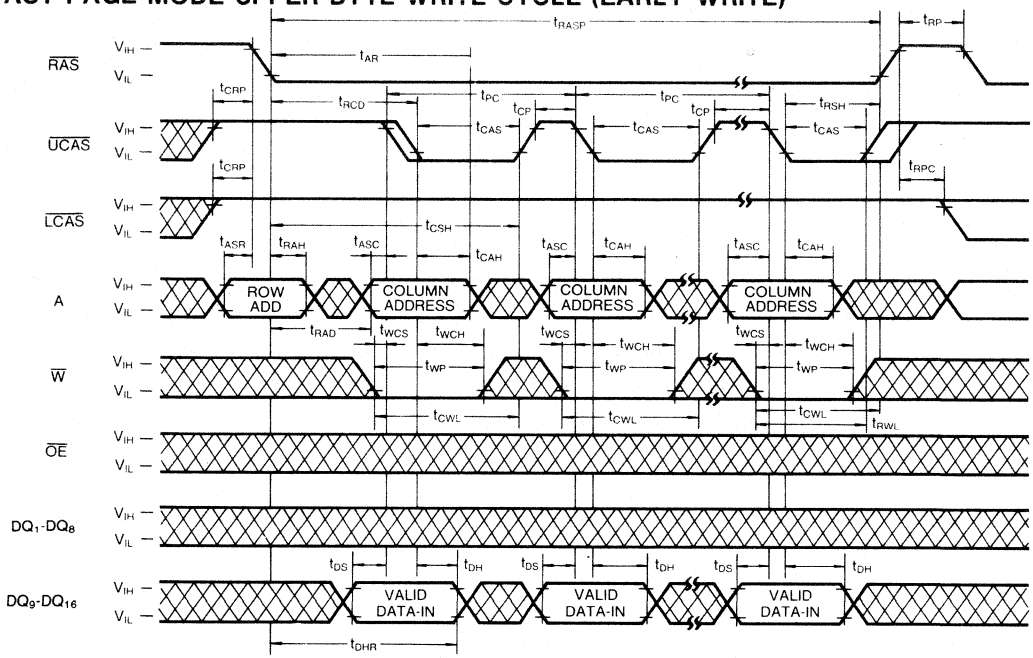


FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)

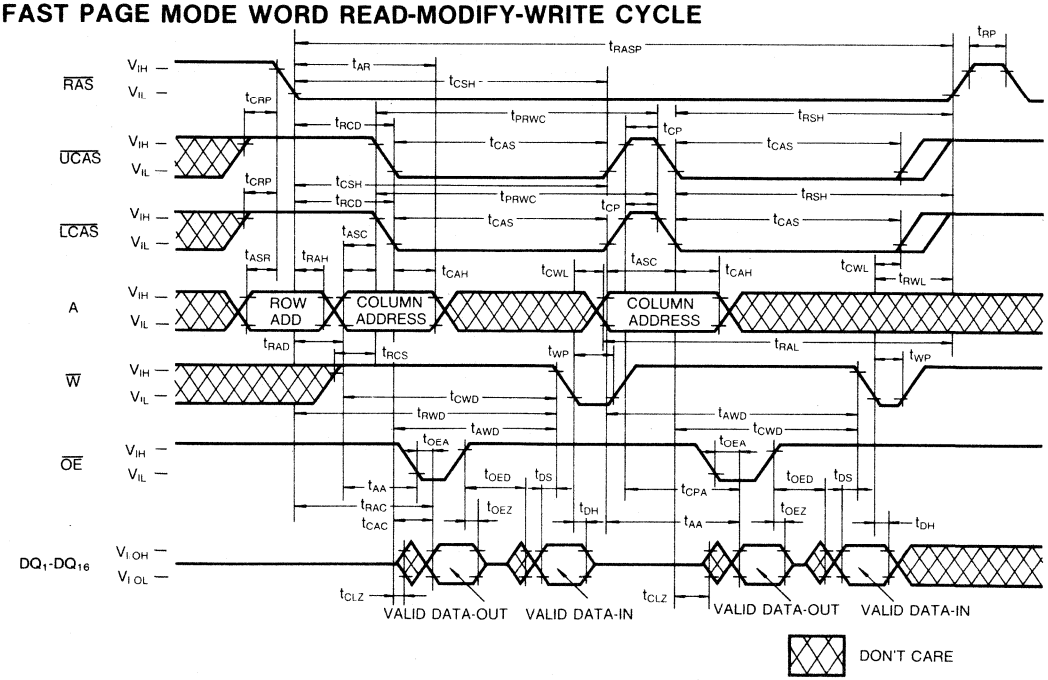


TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

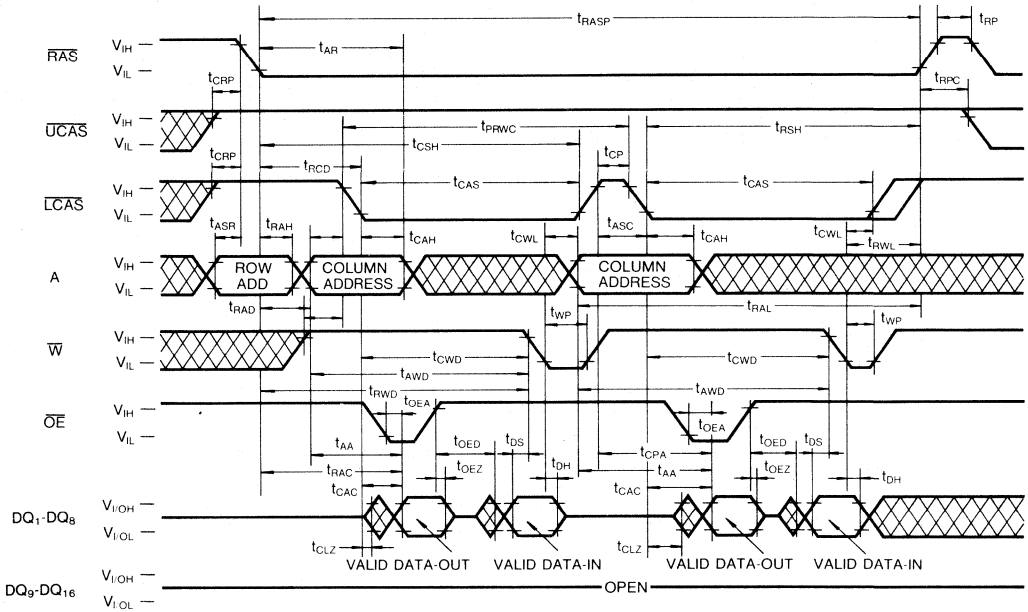


FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE

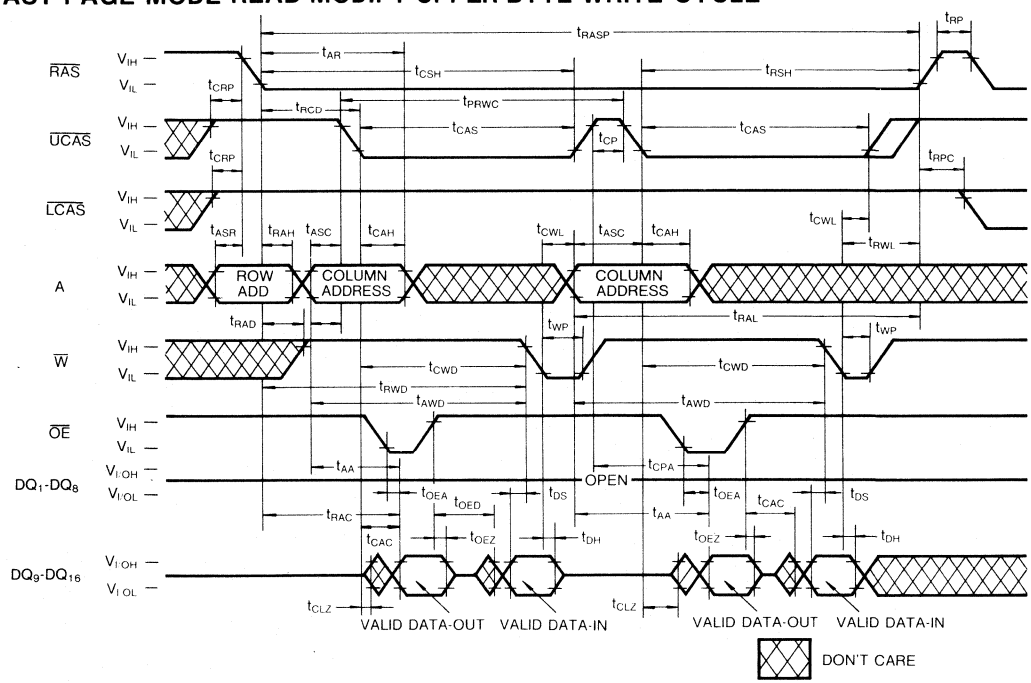


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE



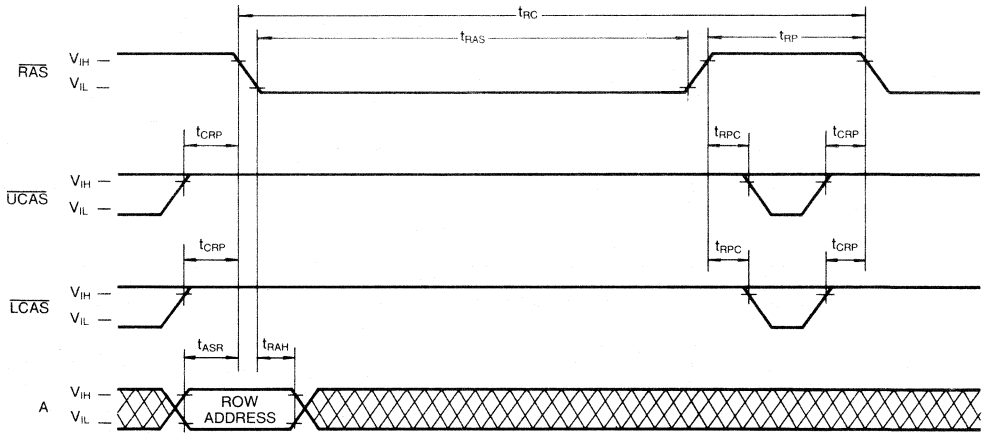
FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



TIMING DIAGRAMS (Continued)

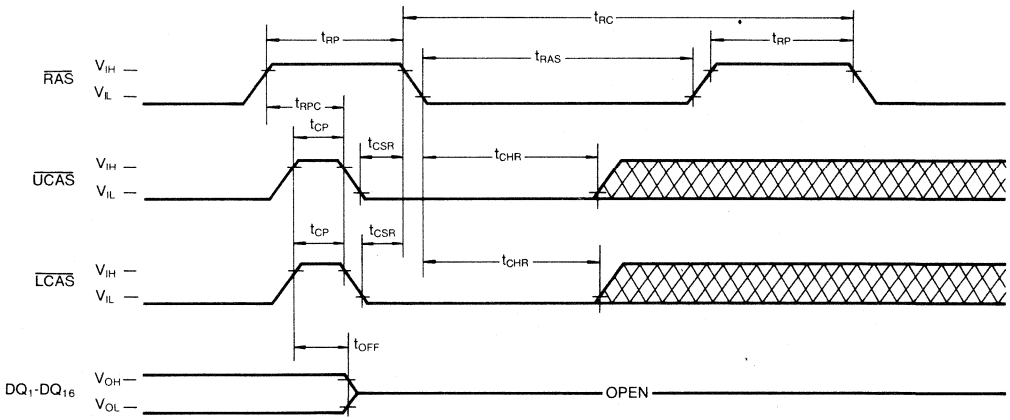
$\overline{RAS}$ ONLY REFRESH CYCLE

NOTE: $\overline{W}$, $\overline{OE}$=Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

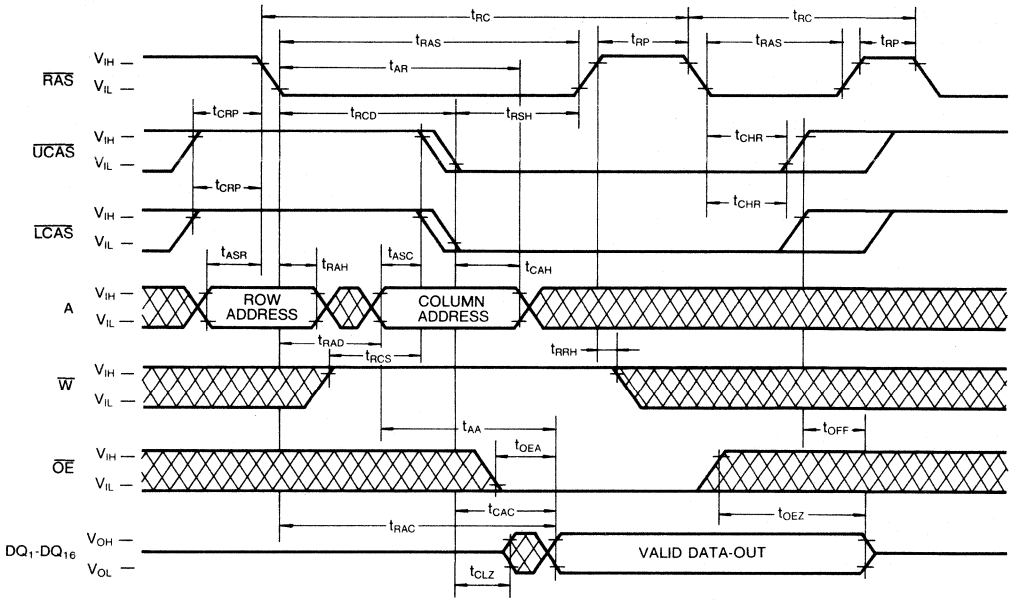
NOTE: $\overline{W}$=V_{IH}, $\overline{OE}$, A=Don't Care



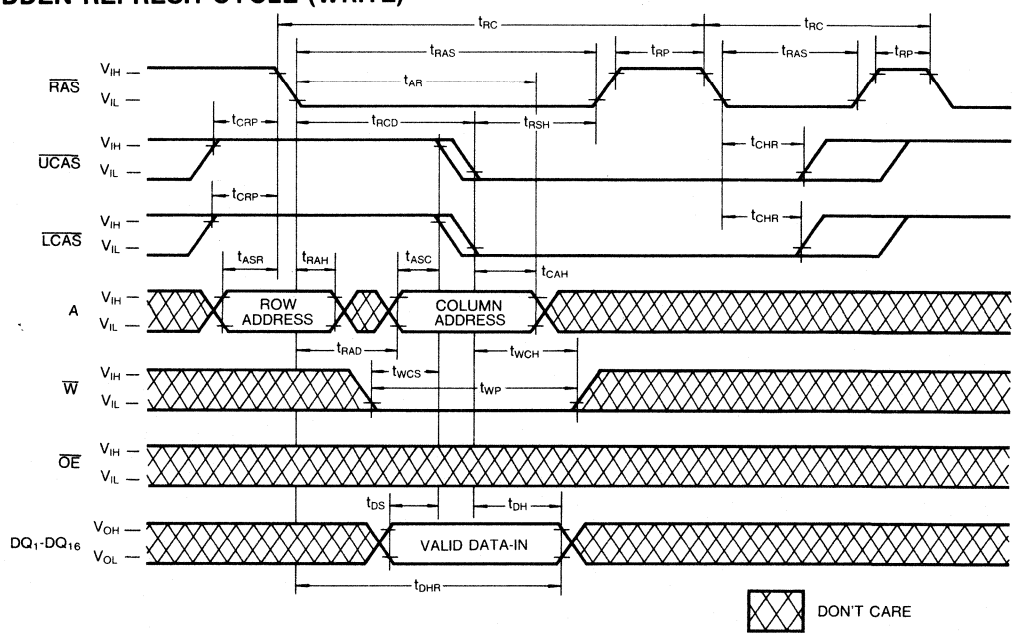
DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

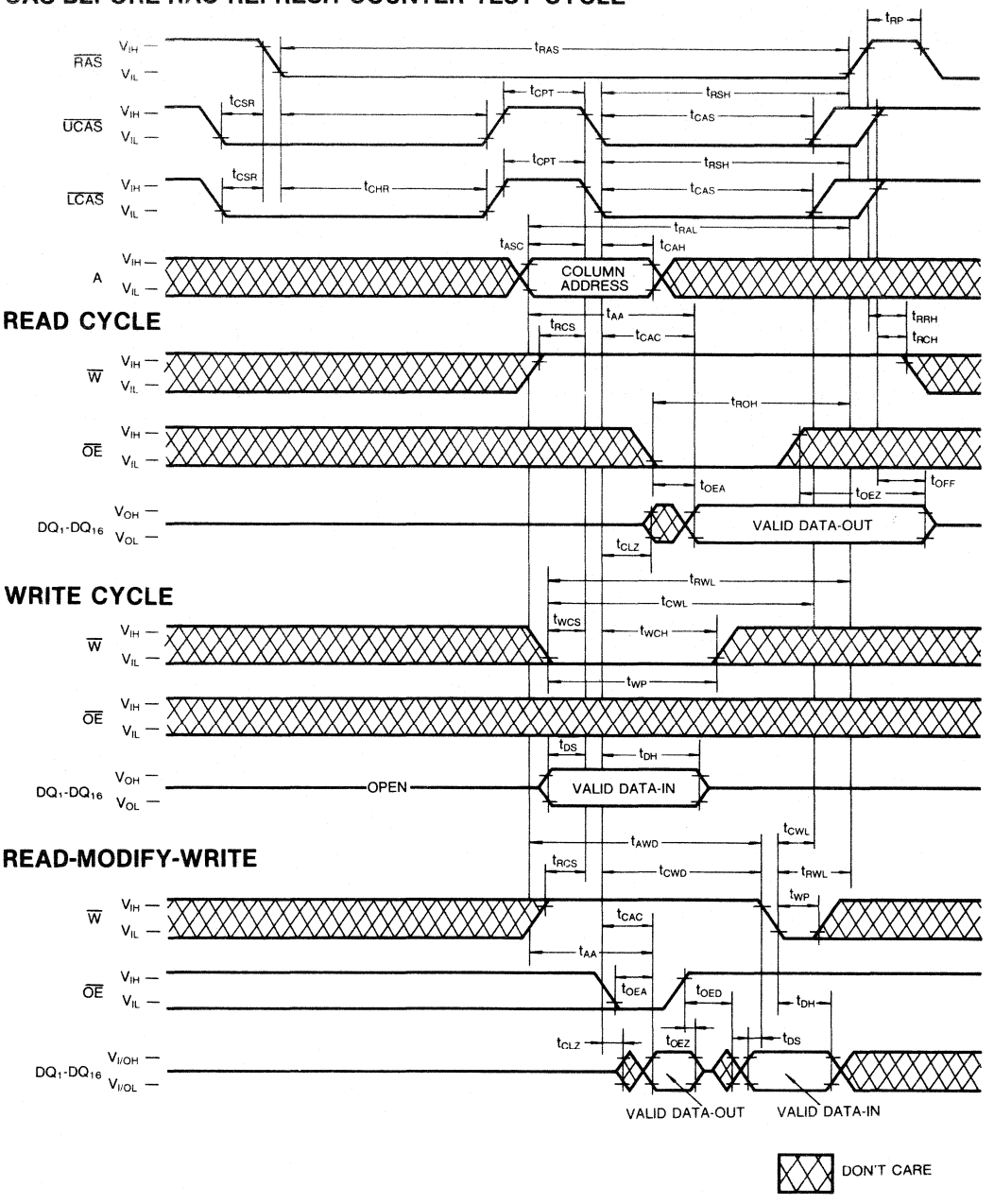


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The KM416C1200 contains 16,777,216 memory locations arranged in 16 groups of 1,048,576 × 1 bit each. Twenty address bits are required to address a particular memory location. Since the KM416C1200 has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{LCAS}$, $\overline{UCAS}$) and the valid row and column address inputs.

Operation of the KM416C1200 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{LCAS}$ ($\overline{UCAS}$) remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{LCAS}$ ($\overline{UCAS}$). This is the beginning of any KM416C1200 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{LCAS}$ ($\overline{UCAS}$) have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM416C1200 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{W}$) high during a $\overline{RAS}$/$\overline{xCAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. Additionally the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{xCAS}$ transitions to a low before t_{RCD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{xCAS}$ transitions low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to meet both t_{RCD}(max) and t_{RAD}(max).

Write

The KM416C1200 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$, $\overline{OE}$, $\overline{LCAS}$ and $\overline{UCAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{xCAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{xCAS}$. The 16 Bit wide data at the data I/O pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{OE}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cells appears at the output before and during the time that data is being written into the same cells. This cycle is achieved by bringin $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write timing requirements. The $\overline{OE}$ input must be low during the time defined by t_{OEA} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met output may contain invalid data. Conforming to the $\overline{OE}$ timing requirements prevents bus contention on the KM416C1200 DQ pins.

Data Output

The KM416C1200 has a three-state output buffers which are controlled by $\overline{CAS}$ and $\overline{OE}$. Whenever either $\overline{CAS}$ or $\overline{OE}$ is high (V_{IH}), the outputs are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the outputs, the outputs enter into the low impedance state in the time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM416C1200 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh, $\overline{OE}$ controlled write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write (t_{CWD} or t_{RWD} times are not met)

Refresh

The data in the KM416C1200 is stored as a charge on microscopic capacitor within each memory cell. The stored charge tends to dissipate over time and will af-

DEVICE OPERATION (Continued)

fect data integrity if the charge is not periodically refreshed. Refresh of the individual storage cells is accomplished by accessing all rows within the refresh period (t_{REF}) of within 16ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 1024 row address (A0-A9).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM416C1200 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If either $\overline{LCAS}$ or $\overline{UCAS}$ input is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ transitions low, the onchip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending either $\overline{LCAS}$ or $\overline{UCAS}$ input active time and cycling $\overline{RAS}$. The hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM416C1200 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The KM416C1200 has Fast page mode capability provides high speed read, write or read-modify-write access to all memory locations within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is held low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter test cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is asserted high and then low again while $\overline{RAS}$ is asserted low, the read and write operations are enabled. In this method, the row address bits A0 through A9 are supplied by on chip refresh counter.

Power-Up

If $\overline{RAS} = V_{SS}$ during power-up, the KM416C1200 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held a valid V_{IH} in order to minimize power-up current.
An initial pause of 200μs is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8ms period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

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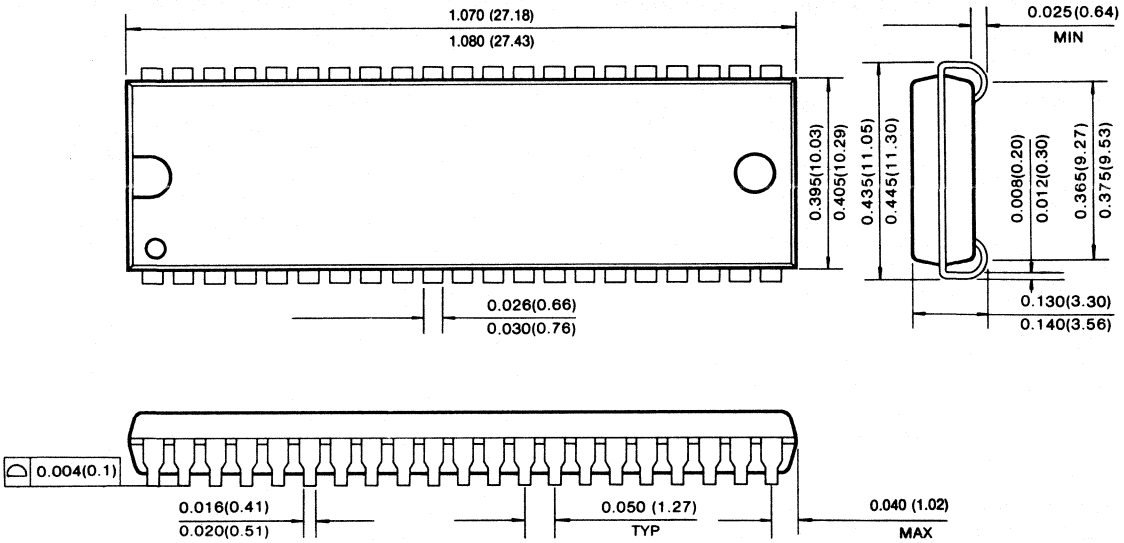

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